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ILI9225G

a-Si TFT LCD Single Chip Driver 176RGBx220 Resolution and 262K color

Specification

Preliminary

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1. Introduction

ILI9225G is a 262,144-color one-chip SoC driver for a-TFT liquid crystal display with resolution of 176RGBx220 dots, comprising a 528-channel source driver, a 220-channel gate driver, 87120 bytes RAM for graphic data of 176RGBx220 dots, and power supply circuit.

ILI9225G has four kinds of system interfaces which are i80/M68-system MPU interface (8-/9-/16-/18-bit bus width), serial data transfer interface (SPI) and RGB 6-/16-/18-bit interface (DOTCLK, VSYNC, HSYNC, ENABLE, DB[17:0]).

In RGB interface, the combined use of high-speed RAM write function and widow address function enables to display a moving picture at a position specified by a user and still pictures in other areas on the screen simultaneously, which makes it possible to transfer display the refresh data only to minimize data transfers and power consumption.

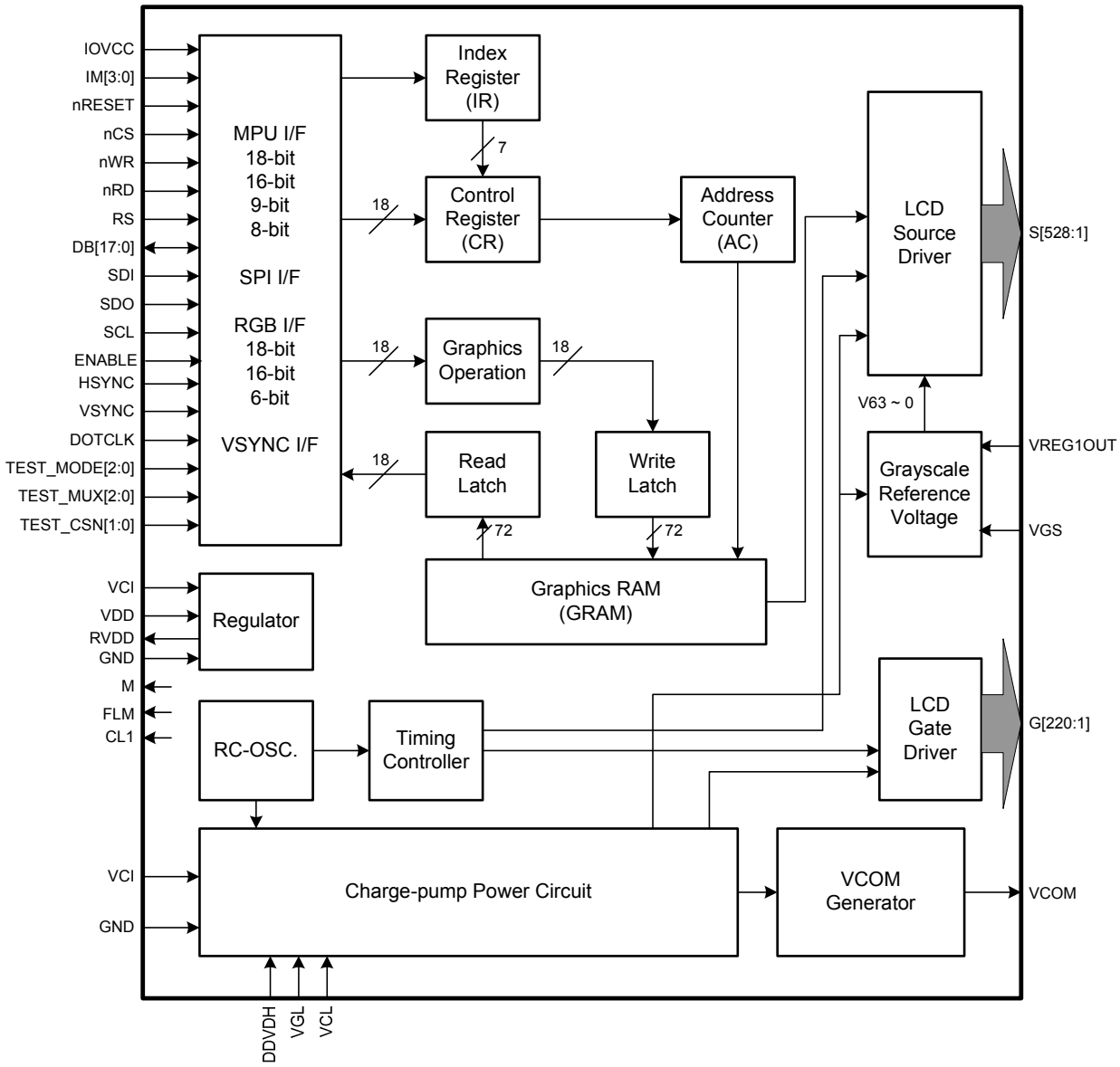
ILI9225G can operate with low I/O interface power supply up to 1.65V, with an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The ILI9225G also supports a function to display in 8 colors and a standby mode, allowing for precise power control by software. These features make the ILI9225G an ideal LCD driver for medium or small size portable products such as digital cellular phones or small PDA, where long battery life is a major concern.

2. Features

- Single chip solution for a liquid crystal QCIF+ TFT LCD display
- 176RGBx220-dot resolution capable of graphics display in 262,144 color
- Incorporate 528-channel source driver and 220-channel gate driver
- Internal 87,120 bytes graphic RAM
- High-speed RAM burst write function
- System interfaces
  - i80 system interface with 8-/ 9-/16-/18-bit bus width
  - M68 system interface with 8-/ 9-/16-/18-bit bus width
  - Serial Peripheral Interface (SPI)
  - RGB interface with 8-/16-/18-bit bus width (VSYNC, HSYNC, DOTCLK, ENABLE, DB[17:0])
- Reversible source/gate driver shift direction
- Window address function to specify a rectangular area for internal GRAM access
- Abundant functions for color display control
  - γ-correction function enabling display in 262,144 colors
  - Line-unit vertical scrolling function
- Partial drive function, enabling partially driving an LCD panel at positions specified by user
- Incorporate step-up circuits for stepping up a liquid crystal drive voltage level up to 6 times (x6)
- Power saving functions
  - 8-color mode
  - standby mode

- Low -power consumption architecture
  - Low operating power supplies:
    - IOVcc (VDD3) = 1.65 ~ 3.3 V (interface I/O)
    - Vci = 2.5 ~ 3.3 V
  - Low voltage drive: AVDD (AVDD) = 4.5 ~ 5.5 V

3. Block Diagram



4. Pin Descriptions

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Type</th><th>Descriptions</th></tr>
<tr><td colspan="4">Input Interface</td></tr>
<tr><td>IM3,
IM2,
IM1,
IM0/ID</td><td>I</td><td>IOVcc</td><td>Select the MPU system interface mode
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU-Interface Mode</th><th>DB Pin in use</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>M68-system 16-bit interface</td><td>DB[17:10], DB[8:1]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>M68-system 8-bit interface</td><td>DB[17:10]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>i80-system 16-bit interface</td><td>DB[17:10], DB[8:1]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>i80-system 8-bit interface</td><td>DB[17:10]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ID</td><td>24-bit 4 wires Serial Peripheral Interface (SPI)</td><td>SDI, SDO, SCL, nCS</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>9-bit 3 wires Serial Peripheral Interface</td><td>SDA, SCL, nCS</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>8-bit 4 wires Serial Peripheral Interface</td><td>SDA, SCL, nCS, RS (D/CX)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>M68-system 18-bit interface</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>M68-system 9-bit interface</td><td>DB[17:9]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>i80-system 18-bit interface</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>i80-system 9-bit interface</td><td>DB[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>*</td><td>*</td><td>Setting invalid</td><td></td></tr>
</table>
When the serial peripheral interface is selected, IM0 pin is used for the device code ID setting.</td></tr>
<tr><td>nCS</td><td>I</td><td>MPU
IOVcc</td><td>A chip select signal.
Low: the ILI9225G is selected and accessible
High: the ILI9225G is not selected and not accessible
Fix to IOVCC level when not in use.</td></tr>
<tr><td>RS (D/CX)</td><td>I</td><td>MPU
IOVcc</td><td>A register select signal.
Low: select an index or status register
High: select a control register
Fix to GND level when not in use.</td></tr>
<tr><td>RW_nWR /SCL</td><td>I</td><td>MPU
IOVcc</td><td>In 68-system mode, this is used to select operation, read or write. (RW)
In 80-system mode, this serves as a write strobe signal (nWR).
In SPI mode, it serves as a synchronous clock (SCL).</td></tr>
<tr><td>E_nRD</td><td>I</td><td>MPU
IOVcc</td><td>In 68-system mode, this serves as write/read enable strobe (E).
In 80-system mode, this serves as a read strobe signal. (nRD).
Must be fixed to GND level when SPI mode.</td></tr>
<tr><td>nRESET</td><td>I</td><td>MPU
IOVcc</td><td>A reset pin.
Initializes the ILI9225G with a low input. Be sure to execute a power-on reset after supplying power.</td></tr>
<tr><td>DB[17:0]</td><td>I/O</td><td>MPU
IOVcc</td><td>18-bit parallel bi-directional data bus for MPU system interface mode

Serves as an input data bus for MPU I/F.
8-bit I/F: DB[17:10] is used.</td></tr>
</table>

Pin Name	I/O	Type	Descriptions
			9-bit I/F: DB[17:9] is used. 16-bit I/F: DB[17:10] and DB[8:1] is used. 18-bit I/F: DB[17:0] is used. Serves as an input data bus for RGB I/F. 6-bit interface: DB[17:12] 16-bit interface: {DB[17:13], DB[11:1]} 18-bit interface: DB[17:0] **Unused pins must be fixed GND level.**
SDI/SDA	I/O	MPU IOVcc	In the 24-bit 4 wires serial peripheral interface, this pin is used as input pin. In the 8/9-bit serial peripheral interface, this pin is used as bi-directional data pin. **Fix to GND level when not in use.**
SDO	O	MPU IOVcc	Serial data output (SDO) pin in serial interface operation. The data is outputted on the falling edge of the SCL signal. ***When the SPI interface is not used, please let SDO as floating.***
DOTCLK	I	MPU IOVcc	A dot clock signal. DPL = "0": Input data on the rising edge of DOTCLK DPL = "1": Input data on the falling edge of DOTCLK **Fix to GND level when not in use.**
VSYNC	I	MPU IOVcc	A frame synchronizing signal. VSPL = "0": Active low. VSPL = "1": Active high. **Fix to GND level when not in use.**
HSYNC	I	MPU IOVcc	A line synchronizing signal. HSPL = "0": Active low. HSPL = "1": Active high. **Fix to GND level when not in use.**
ENABLE	I	MPU IOVcc	A data ENEABLE signal in RGB interface mode. Low: Select (access enabled) High: Not select (access inhibited) The EPL bit inverts the polarity of the ENABLE signal. **Fix to GND level when not in use.**
LCD Driving signals			
S528~S1	O	LCD	Source output voltage signals applied to liquid crystal.

Pin Name	I/O	Type	Descriptions
			To change the shift direction of signal outputs, use the SS bit. SS = "0", the data in the RAM address "h00000" is output from S1. SS = "1", the data in the RAM address "h00000" is output from S528. S1, S4, S7, … display red (R), S2, S5, S8, ... display green (G), and S3, S6, S9, ... display blue (B) (SS = 0).
G220~G1	O	LCD	Gate line output signals. VGH: the level selecting gate lines VGL: the level not selecting gate lines
VCOM	O	TFT common electrode	A supply voltage to the common electrode of TFT panel. VCOM is AC voltage alternating signal between the VCOMH and VCOML levels.
Charge-pump and Regulator Circuit			
VCOMH	O	-	The high level of VCOM AC voltage.
VCOML	O	-	The low level of VCOM AC voltage. Adjust the VCOML level with the VML[6:0] bits. To fix the VCOML level to GND and set VCOMG = "0".
VCOMR	-	open	ILI9225GThis is a floating pad. Leave this pin open.
C11P, C11M C12P, C12M	-	open	Generating AVDD level.
C21P, C21M C22P, C22M	-	open	Generating VGH, VGL level.
C31P, C31M	-	open	Generating VCL level.
AVDD	O	Stabilizing capacitor, AVDD	An output voltage from the step-up circuit 1, twice the Vci level. See "Configurations of Power supply circuit". AVDD = 4.5 ~ 5.5V
VGH	O	-	An output voltage from the step-up circuit 2, 6 ~ 7 times the Vci level. The step-up rate is set with the BT bits. See "Configurations of Power supply circuit". VGH = max 15.5V
VGL	O	Stabilizing capacitor, VGL	An output voltage from the step-up circuit 2, -5 ~ -7 times the Vci level. The step-up rate is set with the BT bits. See "Configurations of Power supply circuit". VGL = min –13V
VCL	O	Stabilizing capacitor, VCL	An output voltage from the step-up circuit 3, –1 times the Vci level. Connect to a stabilizing capacitor. VCL = 0 ~ –Vci

Pin Name	I/O	Type	Descriptions
GVDD (GVDD)	I/O	-	A reference voltage level. The voltage level of GVDD can be adjusted by the GVD[6:0] bits. GVDD is a source driver grayscale reference voltage. GVDD = (Vci+0.3) ~ (AVDD – 0.5)V
VGS	I	GND or external resistor	A reference level for the grayscale voltage generating circuit. The VGS level can be changed by connecting to an external resistor.
VREF	-	-	Floating pin. This pin is a floating pin.
Power Pads			
Vci	I	Power supply	A supply voltage to the analog circuit. Connect to an external power supply of 2.5 ~ 3.3V.
IOVCC (VDD3)	I	Power supply	A supply voltage to the interface pins (IOVcc = 1.65 ~ 3.3V).
AVSS (GND)	P	-	GND for analog circuits
VSSC (GND)	P	-	GND for booster circuits.
VSS (GND)	P	-	GND for logic circuits.
RVDD	P	-	Voltage regulator output for VDD. Connect to VDD pad for supplying power.
VDD	P	RVDD	Power supply for memory and internal logic circuit. Connect this pin to regulated voltage output RVDD. Do not apply any external power to this pin over 1.8V.
Test Pads			
CL1	O	-	Output pins used only for test purpose at vendor-side. In normal operation, leave this pin open.
FLM	O	-	Tearing effect output pin to synchronize MCU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
M	O	-	Output pins used only for test purpose at vendor-side. In normal operation, leave this pin open.
TEST_MODE[2:0]	I	-	Input pins used only for test purpose In normal operation, connect this pin to VSS or IOVCC.
TEST_MUX[2]	I	-	Input pins used only for test purpose This pin is internal pull low. In normal operation, please connect this pin to GND or leave this pin as open.
TEST_MUX[1:0]	I	-	Input pins used only for test purpose In normal operation, connect this pin to VSS or IOVCC.

Pin Name	I/O	Type	Descriptions
TEST_DA	I	-	Input pins used only for test purpose In normal operation, connect this pin to VSS or IOVCC.
Contact	-	-	Contact resistance measurement pin.
EXCLK	I	-	Test pin In normal operation, connect this pin to VSS or IOVCC.
EN_EXCLK	I	-	Test pin In normal operation, connect this pin to VSS or IOVCC.

Liquid crystal power supply specifications Table 1

No.	Item		Description
1	TFT data lines		528 pins (176 x RGB)
2	TFT gate lines		220 pins
3	TFT display's capacitor structure		Cst structure only (Common VCOM)
4	Liquid crystal drive output	S1 ~ S528	V0 ~ V63 grayscales
		G1 ~ G220	VGH - VGL
		VCOM	VCOMH - VCOML: Amplitude = electronic volumes
5	Input voltage	IOVcc	1.65V ~ 3.30V
		Vci	2.50V ~ 3.30V
6	Internal step-up circuits	AVDD	Vci x 2
		VGH	Vci x 6, x 7
		VGL	Vci x -5, x -6, x -7
		VCL	Vci x -1

5. Pad Arrangement and Coordination

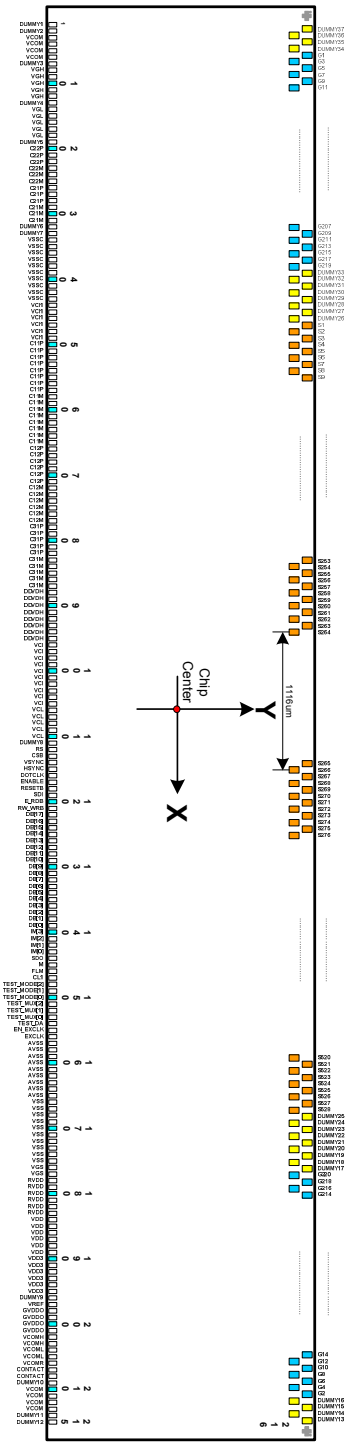
Chip Size: 13880um x 670um

Chip thickness : 280 um / 400 um

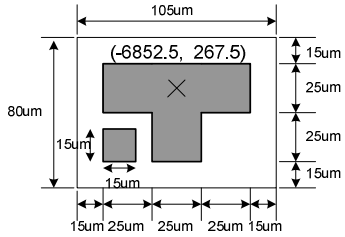
Pad Location: Pad Center.

Coordinate Origin: Chip Center

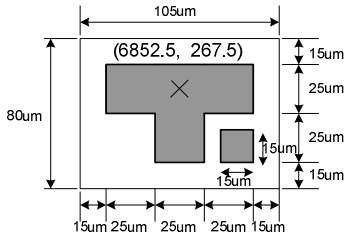
Au bump height: 12 um



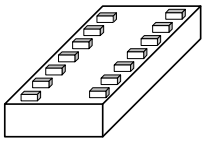
Alignment Mark-Left



Alignment Mark-Right



Face Up
(Bump View)



No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y	No.	Name	X	Y
1	DUMMY1	-6695	-253	51	C11P	-3695	-253	101	VCI	-695	-253	151	TEST_MUX<2>	2855	-253	201	GVDD	5855	-253
2	DUMMY2	-6635	-253	52	C11P	-3635	-253	102	VCI	-635	-253	152	TEST_MUX<1>	2915	-253	202	VCOMH	5915	-253
3	VCOM	-6575	-253	53	C11P	-3575	-253	103	VCI	-575	-253	153	TEST_MUX<0>	2975	-253	203	VCOMH	5975	-253
4	VCOM	-6515	-253	54	C11P	-3515	-253	104	VCI	-515	-253	154	TEST_DA	3035	-253	204	VCOML	6035	-253
5	VCOM	-6455	-253	55	C11P	-3455	-253	105	VCI	-455	-253	155	EN_EXCLK	3095	-253	205	VCOML	6095	-253
6	VCOM	-6395	-253	56	C11P	-3395	-253	106	VCL	-395	-253	156	EXCLK	3155	-253	206	VCOMR	6155	-253
7	DUMMY3	-6335	-253	57	C11P	-3335	-253	107	VCL	-335	-253	157	AVSS	3215	-253	207	CONTACT	6215	-253
8	VGH	-6275	-253	58	C11M	-3275	-253	108	VCL	-275	-253	158	AVSS	3275	-253	208	CONTACT	6275	-253
9	VGH	-6215	-253	59	C11M	-3215	-253	109	VCL	-215	-253	159	AVSS	3335	-253	209	DUMMY10	6335	-253
10	VGH	-6155	-253	60	C11M	-3155	-253	110	VCL	-155	-253	160	AVSS	3395	-253	210	VCOM	6395	-253
11	VGH	-6095	-253	61	C11M	-3095	-253	111	DUMMY8	-95	-253	161	AVSS	3455	-253	211	VCOM	6455	-253
12	VGH	-6035	-253	62	C11M	-3035	-253	112	RS	-35	-253	162	AVSS	3515	-253	212	VCOM	6515	-253
13	DUMMY4	-5975	-253	63	C11M	-2975	-253	113	CSB	25	-253	163	AVSS	3575	-253	213	VCOM	6575	-253
14	VGL	-5915	-253	64	C11M	-2915	-253	114	VSYNC	85	-253	164	AVSS	3635	-253	214	DUMMY11	6635	-253
15	VGL	-5855	-253	65	C11M	-2855	-253	115	HSYNC	145	-253	165	AVSS	3695	-253	215	DUMMY12	6695	-253
16	VGL	-5795	-253	66	C12P	-2795	-253	116	DOTCLK	205	-253	166	VSS	3755	-253	216	DUMMY13	6772	232
17	VGL	-5735	-253	67	C12P	-2735	-253	117	ENABLE	265	-253	167	VSS	3815	-253	217	DUMMY14	6756	107
18	VGL	-5675	-253	68	C12P	-2675	-253	118	RESETB	325	-253	168	VSS	3875	-253	218	DUMMY15	6740	232
19	DUMMY5	-5615	-253	69	C12P	-2615	-253	119	SDI	385	-253	169	VSS	3935	-253	219	DUMMY16	6724	107
20	C22P	-5555	-253	70	C12P	-2555	-253	120	E_RDB	445	-253	170	VSS	3995	-253	220	G<2>	6708	232
21	C22P	-5495	-253	71	C12P	-2495	-253	121	RW_WRB	505	-253	171	VSS	4055	-253	221	G<4>	6692	107
22	C22P	-5435	-253	72	C12M	-2435	-253	122	DB<17>	565	-253	172	VSS	4115	-253	222	G<6>	6676	232
23	C22M	-5375	-253	73	C12M	-2375	-253	123	DB<16>	650	-253	173	VSS	4175	-253	223	G<8>	6660	107
24	C22M	-5315	-253	74	C12M	-2315	-253	124	DB<15>	735	-253	174	VSS	4235	-253	224	G<10>	6644	232
25	C22M	-5255	-253	75	C12M	-2255	-253	125	DB<14>	820	-253	175	VSS	4295	-253	225	G<12>	6628	107
26	C21P	-5195	-253	76	C12M	-2195	-253	126	DB<13>	905	-253	176	VGS	4355	-253	226	G<14>	6612	232
27	C21P	-5135	-253	77	C12M	-2135	-253	127	DB<12>	990	-253	177	VGS	4415	-253	227	G<16>	6596	107
28	C21P	-5075	-253	78	C31P	-2075	-253	128	DB<11>	1075	-253	178	RVDD	4475	-253	228	G<18>	6580	232
29	C21M	-5015	-253	79	C31P	-2015	-253	129	DB<10>	1160	-253	179	RVDD	4535	-253	229	G<20>	6564	107
30	C21M	-4955	-253	80	C31P	-1955	-253	130	DB<9>	1245	-253	180	RVDD	4595	-253	230	G<22>	6548	232
31	C21M	-4895	-253	81	C31P	-1895	-253	131	DB<8>	1330	-253	181	RVDD	4655	-253	231	G<24>	6532	107
32	DUMMY6	-4835	-253	82	C31P	-1835	-253	132	DB<7>	1415	-253	182	RVDD	4715	-253	232	G<26>	6516	232
33	DUMMY7	-4775	-253	83	C31M	-1775	-253	133	DB<6>	1500	-253	183	RVDD	4775	-253	233	G<28>	6500	107
34	VSSC	-4715	-253	84	C31M	-1715	-253	134	DB<5>	1585	-253	184	VDD	4835	-253	234	G<30>	6484	232
35	VSSC	-4655	-253	85	C31M	-1655	-253	135	DB<4>	1670	-253	185	VDD	4895	-253	235	G<32>	6468	107
36	VSSC	-4595	-253	86	C31M	-1595	-253	136	DB<3>	1755	-253	186	VDD	4955	-253	236	G<34>	6452	232
37	VSSC	-4535	-253	87	C31M	-1535	-253	137	DB<2>	1840	-253	187	VDD	5015	-253	237	G<36>	6436	107
38	VSSC	-4475	-253	88	AVDD	-1475	-253	138	DB<1>	1925	-253	188	VDD	5075	-253	238	G<38>	6420	232
39	VSSC	-4415	-253	89	AVDD	-1415	-253	139	DB<0>	2010	-253	189	VDD	5135	-253	239	G<40>	6404	107
40	VSSC	-4355	-253	90	AVDD	-1355	-253	140	IM<3>	2095	-253	190	VDD3	5195	-253	240	G<42>	6388	232
41	VSSC	-4295	-253	91	AVDD	-1295	-253	141	IM<2>	2155	-253	191	VDD3	5255	-253	241	G<44>	6372	107
42	VSSC	-4235	-253	92	AVDD	-1235	-253	142	IM<1>	2215	-253	192	VDD3	5315	-253	242	G<46>	6356	232
43	VSSC	-4175	-253	93	AVDD	-1175	-253	143	IM<0>	2275	-253	193	VDD3	5375	-253	243	G<48>	6340	107
44	VCI1	-4115	-253	94	AVDD	-1115	-253	144	SDO	2335	-253	194	VDD3	5435	-253	244	G<50>	6324	232
45	VCI1	-4055	-253	95	AVDD	-1055	-253	145	M	2420	-253	195	VDD3	5495	-253	245	G<52>	6308	107
46	VCI1	-3995	-253	96	VCI	-995	-253	146	FLM	2505	-253	196	DUMMY9	5555	-253	246	G<54>	6292	232
47	VCI1	-3935	-253	97	VCI	-935	-253	147	CL1	2590	-253	197	VREF	5615	-253	247	G<56>	6276	107
48	VCI1	-3875	-253	98	VCI	-875	-253	148	TEST_MODE<2>	2675	-253	198	GVDD	5675	-253	248	G<58>	6260	232
49	VCI1	-3815	-253	99	VCI	-815	-253	149	TEST_MODE<1>	2735	-253	199	GVDD	5735	-253	249	G<60>	6244	107
50	C11P	-3755	-253	100	VCI	-755	-253	150	TEST_MODE<0>	2795	-253	200	GVDD	5795	-253	250	G<62>	6228	232

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252	G<66>	6196	232	302	G<166>	5396	232	352	S<515>	4596	232	402	S<465>	3796	232	452	S<415>	2996	232
253	G<68>	6180	107	303	G<168>	5380	107	353	S<514>	4580	107	403	S<464>	3780	107	453	S<414>	2980	107
254	G<70>	6164	232	304	G<170>	5364	232	354	S<513>	4564	232	404	S<463>	3764	232	454	S<413>	2964	232
255	G<72>	6148	107	305	G<172>	5348	107	355	S<512>	4548	107	405	S<462>	3748	107	455	S<412>	2948	107
256	G<74>	6132	232	306	G<174>	5332	232	356	S<511>	4532	232	406	S<461>	3732	232	456	S<411>	2932	232
257	G<76>	6116	107	307	G<176>	5316	107	357	S<510>	4516	107	407	S<460>	3716	107	457	S<410>	2916	107
258	G<78>	6100	232	308	G<178>	5300	232	358	S<509>	4500	232	408	S<459>	3700	232	458	S<409>	2900	232
259	G<80>	6084	107	309	G<180>	5284	107	359	S<508>	4484	107	409	S<458>	3684	107	459	S<408>	2884	107
260	G<82>	6068	232	310	G<182>	5268	232	360	S<507>	4468	232	410	S<457>	3668	232	460	S<407>	2868	232
261	G<84>	6052	107	311	G<184>	5252	107	361	S<506>	4452	107	411	S<456>	3652	107	461	S<406>	2852	107
262	G<86>	6036	232	312	G<186>	5236	232	362	S<505>	4436	232	412	S<455>	3636	232	462	S<405>	2836	232
263	G<88>	6020	107	313	G<188>	5220	107	363	S<504>	4420	107	413	S<454>	3620	107	463	S<404>	2820	107
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265	G<92>	5988	107	315	G<192>	5188	107	365	S<502>	4388	107	415	S<452>	3588	107	465	S<402>	2788	107
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267	G<96>	5956	107	317	G<196>	5156	107	367	S<500>	4356	107	417	S<450>	3556	107	467	S<400>	2756	107
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503	S<364>	2130	107	553	S<314>	1330	107	603	S<264>	-554	107	653	S<214>	-1354	107	703	S<164>	-2154	107
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514	S<353>	1954	232	564	S<303>	1154	232	614	S<253>	-730	232	664	S<203>	-1530	232	714	S<153>	-2330	232
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545	S<322>	1458	107	595	S<272>	658	107	645	S<222>	-1226	107	695	S<172>	-2026	107	745	S<122>	-2876	107
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547	S<320>	1426	107	597	S<270>	626	107	647	S<220>	-1258	107	697	S<170>	-2058	107	747	S<120>	-2908	107
548	S<319>	1410	232	598	S<269>	610	232	648	S<219>	-1274	232	698	S<169>	-2074	232	748	S<119>	-2924	232
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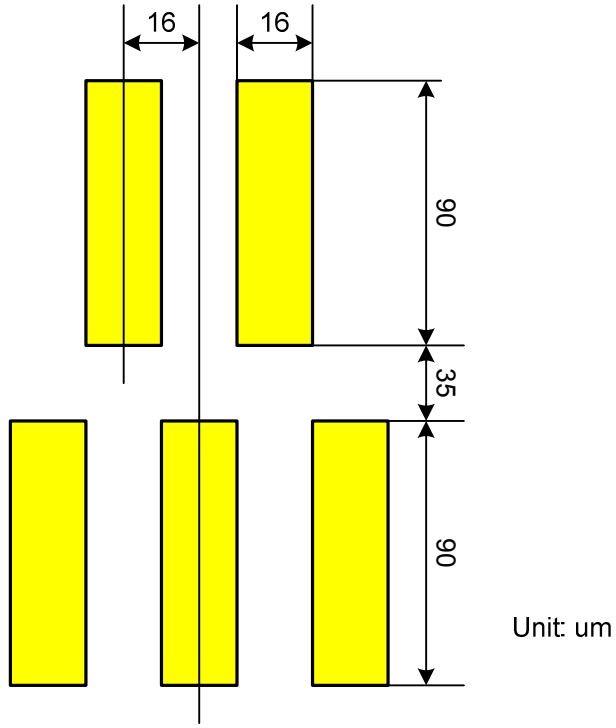
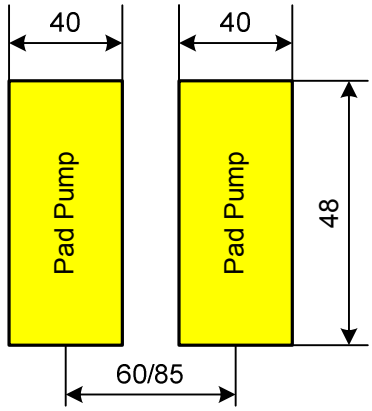
773	S<94>	-3324	107	823	S<44>	-4124	107	873	DUMMY32	-4924	107	923	G<123>	-5724	107	973	G<23>	-6524	107
774	S<93>	-3340	232	824	S<43>	-4140	232	874	DUMMY33	-4940	232	924	G<121>	-5740	232	974	G<21>	-6540	232
775	S<92>	-3356	107	825	S<42>	-4156	107	875	G<219>	-4956	107	925	G<119>	-5756	107	975	G<19>	-6556	107
776	S<91>	-3372	232	826	S<41>	-4172	232	876	G<217>	-4972	232	926	G<117>	-5772	232	976	G<17>	-6572	232
777	S<90>	-3388	107	827	S<40>	-4188	107	877	G<215>	-4988	107	927	G<115>	-5788	107	977	G<15>	-6588	107
778	S<89>	-3404	232	828	S<39>	-4204	232	878	G<213>	-5004	232	928	G<113>	-5804	232	978	G<13>	-6604	232
779	S<88>	-3420	107	829	S<38>	-4220	107	879	G<211>	-5020	107	929	G<111>	-5820	107	979	G<11>	-6620	107
780	S<87>	-3436	232	830	S<37>	-4236	232	880	G<209>	-5036	232	930	G<109>	-5836	232	980	G<9>	-6636	232
781	S<86>	-3452	107	831	S<36>	-4252	107	881	G<207>	-5052	107	931	G<107>	-5852	107	981	G<7>	-6652	107
782	S<85>	-3468	232	832	S<35>	-4268	232	882	G<205>	-5068	232	932	G<105>	-5868	232	982	G<5>	-6668	232
783	S<84>	-3484	107	833	S<34>	-4284	107	883	G<203>	-5084	107	933	G<103>	-5884	107	983	G<3>	-6684	107
784	S<83>	-3500	232	834	S<33>	-4300	232	884	G<201>	-5100	232	934	G<101>	-5900	232	984	G<1>	-6700	232
785	S<82>	-3516	107	835	S<32>	-4316	107	885	G<199>	-5116	107	935	G<99>	-5916	107	985	DUMMY34	-6716	107
786	S<81>	-3532	232	836	S<31>	-4332	232	886	G<197>	-5132	232	936	G<97>	-5932	232	986	DUMMY35	-6732	232
787	S<80>	-3548	107	837	S<30>	-4348	107	887	G<195>	-5148	107	937	G<95>	-5948	107	987	DUMMY36	-6748	107
788	S<79>	-3564	232	838	S<29>	-4364	232	888	G<193>	-5164	232	938	G<93>	-5964	232	988	DUMMY37	-6764	232
789	S<78>	-3580	107	839	S<28>	-4380	107	889	G<191>	-5180	107	939	G<91>	-5980	107	Alignment Mark Left		-6852.5	267.5
790	S<77>	-3596	232	840	S<27>	-4396	232	890	G<189>	-5196	232	940	G<89>	-5996	232	Alignment Mark Right		6852.5	267.5
791	S<76>	-3612	107	841	S<26>	-4412	107	891	G<187>	-5212	107	941	G<87>	-6012	107				
792	S<75>	-3628	232	842	S<25>	-4428	232	892	G<185>	-5228	232	942	G<85>	-6028	232				
793	S<74>	-3644	107	843	S<24>	-4444	107	893	G<183>	-5244	107	943	G<83>	-6044	107				
794	S<73>	-3660	232	844	S<23>	-4460	232	894	G<181>	-5260	232	944	G<81>	-6060	232				
795	S<72>	-3676	107	845	S<22>	-4476	107	895	G<179>	-5276	107	945	G<79>	-6076	107				
796	S<71>	-3692	232	846	S<21>	-4492	232	896	G<177>	-5292	232	946	G<77>	-6092	232				
797	S<70>	-3708	107	847	S<20>	-4508	107	897	G<175>	-5308	107	947	G<75>	-6108	107				
798	S<69>	-3724	232	848	S<19>	-4524	232	898	G<173>	-5324	232	948	G<73>	-6124	232				
799	S<68>	-3740	107	849	S<18>	-4540	107	899	G<171>	-5340	107	949	G<71>	-6140	107				
800	S<67>	-3756	232	850	S<17>	-4556	232	900	G<169>	-5356	232	950	G<69>	-6156	232				

S1 ~ S528 G1 ~ G220 (pin 216 ~ 988)	
I/O Pads (pin 1 ~ 215)	

6. Block Description

MPU System Interface

ILI9225G supports three system high-speed interfaces: i80/M68-system high-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports and serial peripheral interface (SPI). The interface mode is selected by setting the IM[3:0] pins.

ILI9225G has a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the ILI9225G read the first data from the internal GRAM. Valid data are read out after the ILI9225G performs the second read operation.
Registers are written consecutively as the register execution time except starting oscillator takes 0 clock cycle.

Registers selection by system interface (8-/9-/16-/18-bit bus width)		I80		M68	
Function	RS	nWR	nRD	E	RW
Write an index to IR register	0	0	1	1	0
Read an internal status	0	1	0	1	1
Write to control registers or the internal GRAM by WDR register.	1	0	1	1	0
Read from the internal GRAM by RDR register.	1	1	0	1	1

Registers selection by the SPI system interface		
Function	R/W	RS
Write an index to IR register	0	0
Read an internal status	1	0
Write to control registers or the internal GRAM by WDR register.	0	1
Read from the internal GRAM by RDR register.	1	1

Parallel RGB Interface

ILI9225G supports the RGB interface as the external interface for displaying a moving picture. When the RGB interface is selected, display operations are synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface mode, data (DB17-0) are written in synchronization with these signals according to the polarity of enable signal (ENABLE) to prevent flicker on display while updating display data.
The RGB interface, by writing all display data to the internal RAM, allows for transferring data only when updating the frames of a moving picture, contributing to low power requirement for moving picture display.

Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As writing data to the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

Graphics RAM (GRAM)

GRAM is graphics RAM storing bit-pattern data of 87,120 (176 x 220x 18/8) bytes, using 18 bits for each pixel.

Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates a liquid crystal drive voltage according to grayscale data set in the γ-correction register to display in 262,144 colors. For details, see the "γ-Correction Register" section.

Timing Controller

The timing generator generates a timing signal for operation of internal circuits such as the internal GRAM. The timing for the display operation such as RAM read operation and the timing for the internal operation such as access from the MPU are generated in the way not to interfere each other.

Oscillator (OSC.)

The ILI9225G can provide R-C oscillation without external resistor. The appropriate oscillation frequency for operation voltage, display size, and frame frequency can be obtained by adjusting the register setting value[R0Fh]. Clock pulse can also be supplied externally. Since R-C oscillation stops during the standby mode, currentconsumption can be reduced. For details, see the Oscillation Circuit section.

ILI9225G

LCD Driver Circuit

The LCD driver circuit of ILI9225G consists of a 528-output source driver (S1 ~ S528) and a 220-output gate driver (G1~G220). Display pattern data are latched when the 528th bit data are input. The latched data control the source driver and generate a drive waveform. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 528-bit source outputs from the source driver is set with the SS bit and the shift direction of gate outputs from the gate driver is set with the GS bit. The scan mode by the gate driver is set with the SM bit. These bits allow setting an appropriate scan method for an LCD module.

LCD Driver Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels GVDD, VGH, VGL and Vcom for driving an LCD.

7. System Interface

7.1. Interface Specifications

ILI9225G has the system interface to read/write the control registers and display graphics memory (GRAM), and the RGB Input Interface for displaying a moving picture. User can select an optimum interface to display the moving or still picture with efficient data transfer. All display data are stored in the GRAM to reduce the data transfer efforts and only the updating data is necessary to be transferred. User can only update a sub-range of GRAM by using the window address function.

ILI9225G also has the RGB interface to transfer the display data without flicker the moving picture on the screen. In RGB interface mode, the display data is written into the GRAM through the control signals of ENABLE, VSYNC, HSYNC, DOTCLK and data bus DB[17:0].

ILI9225G operates in one of the following 3 modes. The display mode can be switched by the control register. When switching from one mode to another, refer to the sequences mentioned in the sections of RGB interfaces.

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM)
Internal operating clock only (Displaying still pictures)	System interface (RM = 0)	Internal operating clock (DM=0)
RGB interface (1) (Displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM=1)
RGB interface (2) (Rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM=1)

Note 1) Registers are set only via the system interface.

Note 2) The RGB-I/F is not available simultaneously.

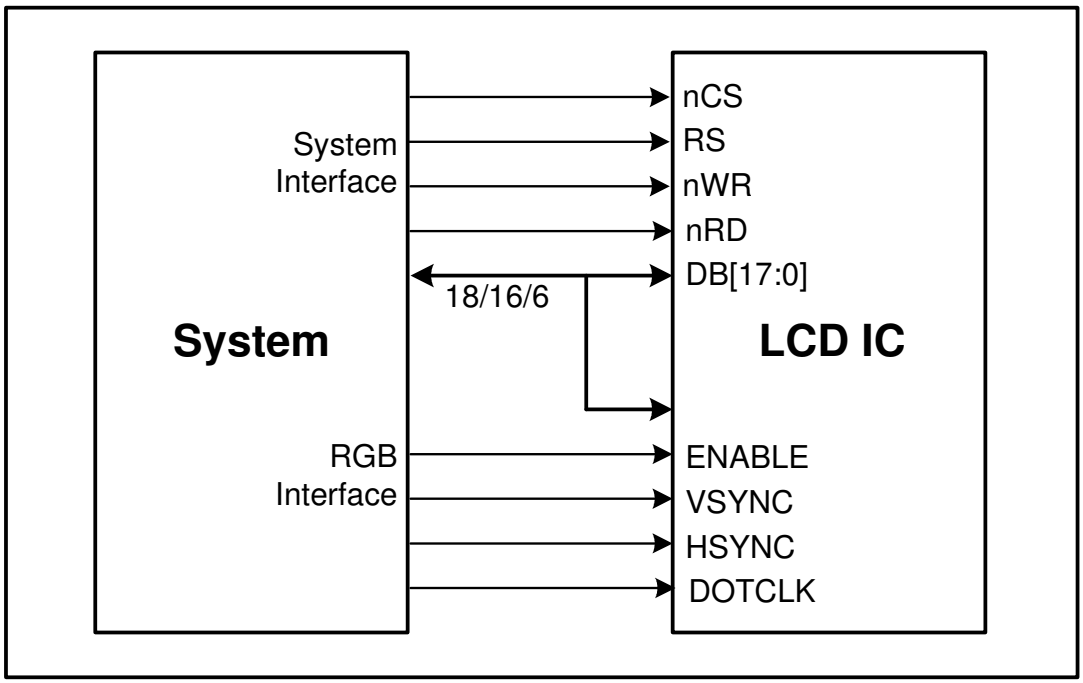


Figure1 System Interface and RGB Interface connection

7.2. Input Interfaces

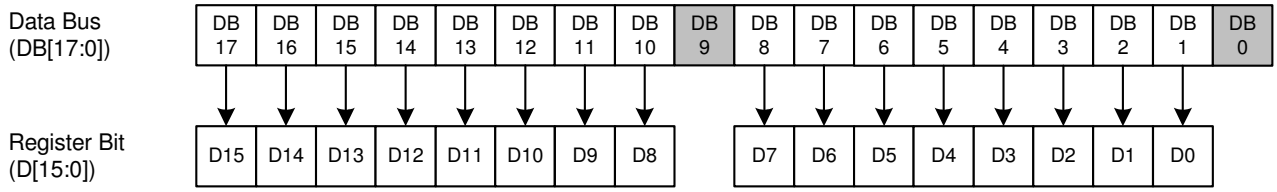
The following are the system interfaces available with the ILI9225G. The interface is selected by setting the IM[3:0] pins. The system interface is used for setting instructions and RAM access.

IM3	IM2	IM1	IM0/ID	Interface Mode	DB Pin
0	0	0	0	M68-system 16-bit interface	DB[17:10], DB[8:1]
0	0	0	1	M68-system 8-bit interface	DB[17:10]
0	0	1	0	i80-system 16-bit interface	DB[17:10], DB[8:1]
0	0	1	1	i80-system 8-bit interface	DB[17:10]
0	1	0	ID	Serial Peripheral Interface (SPI)	SDI, SDO,SCL,nCS
0	1	1	0	3-wire 9-bit serial interface	nCS, SCL, SDA
0	1	1	1	4-wire 8-bit serial interface	nCS, SCL, SDA, RS (D/CX)
1	0	0	0	M68-system18-bit interface	DB[17:0]
1	0	0	1	M68-system 9-bit interface	DB[17:9]
1	0	1	0	i80-system18-bit interface	DB[17:0]
1	0	1	1	i80-system 9-bit interface	DB[17:9]
1	1	*	*	Setting invalid	

7.2.1. 18-bit System Interface

The data format for 18-bit data bus is as following,

Read/Write Register Data format:



Read/Write GRAM Data format:

18-bit System Interface (262K colors)

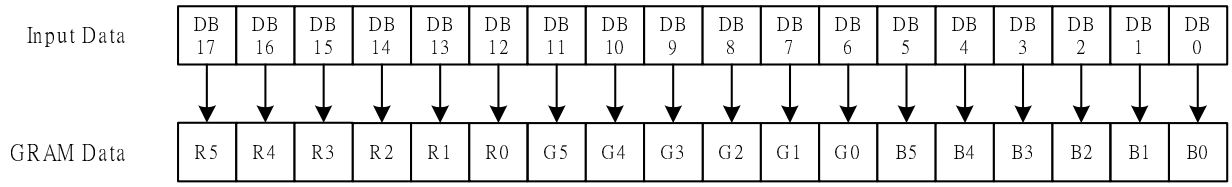
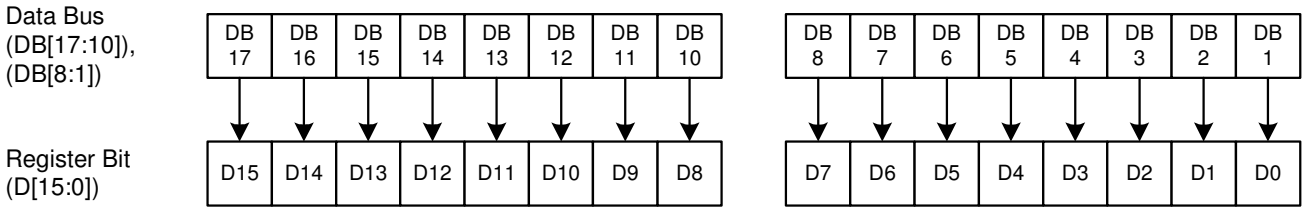


Figure2 18-bit System Interface Data Format

7.2.2. 16-bit System Interface

The data format for 16-bit data bus is as following,

Read/Write Register Data format:



Read/Write GRAM Data format:

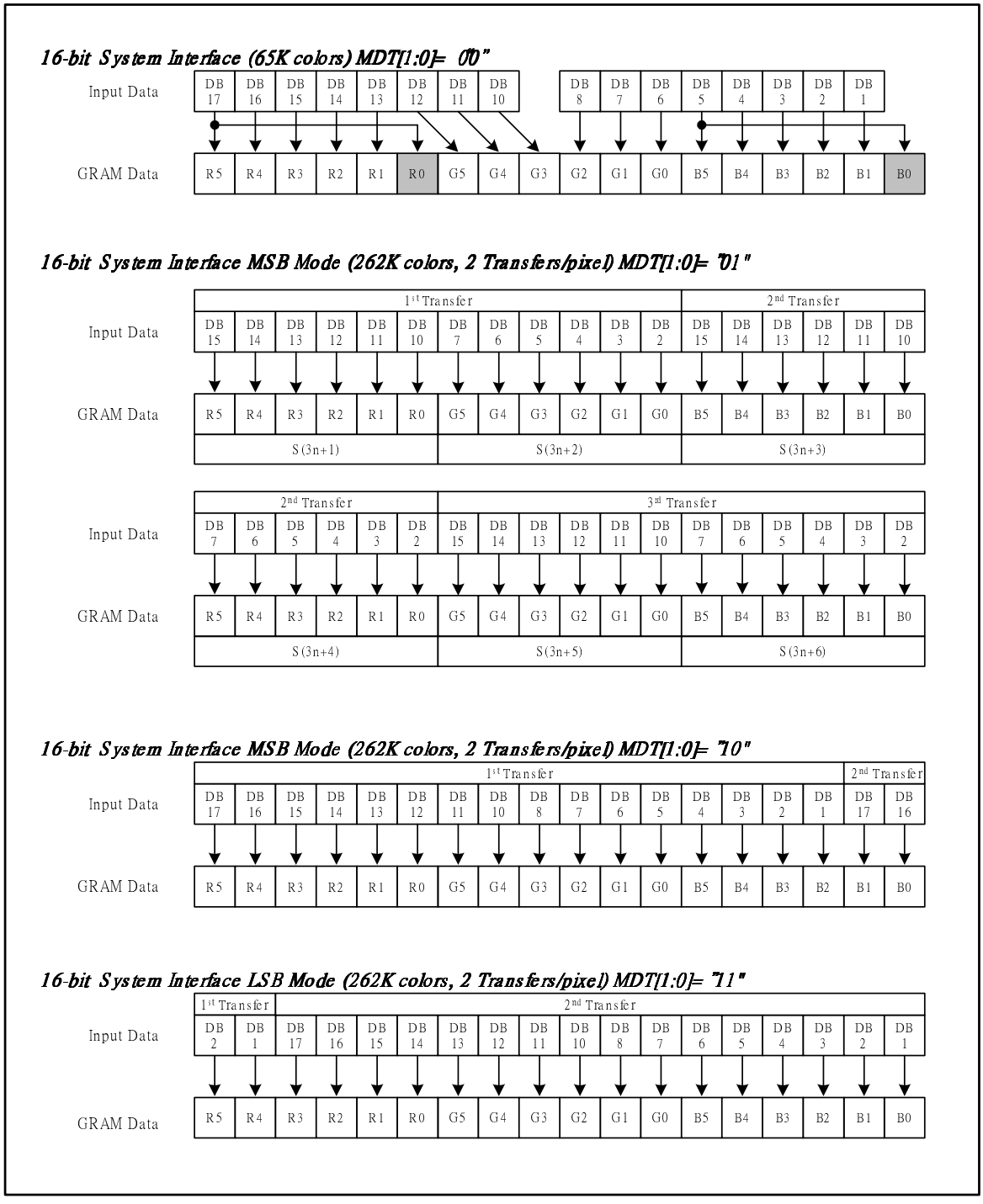


Figure3 16-bit System Interface Data Format

i80 **Read/Write Timing:**

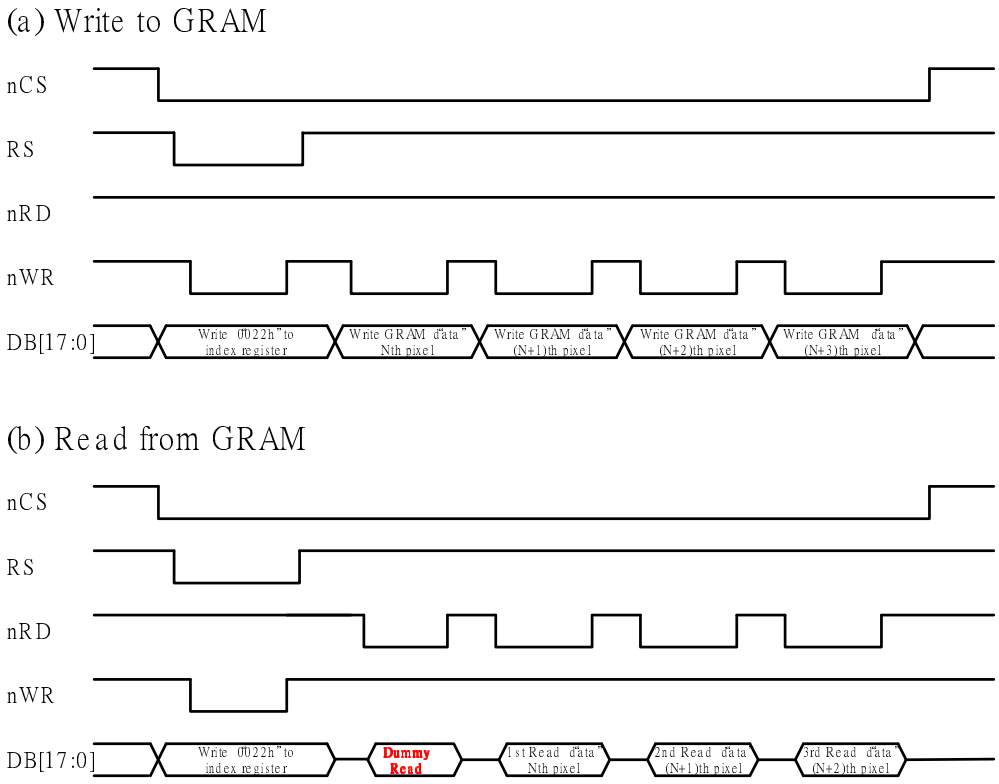


Figure4 i80 16/18-bit System Interface Timing

M68 **Read/Write Timing:**

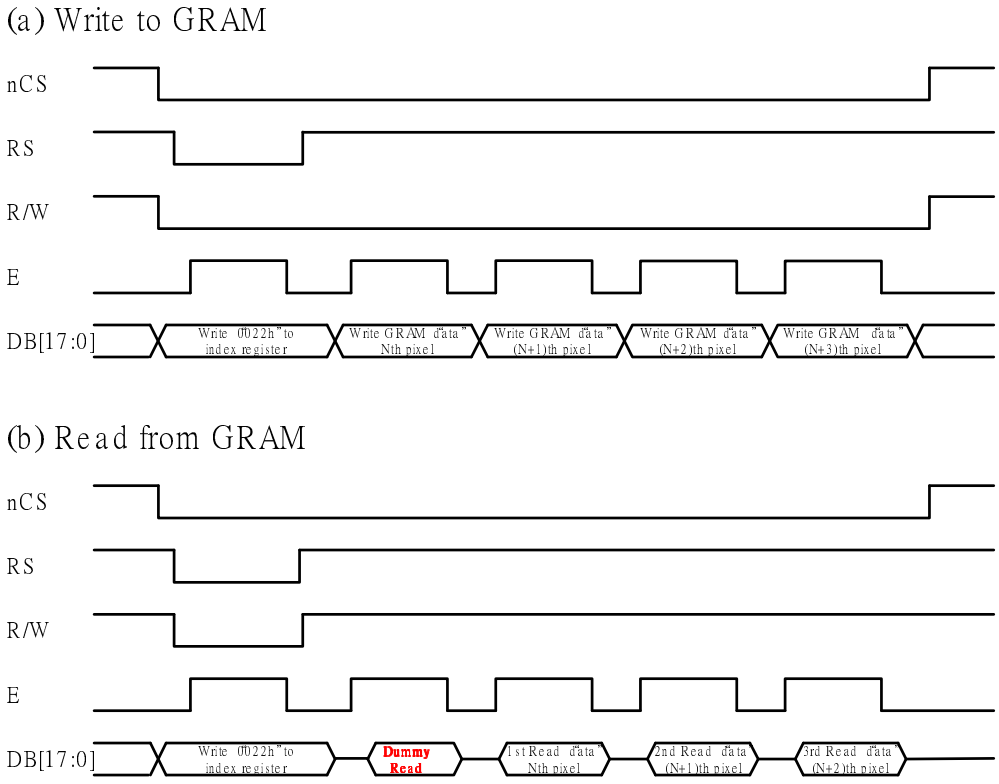
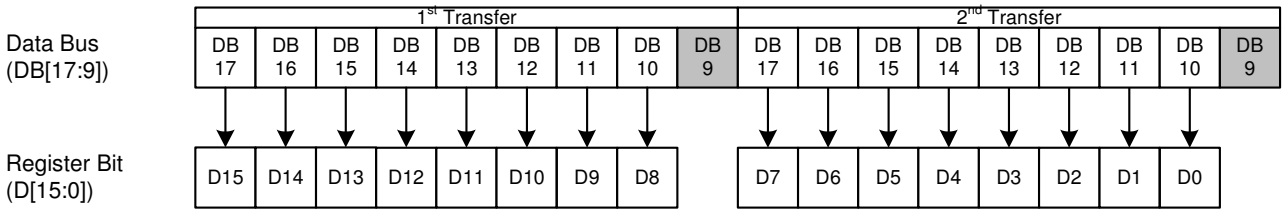


Figure5 M68 16/18-bit System Interface Timing

7.2.3. 9-bit System Interface

The DB17~DB9 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (9 bits) and lower byte, and the upper byte is transferred first. The unused DB[8:0] pins must be tied to ground.

Read/Write Register Data format:



Read/Write GRAM Data format:

9-bit System Interface (262K colors)

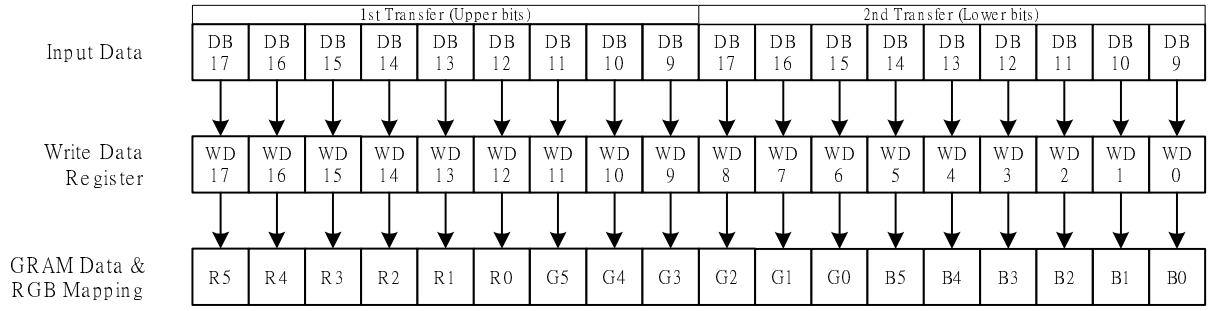
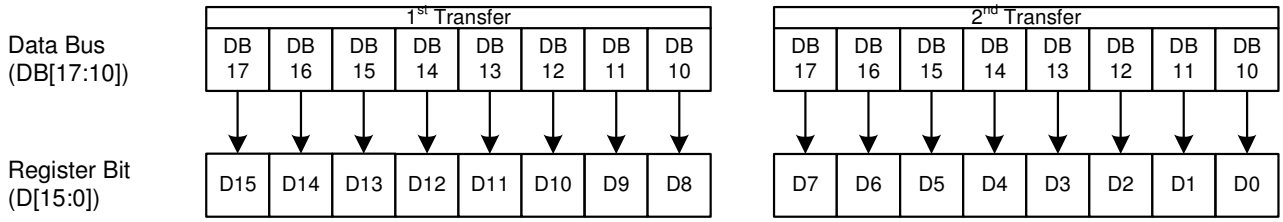


Figure6 9-bit System Interface Data Format

7.2.4. 8-bit System Interface

The DB17~DB10 pins are used to transfer the data. When writing the 16-bit register, the data is divided into upper byte (8 bits and LSB is not used) lower byte and the upper byte is transferred first. The display data is also divided in upper byte (8 bits) and lower byte, and the upper byte is transferred first. The written data is expanded into 18 bits internally (see the figure below) and then written into GRAM. The unused DB[9:0] pins must be tied to ground.

Read/Write Register Data format:



Read/Write GRAM Data format:

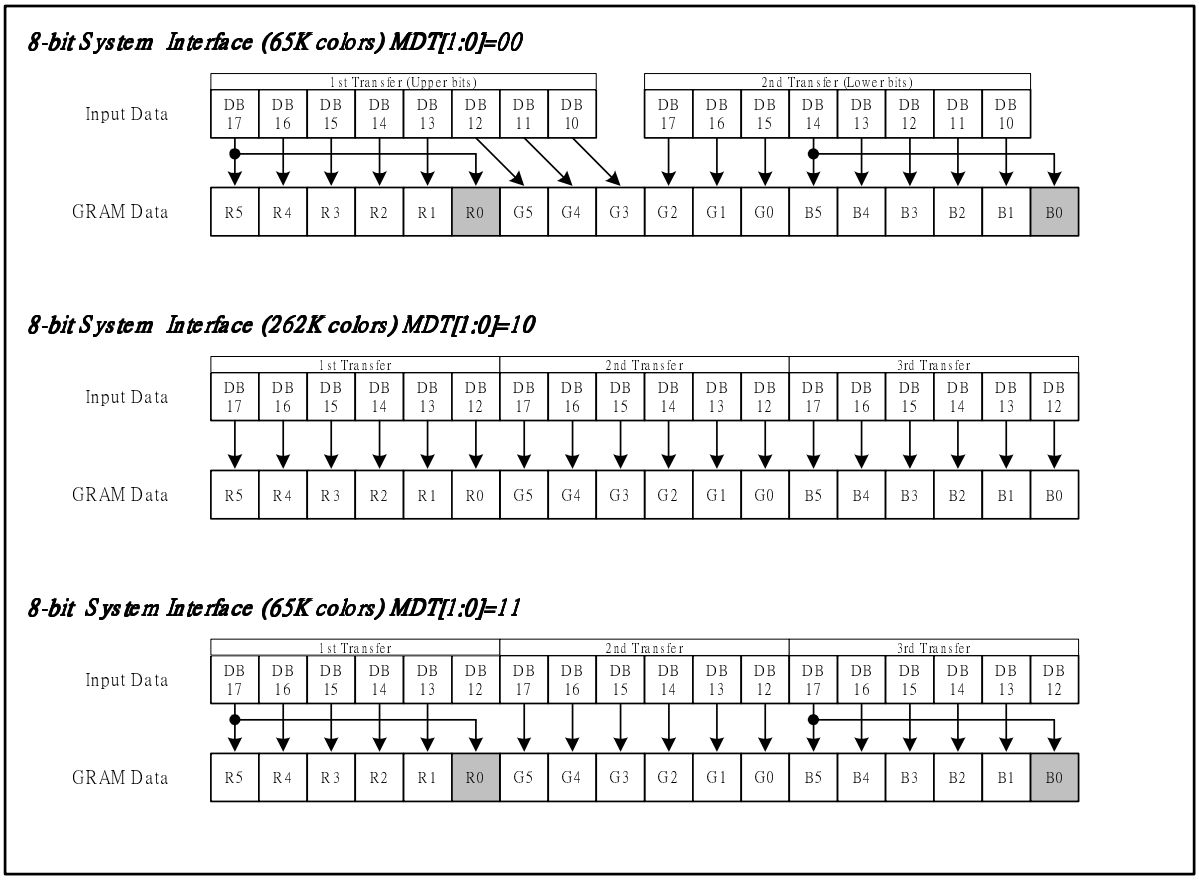


Figure7 8-bit System Interface Data Format

Data transfer synchronization in 8/9-bit bus interface mode

ILI9225G supports a data transfer synchronization function to reset upper and lower counters which count the transfers umner of upper and lower byte in 8/9-bit interface mode. If a mismatch arises in then numbers of transfers between the upper and lower byte counters due to noise and so on, the “00”h register is written 4 times consecutively to reset the upper and lower counters so that data transfer will restart with a transfer of upper byte. This synchronization function can effectively prevent display error if the upper/lower counters are periodically reset.

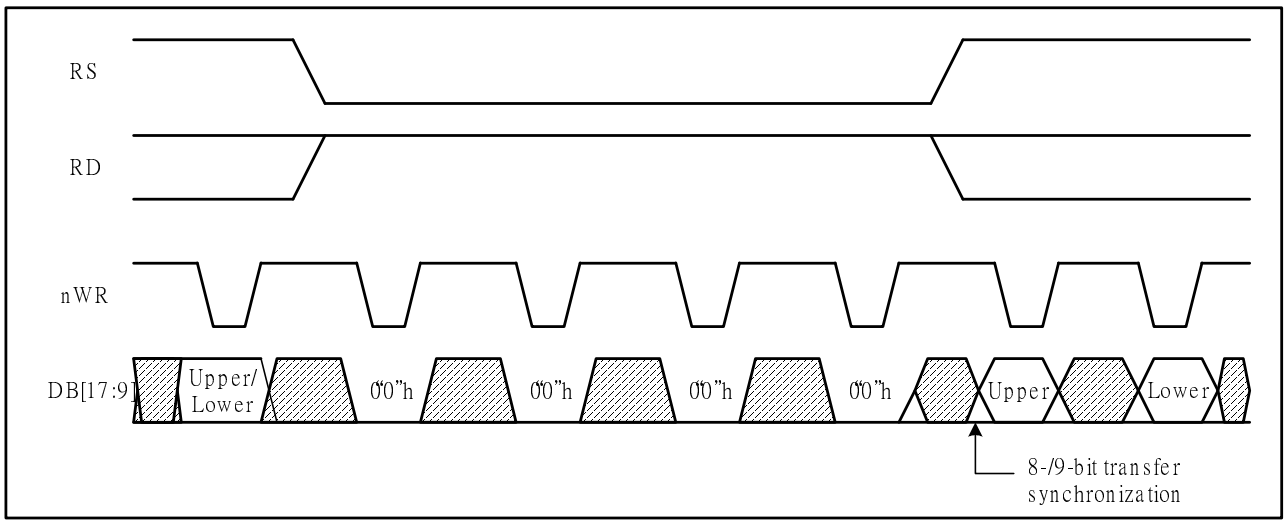


Figure8 Data Transfer Synchronization in 8/9-bit System Interface

7.3. Serial Peripheral Interface (SPI)

7.3.1. 24-bit 4 wires Serial Peripherial Interface

The Serial Peripheral Interface (SPI) is selected by setting the IM[3:0] pins as “010x” level. The chip select pin (nCS), the serial transfer clock pin (SCL), the serial data input pin (SDI) and the serial data output pin (SDO) are used in SPI mode. The ID pin sets the least significant bit of the identification code.The DB[17:0] pins, which are not used, must be tied to ground.

The SPI interface operation enables from the falling edge of nCS and ends of data transfer on the rising edge of nCS. The start byte is transferred to start the SPI interface and the read/write operation and RS information are also included in the start byte. When the start byte is matched, the subsequent data is received by ILI9225G.

The seventh bit of start byte is RS bit. When RS = “0”, either index write operation or status read operation is executed. When RS = “1”, either register write operation or RAM read/write operation is executed. The eighth bit of the start byte is used to select either read or write operation (R/W bit). Data is written when the R/W bit is “0” and read back when the R/W bit is “1”.

After receiving the start byte, ILI9225G starts to transfer or receive the data in unit of byte and the data transfer starts from the MSB bit. All the registers of the ILI9225G are 16-bit format and receive the first and the second byte datat as the upper and the lower eight bits of the 16-bit register respectively. In SPI mode, 5 bytes dummy read is necessary and the valid data starts from 6th byte of read back data.

Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID	1/0	1/0

Note: ID bit is selected by setting the IM0/ID pin.

RS and R/W Bit Function

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write a register or GRAM data
1	1	Read a register or GRAM data

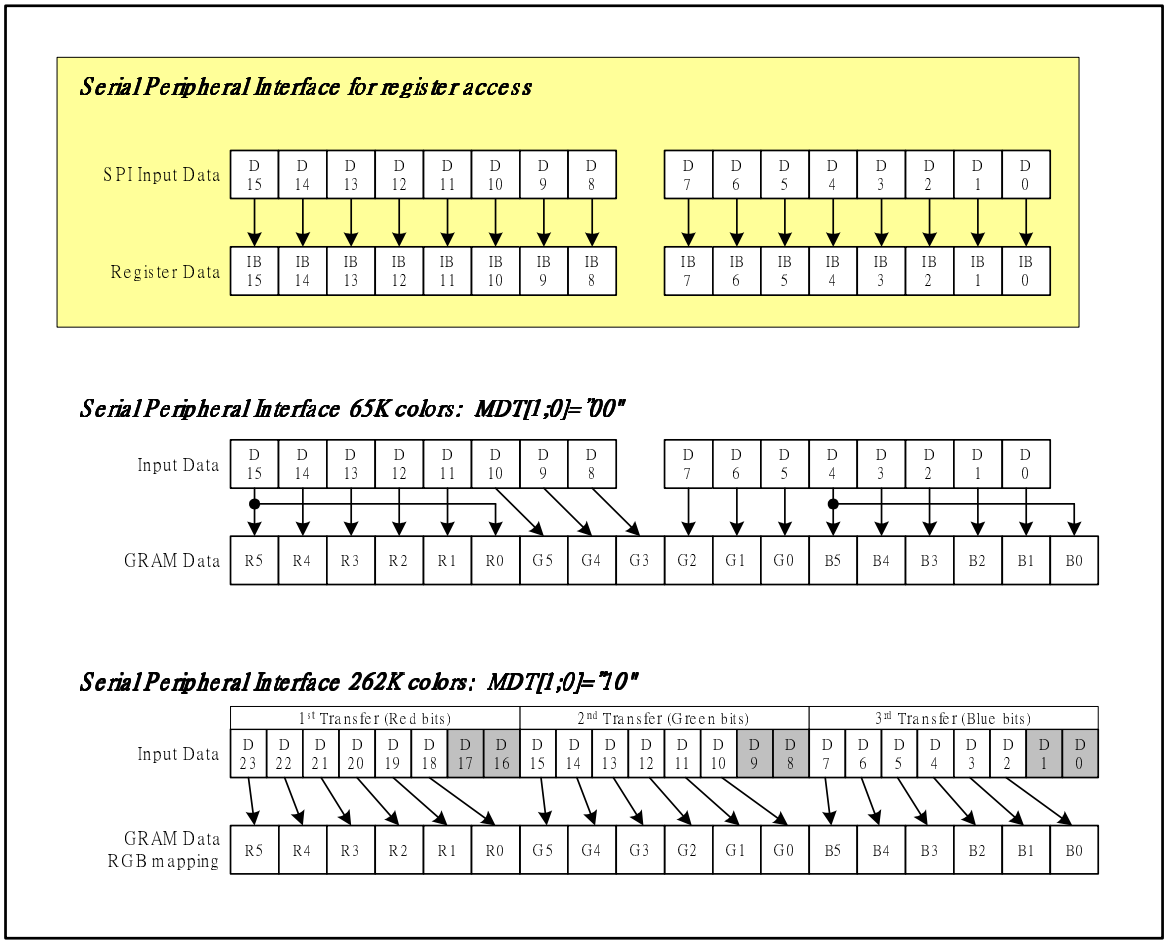
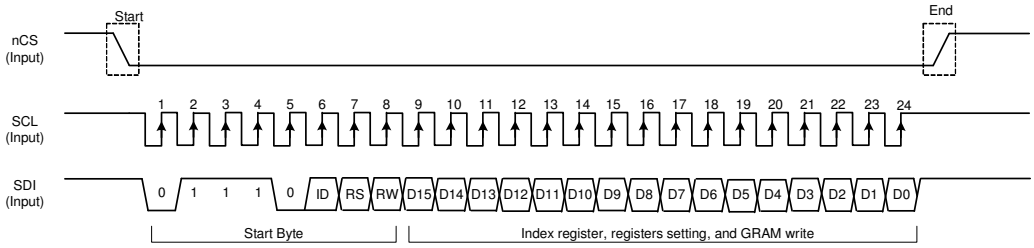
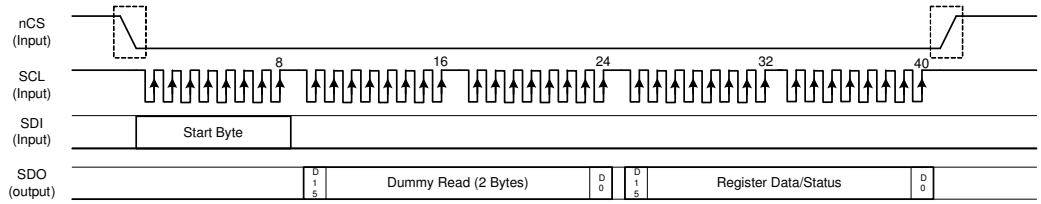


Figure9 Data Format of SPI Interface

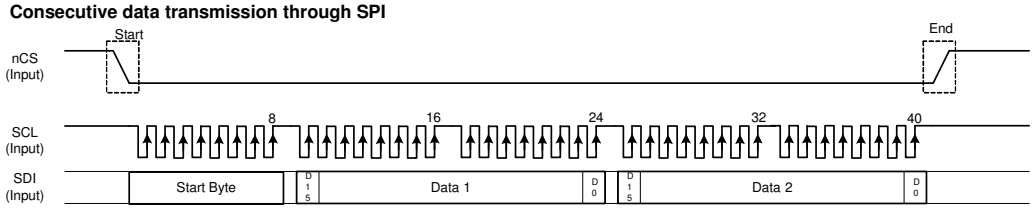
Basic data transmission through SPI



Status/registers read transmission



Consecutive data transmission through SPI



Note: The first byte after the start byte is always the upper eight bits .

GRAM data read transmission, MDT[1:0]= "00"

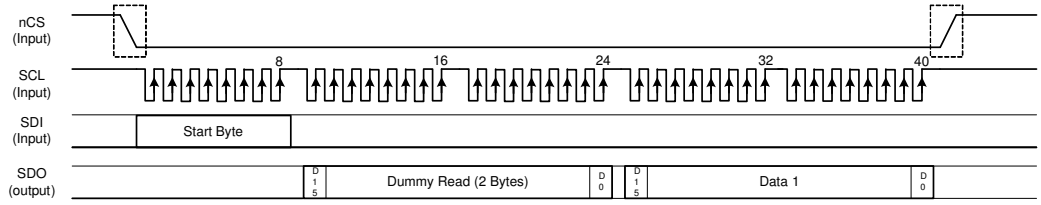


Figure10 Data transmission through SPI, 65 Color

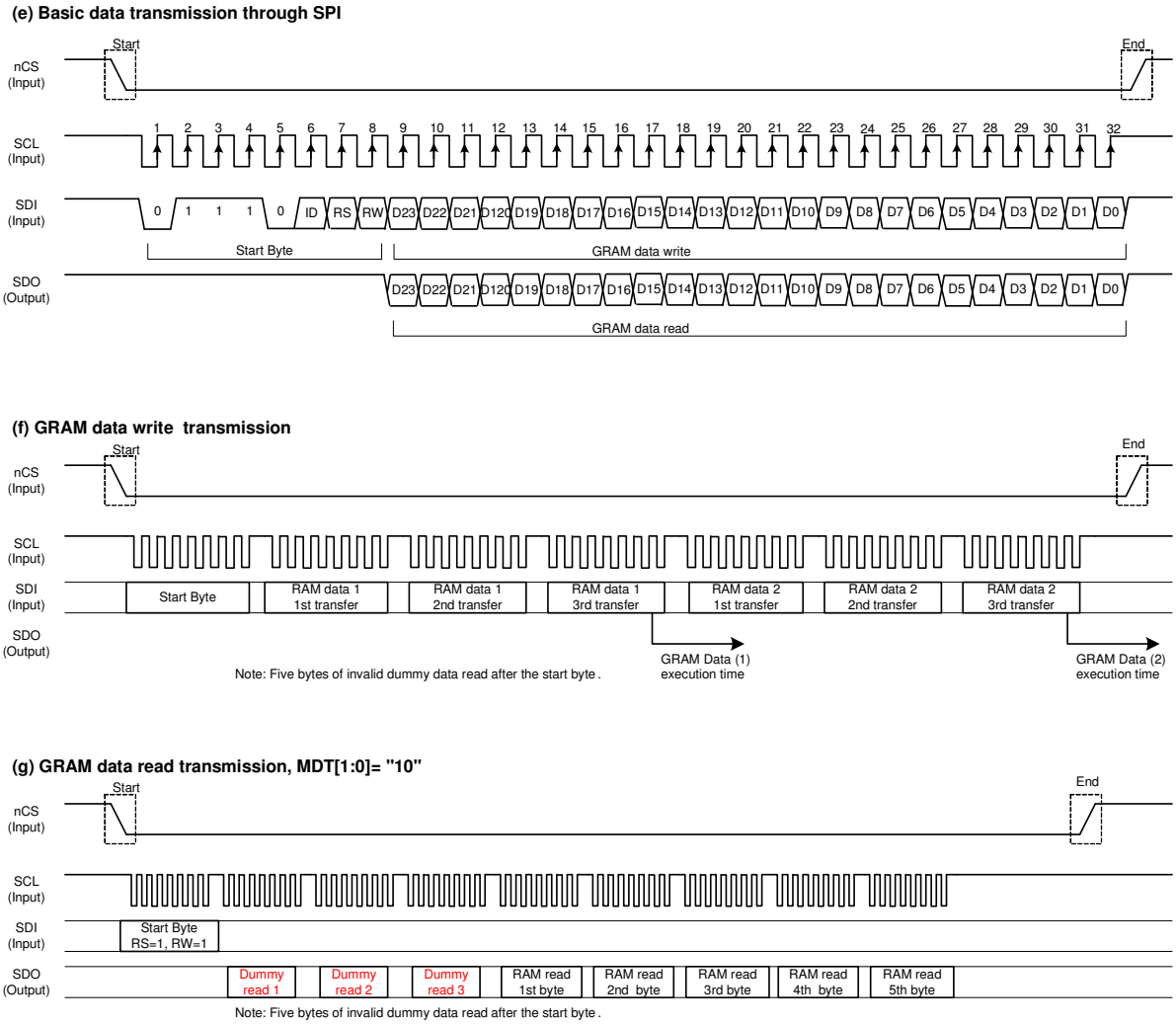


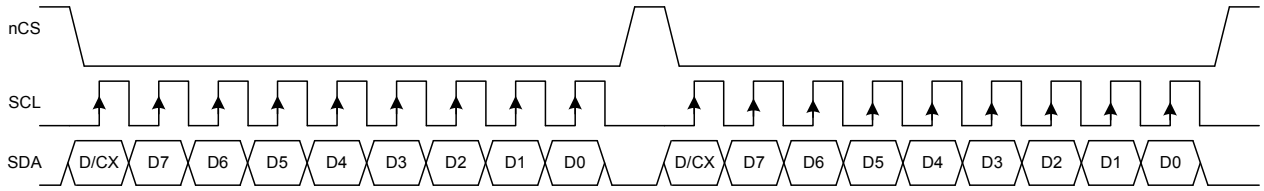
Figure11 Data transmission through SPI, 262K Color

7.3.2. 3-wire 9-bit Serial Interface

This SPI mode uses a 3-wire 9-bit serial interface. The chip-select **nCS** (active low) enables and disables the serial interface. **SCL** is the serial data clock and **SDA** is serial data.

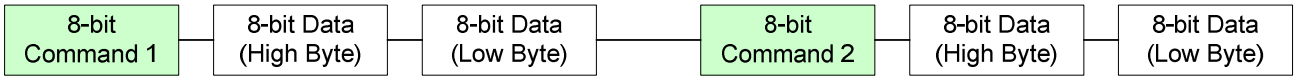
Serial data must be input to **SDA** in the sequence D/CX, D7 to D0. The ILI9225G reads the data at the rising edge of **SCL** signal. The first bit of serial data D/CX is data/command flag. When D/CX = "1", D7 to D0 bits are display RAM data or command parameters. When D/CX = "0" D7 to D0 bits are commands.

Register Write Mode:



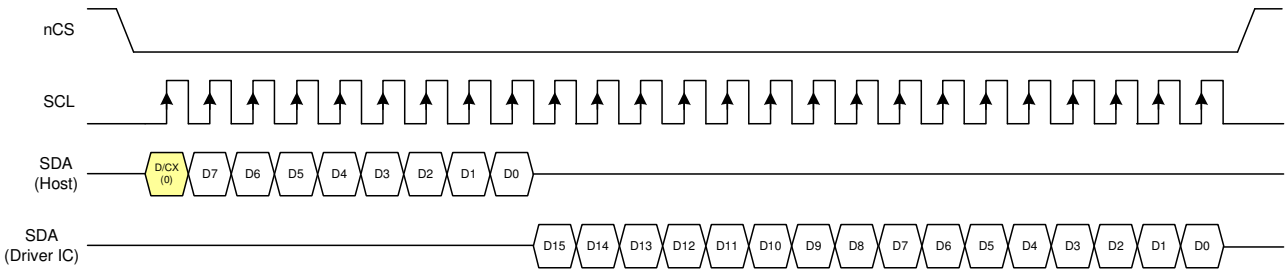
D/CX=0: Register Index (command).

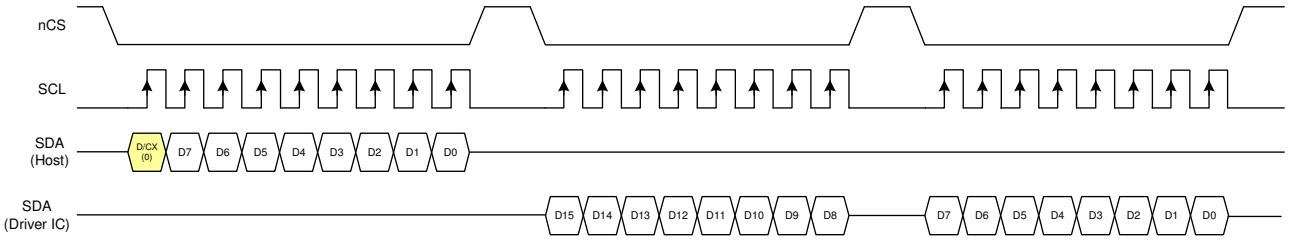
D/CX: register data or GRAM data.



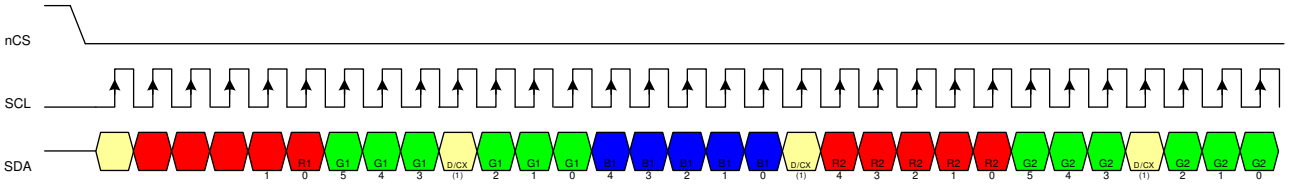
Register Read Mode:

When users need to read back the register or GRAM data, the register R66h must be set as "1" first, and then write the register index to read back the register or GRAM data. The following timing diagrams show examples to read back the register data.

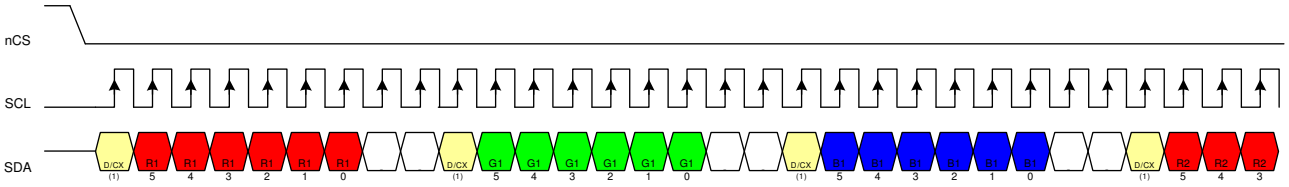




Serial Data Transfer Interface (65K colors, MDT[1:0]="00")



Serial Data Transfer Interface (262K colors, MDT[1:0]="10")

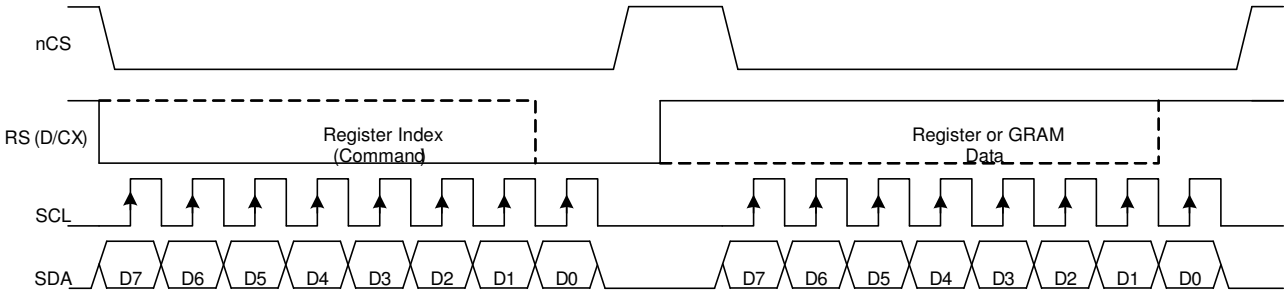


7.3.3. 4-wire 8-bit Serial Interface

This SPI mode uses a 4-wire 9-bit serial interface. The chip-select **nCS** (active low) enables and disables the serial interface. **D/CX** is the command or data select signal, **SCL** is the serial data clock and **SDA** is serial data.

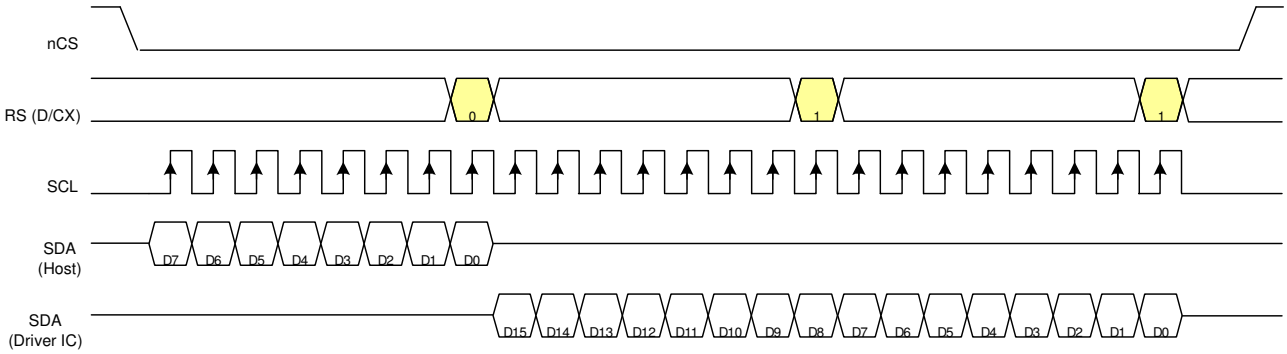
Serial data must be input to **SDA** in the sequence D7 to D0. The ILI9225G reads the data at the rising edge of **SCL** signal. The **D/CX** signal indicates data/command. When D/CX = "1", D7 to D0 bits are display RAM data or command parameters. When D/CX = "0" D7 to D0 bits are commands.

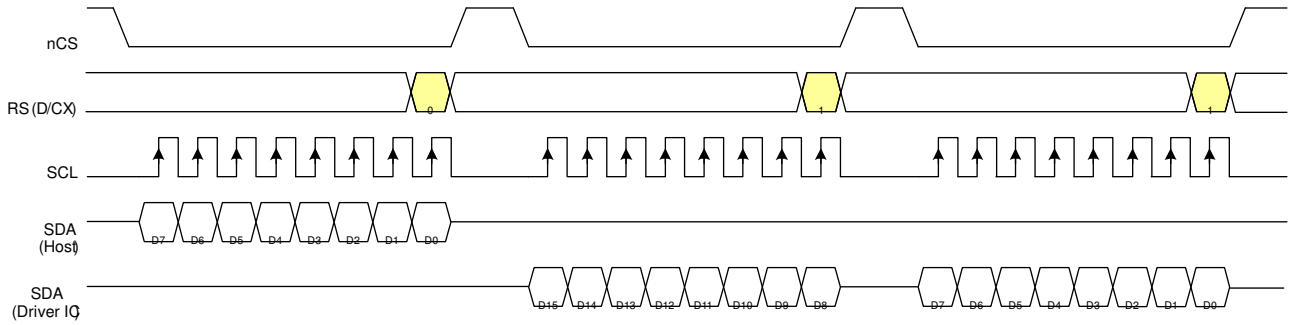
Register Write Mode:



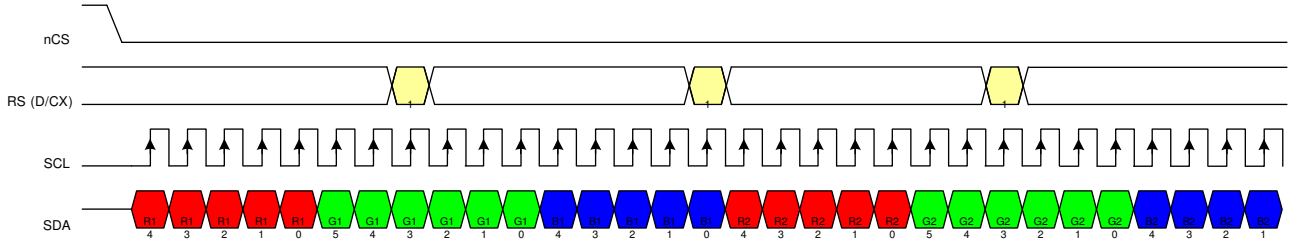
Register Read Mode:

When users need to read back the register or GRAM data, the register R66h must be set as "1" first, and then write the register index to read back the register or GRAM data. The following timing diagrams show examples to read back the register data.

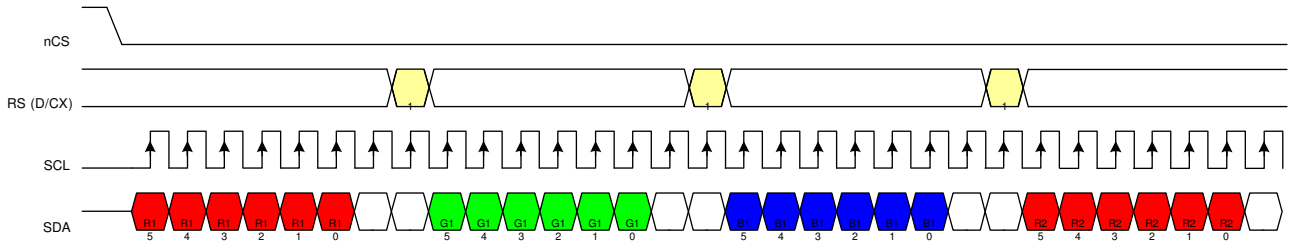




Serial Data Transfer Interface (65K colors, MDT[1:0]="00")

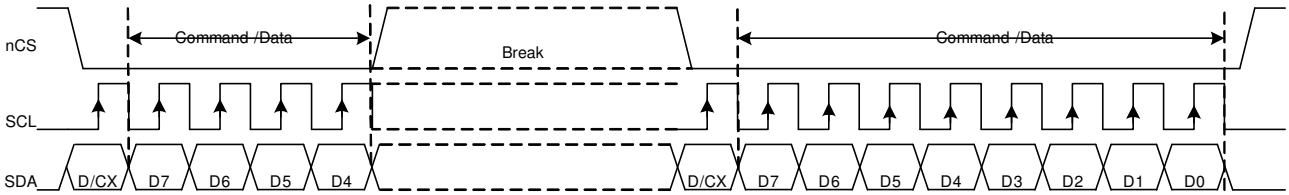


Serial Data Transfer Interface (262K colors, MDT[1:0]="10")



7.3.4. Data Transfer Recovery

If there is a break in data transmission while transferring a command or GRAM data or multiple register data, before Bit D0 of the byte has been completed, then the ILI9225G will reject the previous bits and have reset the interface such that it will be ready to receive the same byte retransmitted when the chip select line (nCS) is next activated. See the following example:



If the 2 parameter of command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred isrejected. The interface is ready to receive next byte as show below.

Note: Break can be e.g. another command or noise pulse.

7.4. RGB Input Interface

The RGB Interface mode is available for ILI9225G and the interface is selected by setting the RIM[1:0] bits as following table.

RIM1	RIM0	RGB Interface	DB pins
0	0	18-bit RGB Interface	DB[17:0]
0	1	16-bit RGB Interface	DB[17:13], DB[11:1]
1	0	6-bit RGB Interface	DB[17:12]
1	1	Setting prohibited	

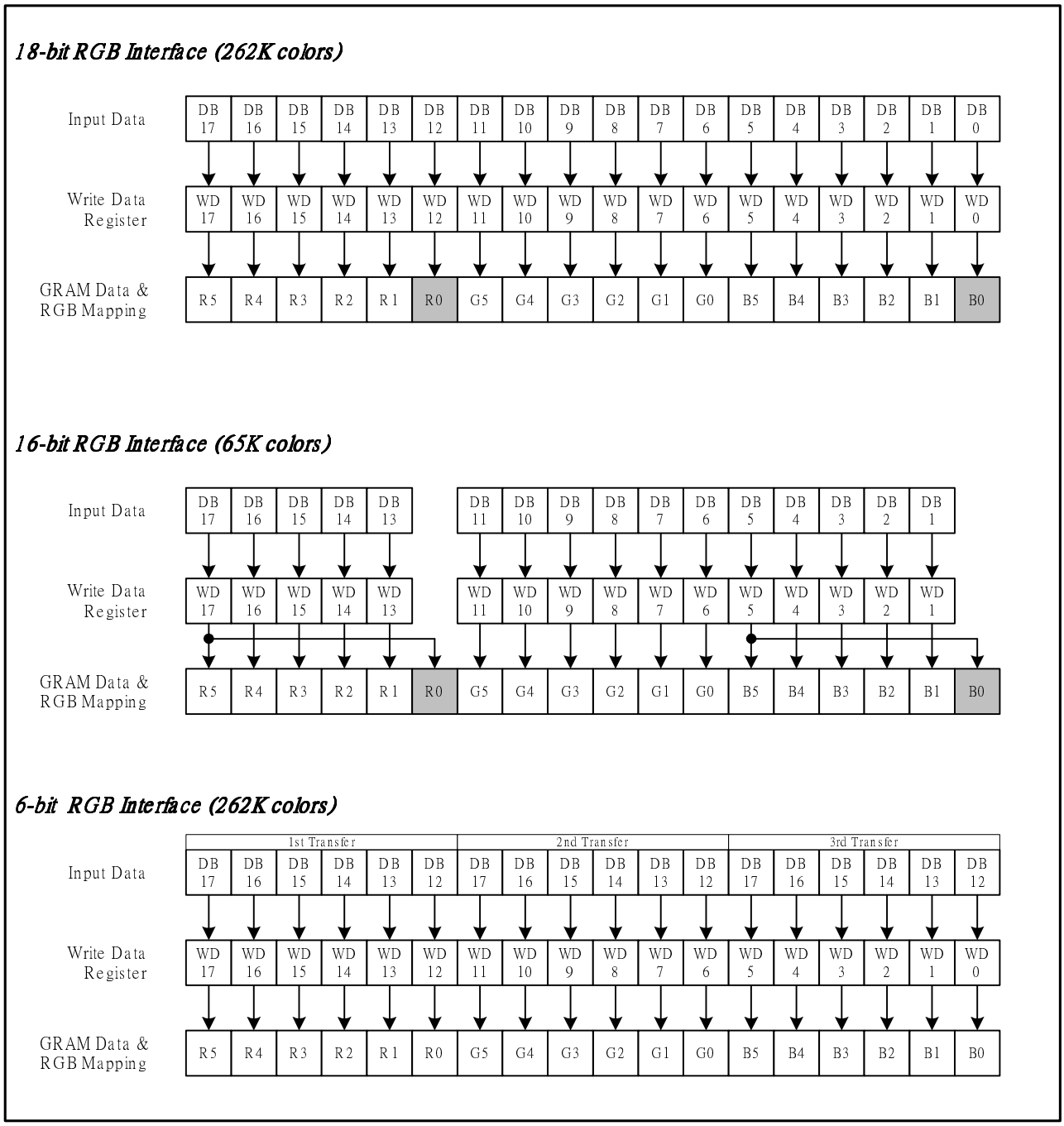


Figure12 RGB Interface Data Format

7.4.1. RGB Interface

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The RGB interface transfers the updated data to GRAM with the high-speed write function and the update area is defined by the window address function. The back porch and front porch are used to set the RGB interface timing.

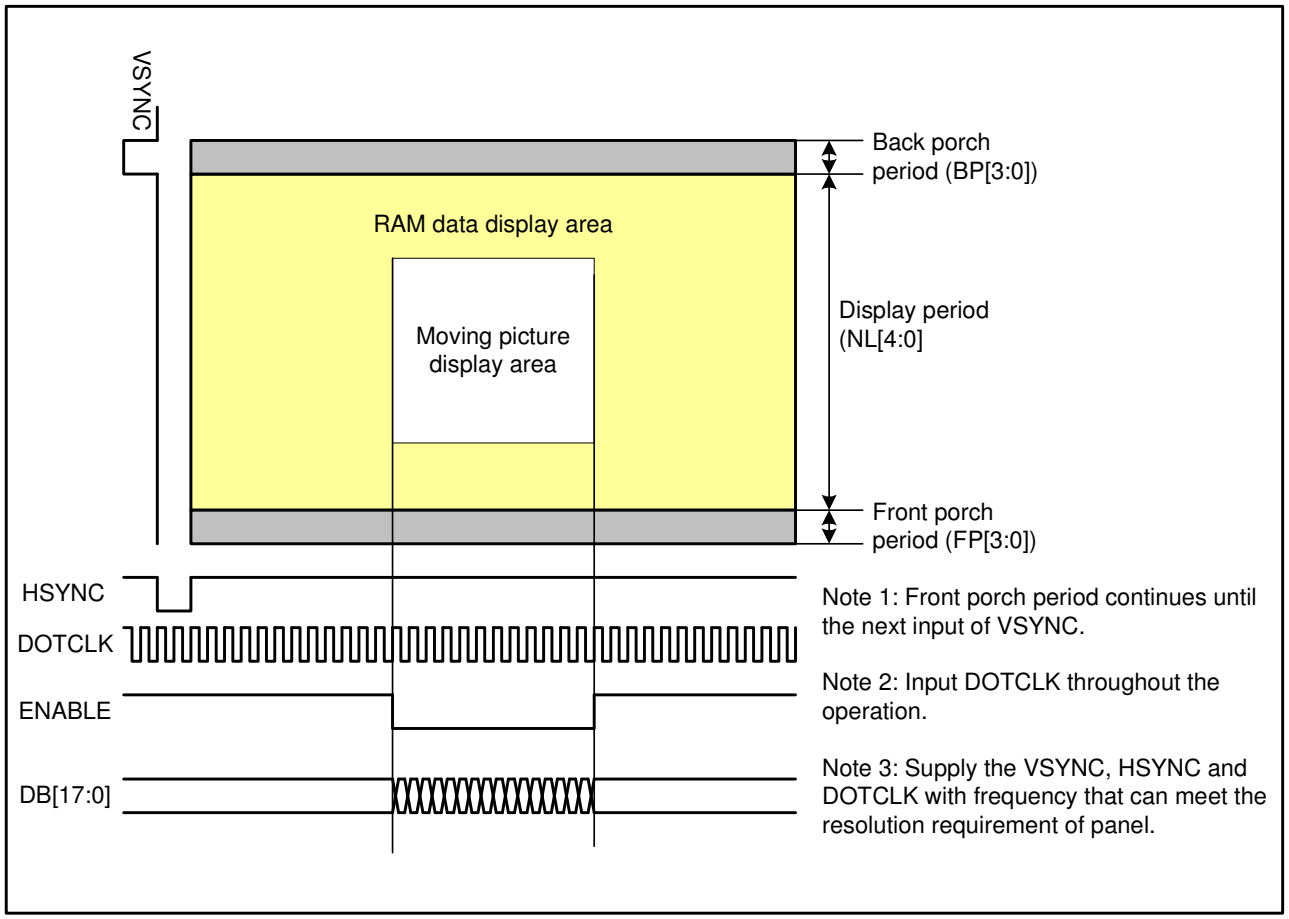


Figure13 GRAM Access Area by RGB Interface

7.4.2. RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as follows.

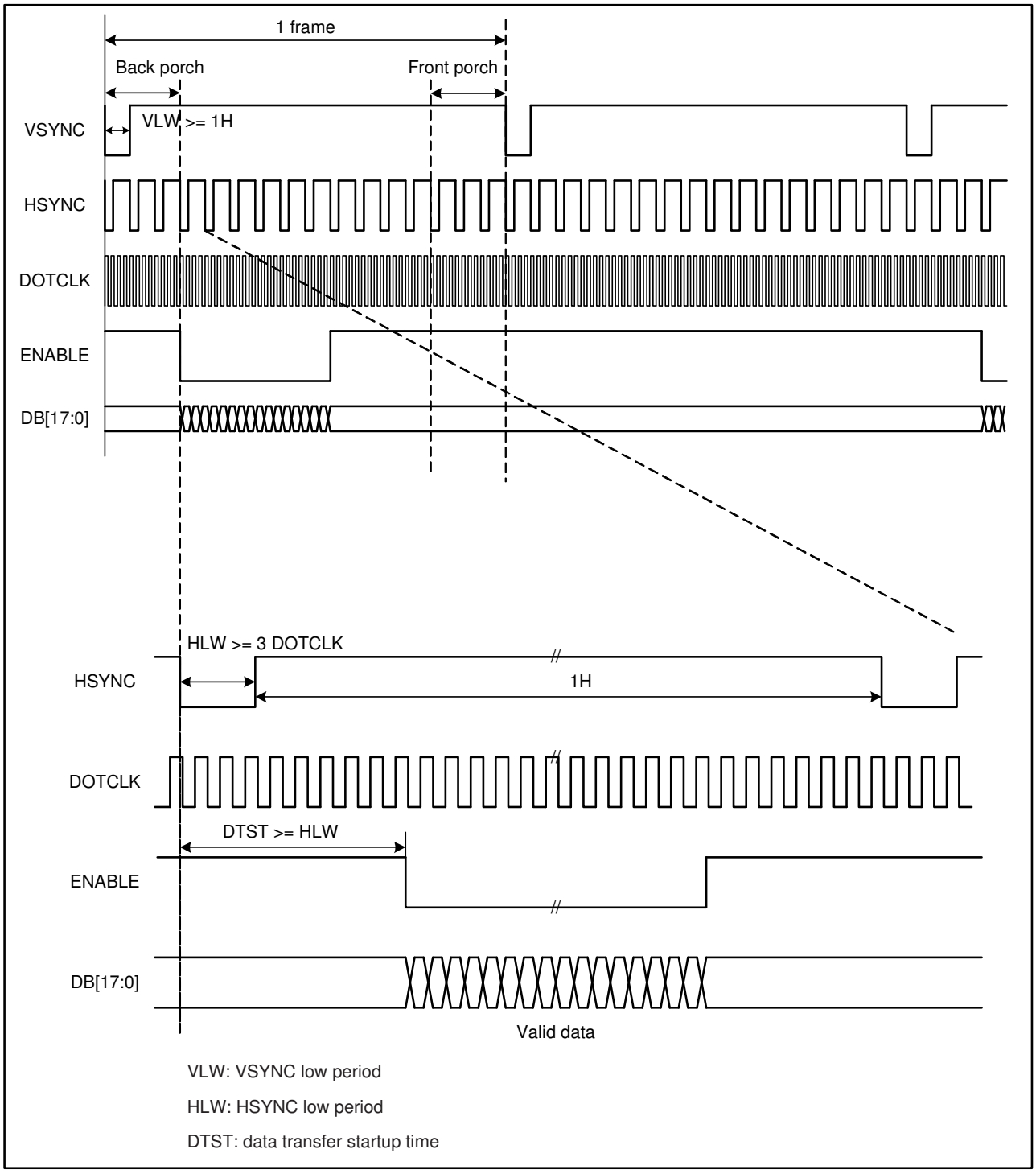


Figure14 Timing Chart of Signals in 18-/16-bit RGB Interface Mode

The timing chart of 6-bit RGB interface mode is shown as follows.

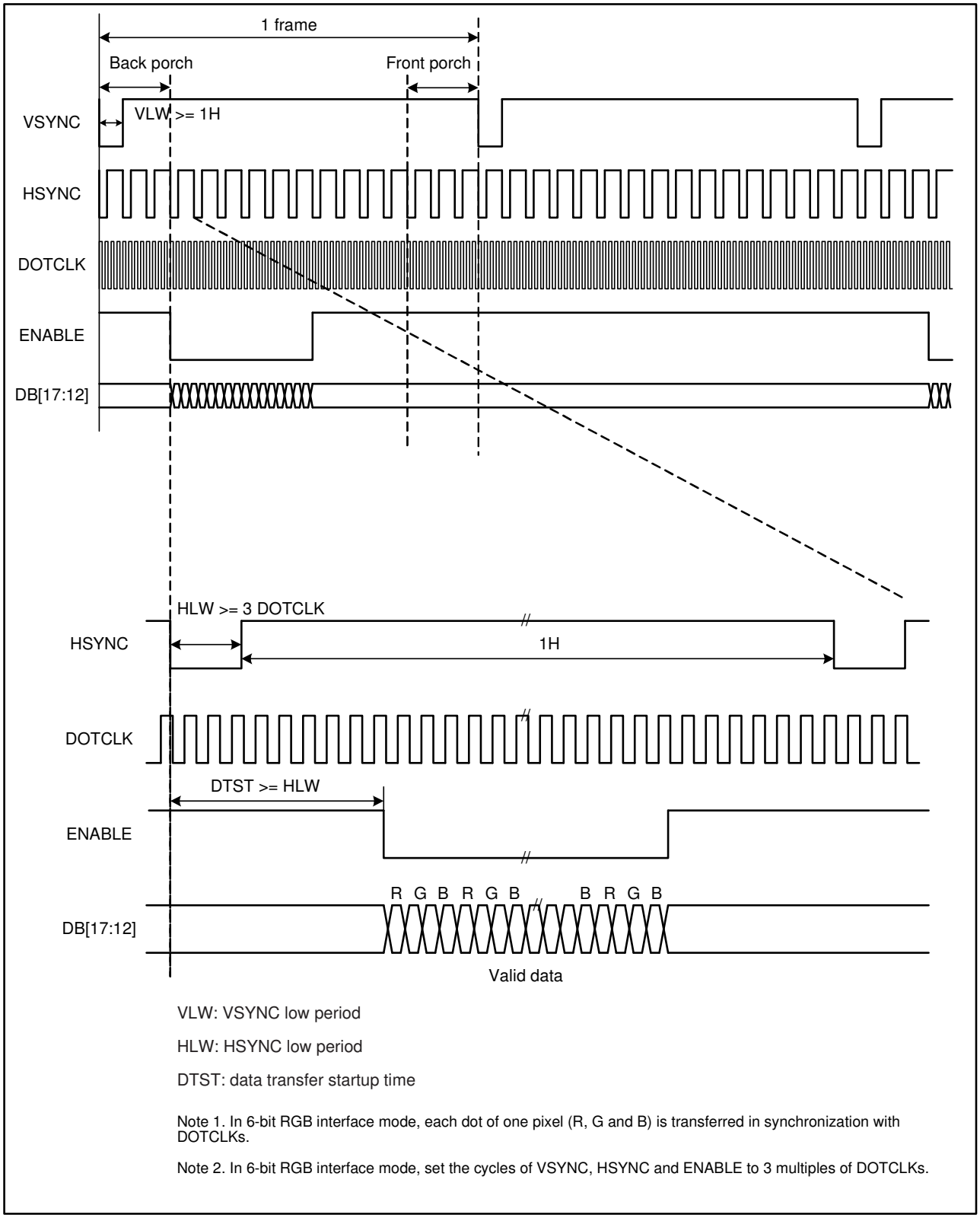


Figure15 Timing chart of signals in 6-bit RGB interface mode

7.4.3. Moving Picture Mode

ILI9225G has the RGB interface to display moving picture and incorporates GRAM to store display data, which has following merits in displaying a moving picture.

- The window address function defined the update area of GRAM.
- Only the moving picture area of GRAM is updated.
- When display the moving picture in RGB interface mode, the DB[17:0] can be switched as system interface to update still picture area and registers, such as icons.

RAM access via a system interface in RGB-I/F mode

ILI9225G allows GRAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal GRAM in synchronization with DOTCLK and ENABLE signals. When write data to the internal GRAM by the system interface, set ENABLE to terminate the RGB interface and switch to the system interface to update the registers (RM = "0") and the still picture of GRAM. When restart RAM access in RGB interface mode, wait one read/write cycle and then set RM = "1" and the index register to R22h to start accessing RAM via the RGB interface. If RAM accesses via two interfaces conflicts, there is no guarantee that data are written to the internal GRAM.

The following figure illustrates the operation of the ILI9225G when displaying a moving picture via the RGB interface and rewriting the still picture RAM area via the system interface.

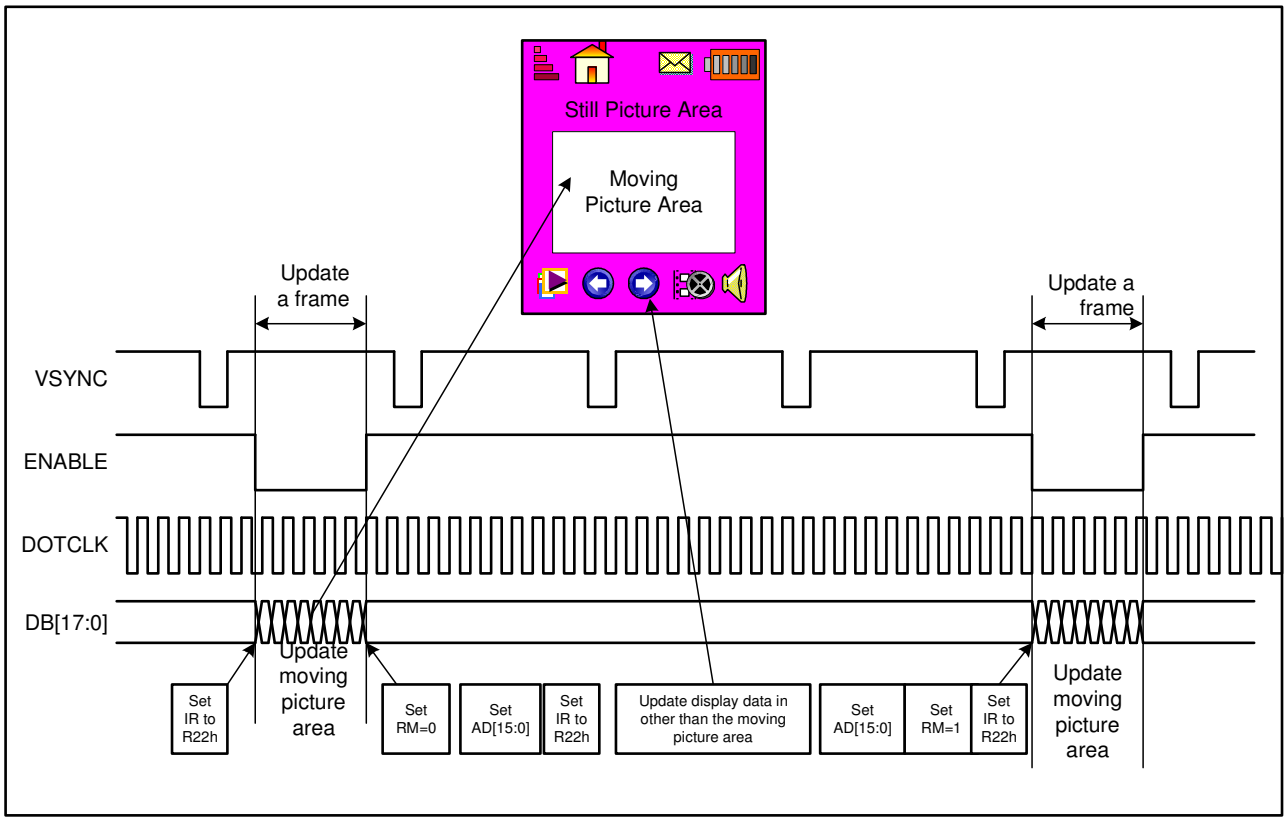
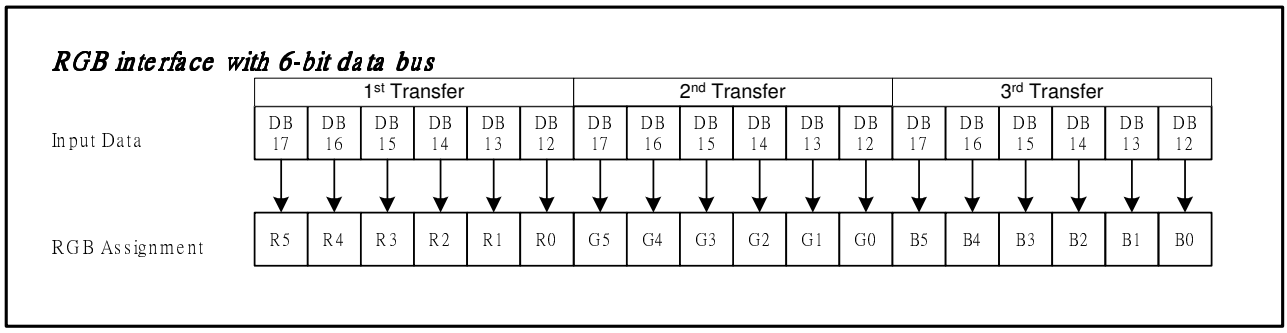


Figure16 Example of update the still and moving picture

7.4.4. 6-bit RGB Interface

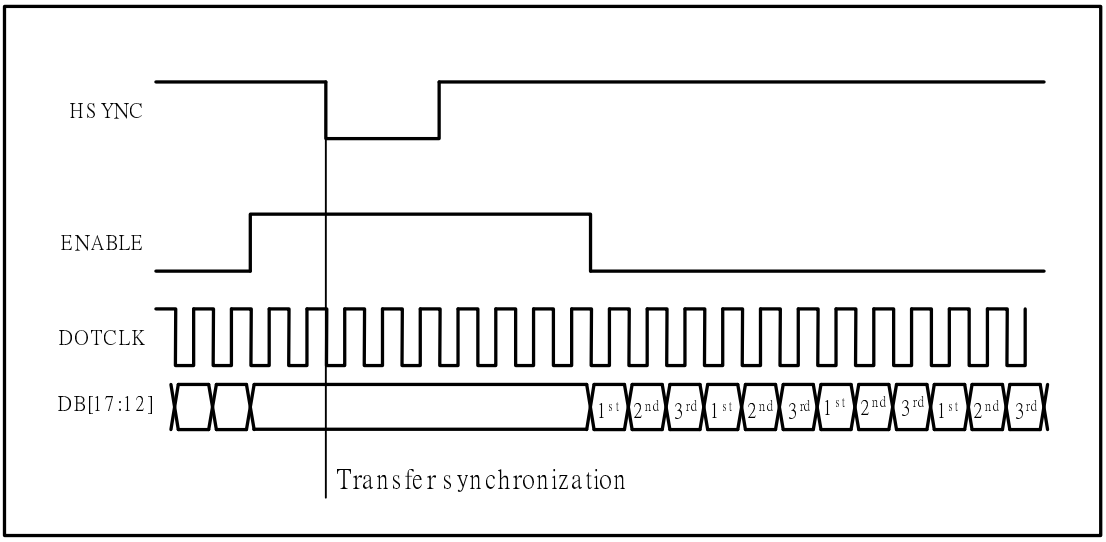
The 6-bit RGB interface is selected by setting the RIM[1:0] bits to “10”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (DB[17:12]) according to the data enable signal (ENABLE). Unused pins (DB[11:0]) must be fixed at ground. Registers can be set by the system interface (i80/M68/SPI).



Data transfer synchronization in 6-bit RGB interface mode

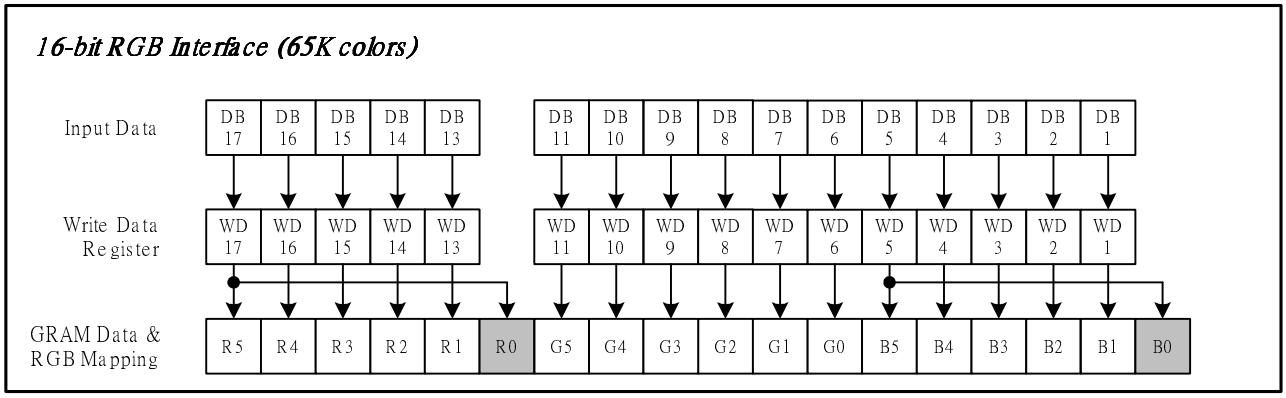
ILI9225G has data transfer counters to count the first, second, third data transfers in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.



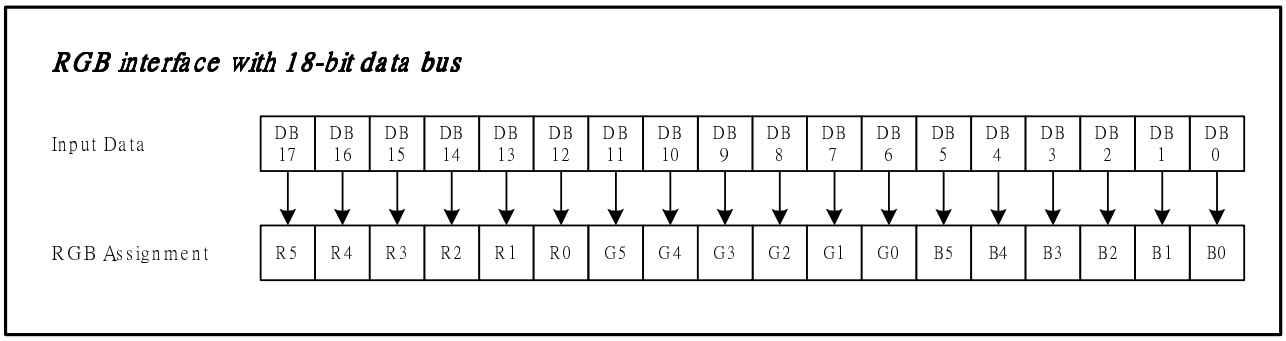
7.4.5. 16-bit RGB Interface

The 16-bit RGB interface is selected by setting the RIM[1:0] bits to “01”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus (DB17-13, DB11-1) according to the data enable signal (ENABLE). Registers are set only via the system interface.



7.4.6. 18-bit RGB Interface

The 18-bit RGB interface is selected by setting the RIM[1:0] bits to “00”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB[17:0]) according to the data enable signal (ENABLE). Registers are set only via the system interface.



Notes in using the RGB Input Interface

1. The following are the functions not available in RGB Input Interface mode.

Function	RGB interface	I80/M68 system interface
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

2. VSYNC, HSYNC, and DOTCLK signals must be supplied throughout a display operation period.
3. The periods set with the NO[1:0] bits (gate output non-overlap period), STD[1:0] bits (source output delay period) and EQ[1:0] bits (equalization period) are not based on the internal clock but based on DOTCLK in

RGB interface mode.

4. In 6-bit RGB interface mode, each of RGB dots is transferred in synchronization with a DOTCLK input. In other words, it takes 3 DOTCLK inputs to transfer one pixel. Be sure to complete data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode.
5. In 6-bit RGB interface mode, data of one pixel, which consists of RGB dots, are transferred in units of 3 DOTCLK. Accordingly, set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC, ENABLE, DB[17:0]) to contain DOTCLK inputs of a multiple of 3 to complete data transfer in units of pixels.
6. When switching from the internal operation mode to the RGB Input Interface mode, or the other way around, follow the sequence below.
7. In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.
8. In RGB interface mode, a RAM address (AD[15:0]) is set in the address counter every frame on the falling edge of VSYNC.

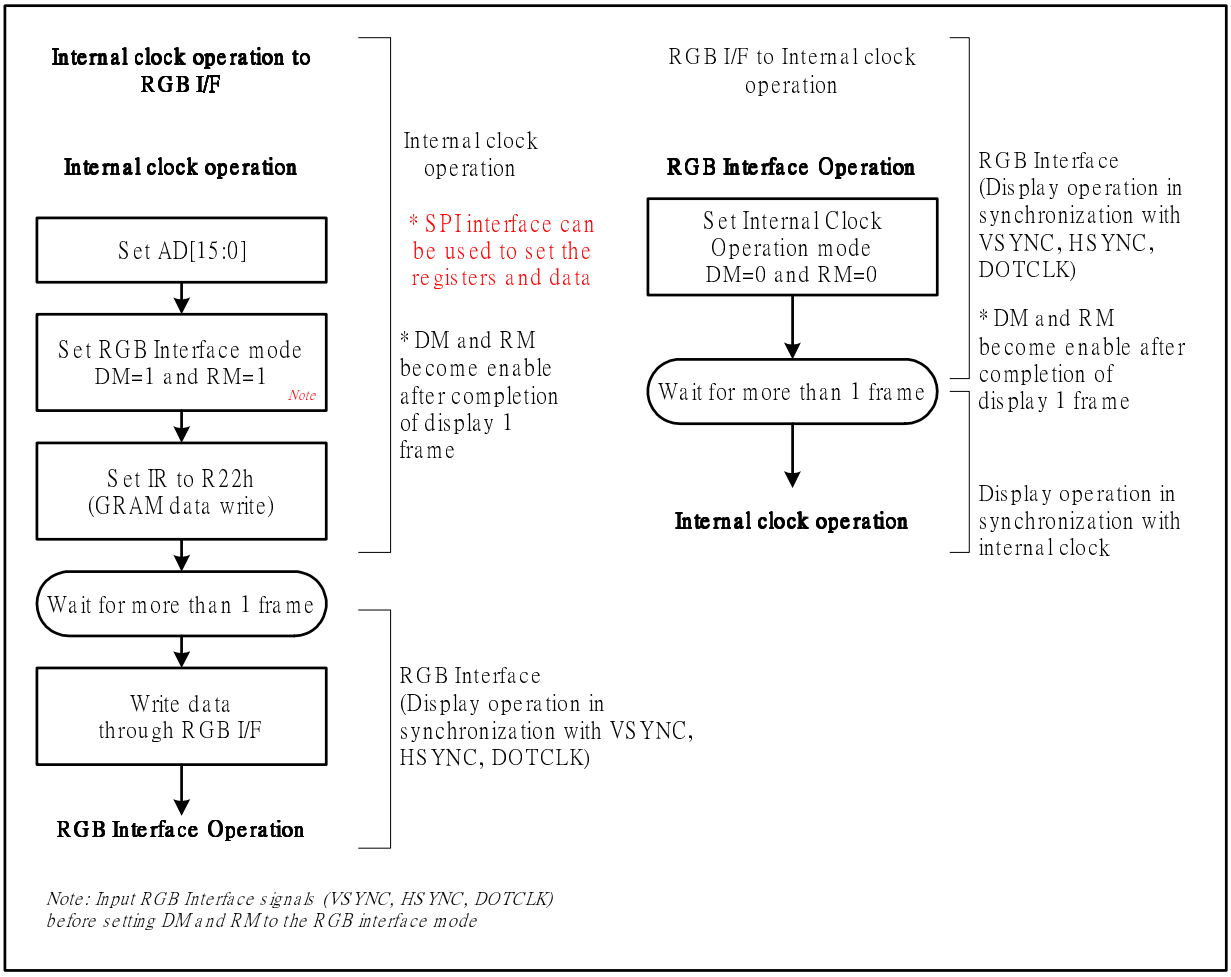


Figure17 Internal clock operation/RGB interface mode switching

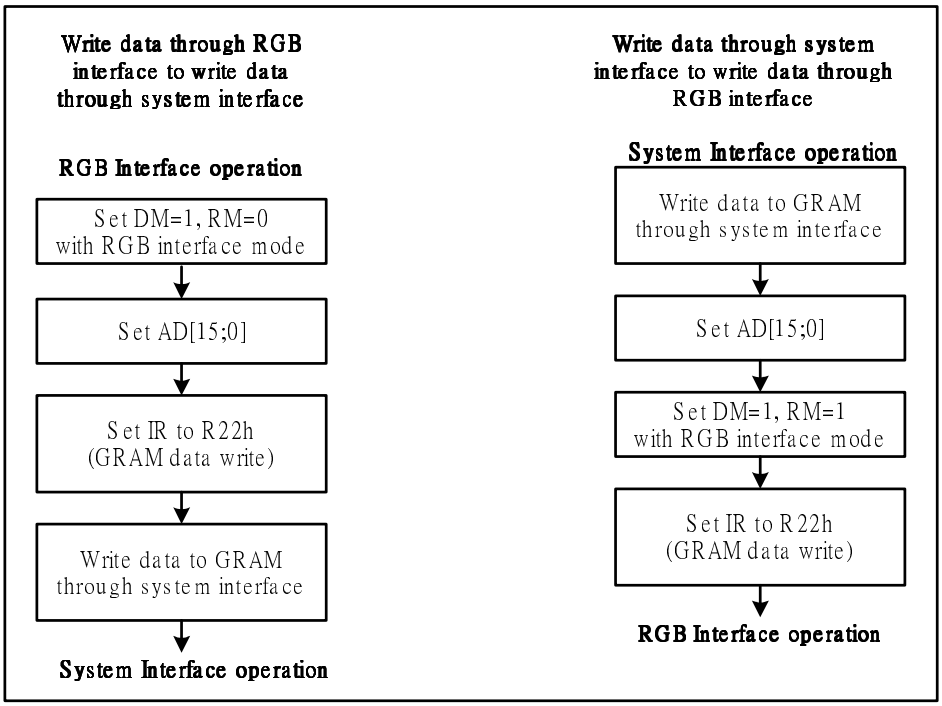


Figure18 GRAM access between system interface and RGB interface

7.5. Interface Timing

The following are diagrams of interfacing timing with LCD panel control signals in internal operation and RGB interface modes.

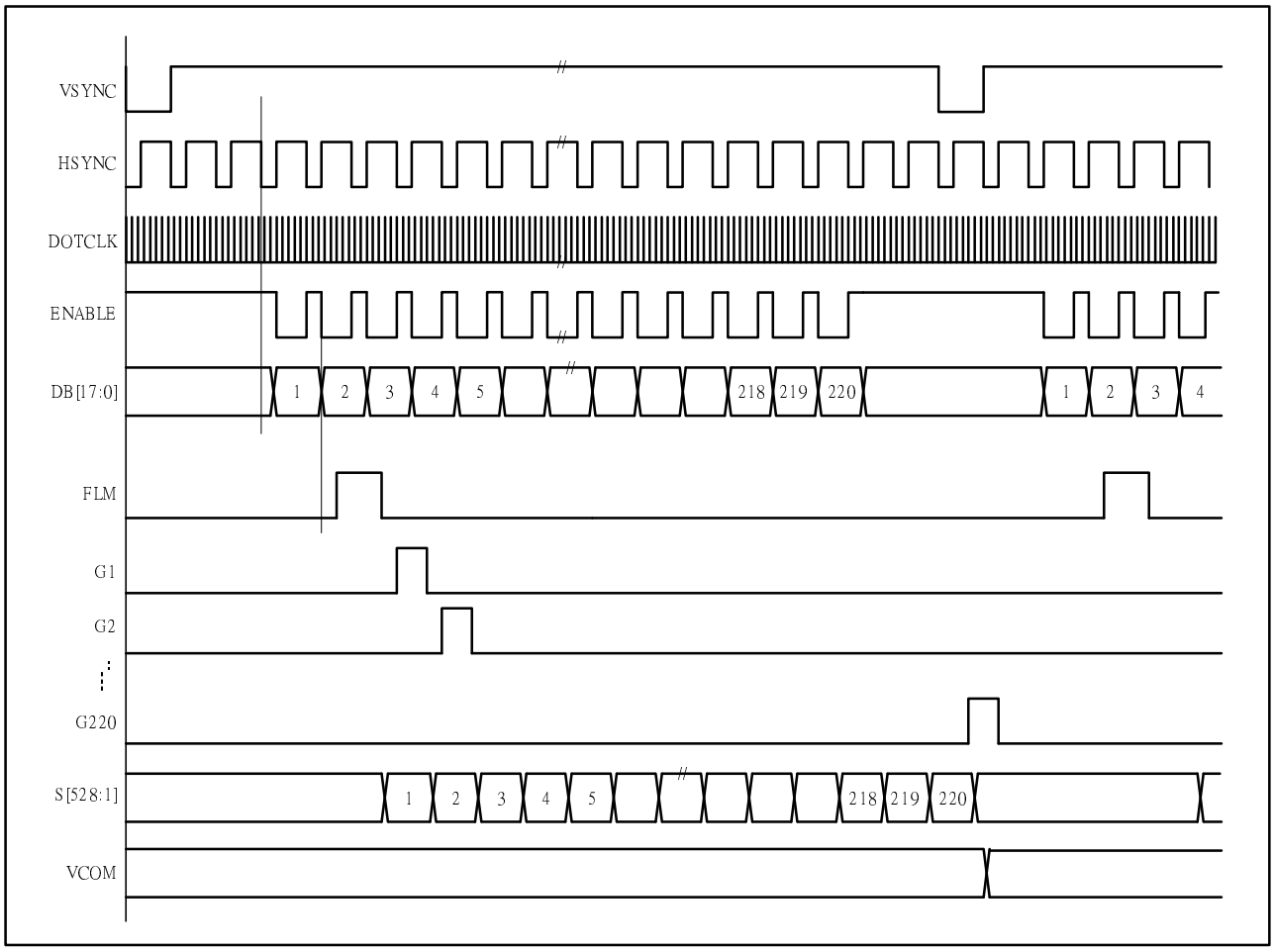


Figure19 Relationship between RGB I/F signals and LCD Driving Signals for Panel

8. Register Descriptions

8.1. Registers Access

ILI9225G adopts 18-bit bus interface architecture for high-performance microprocessor. All the functional blocks of ILI9225G starts to work after receiving the correct instruction from the external microprocessor by the 18-, 16-, 9-, 8-bit interface. The index register (IR) stores the register address to which the instructions and display data will be written. The register selection signal (RS), the read/write signals (nRD/nWR) and data bus D17-0 are used to read/write the instructions and data of ILI9225G. The registers of the ILI9225G are categorized into the following groups.

1. Specify the index of register (IR)
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address (AC)
7. Transfer data to/from the internal GRAM (R22)
8. Internal grayscale γ-correction (R50 ~ R59)

Normally, the display data (GRAM) is most often updated, and in order since the ILI9225G can update internal GRAM address automatically as it writes data to the internal GRAM and minimize data transfer by using the window address function, there are fewer loads on the program in the microprocessor. As the following figure shows, the way of assigning data to the 16 register bits (D[15:0]) varies for each interface. Send registers in accordance with the following data transfer format.

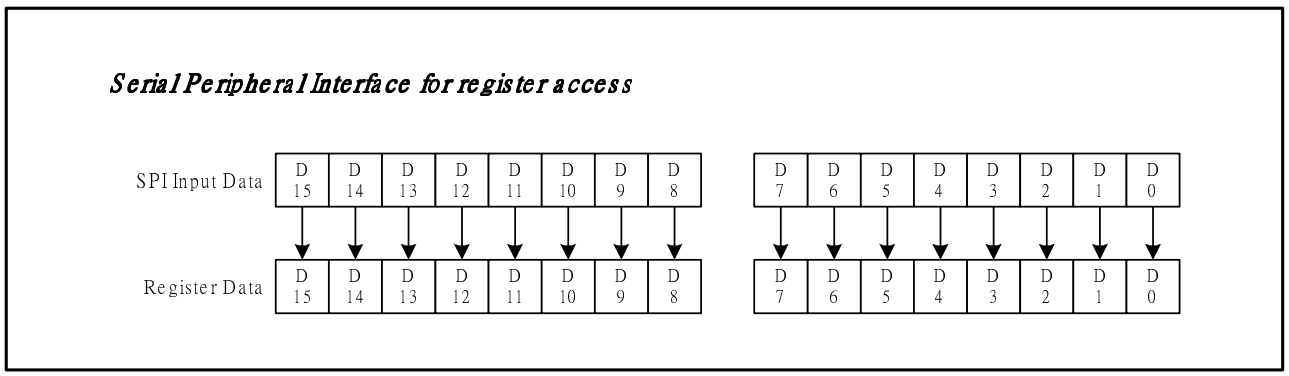


Figure20 Register Setting with Serial Peripheral Interface (SPI)

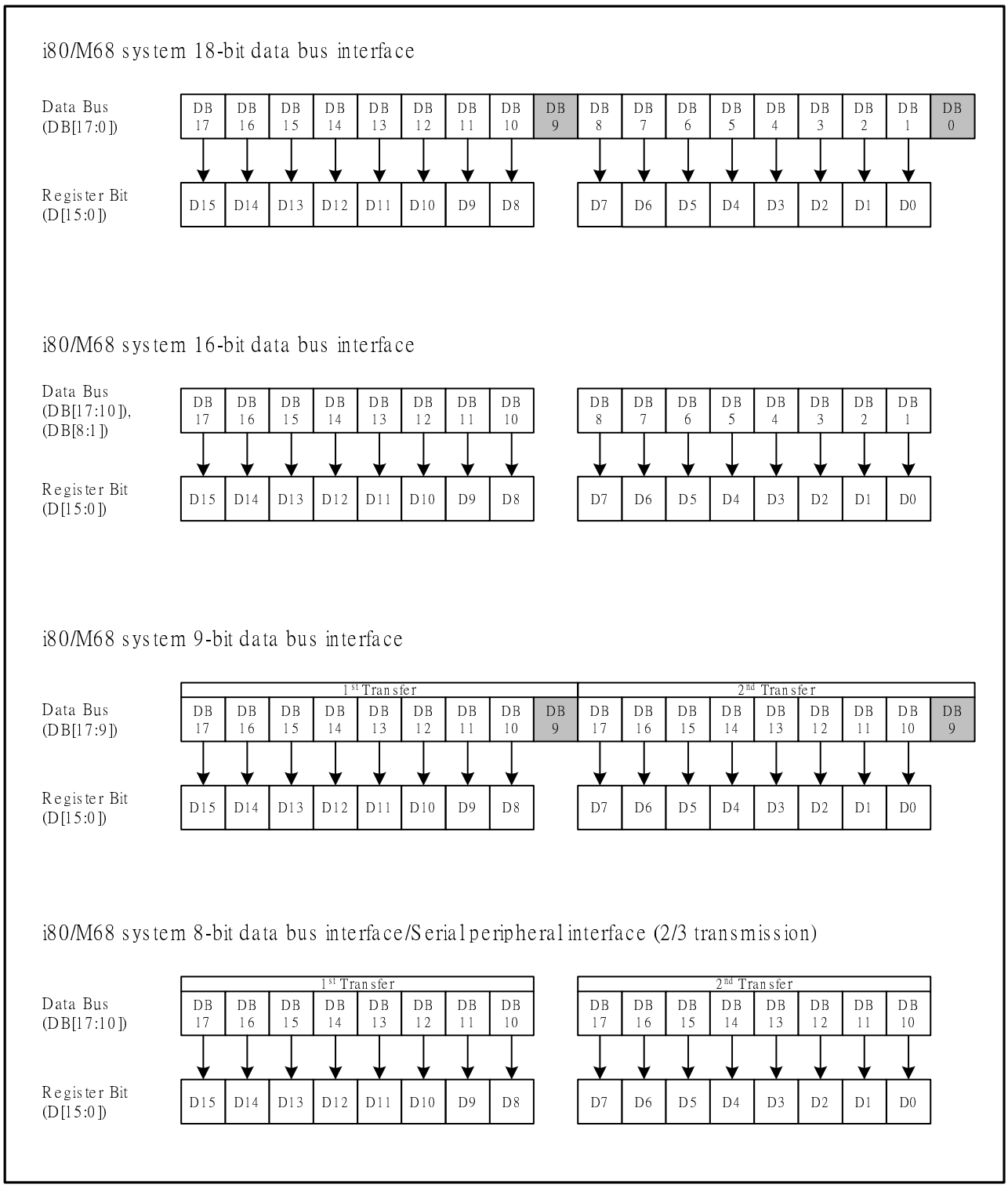
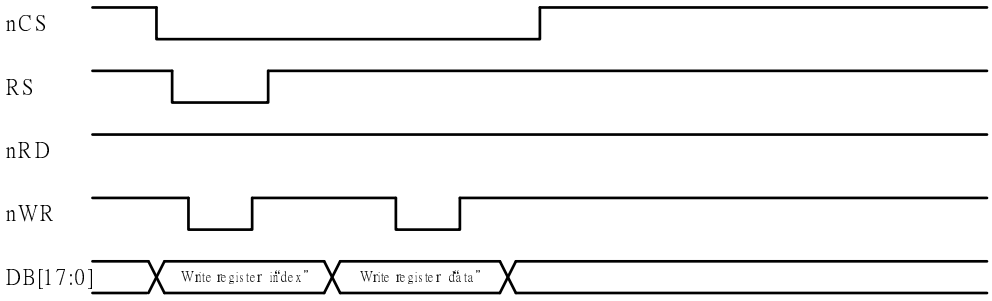


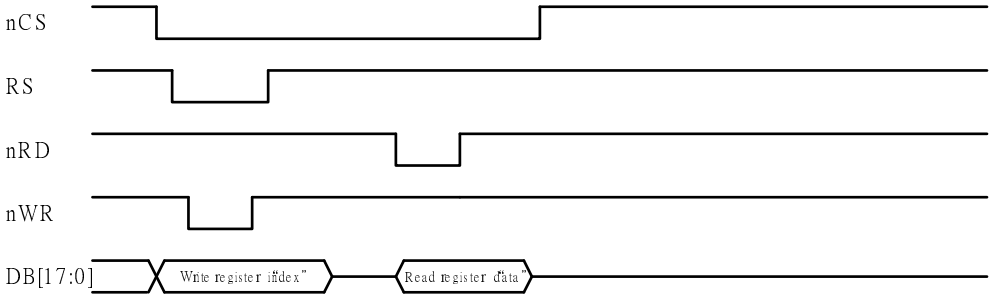
Figure21 Register setting with i80/M68 System Interface

i80 18-/16-bit System Bus Interface Timing

(a) Write to register

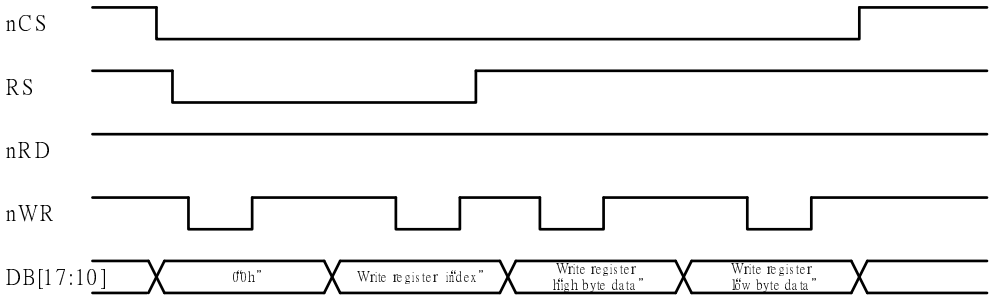


(b) Read from register



i80 9-/8-bit System Bus Interface Timing

(a) Write to register



(b) Read from register

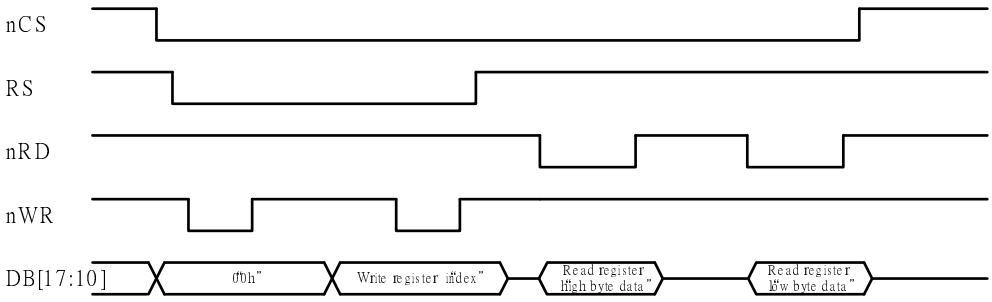


Figure22 Register Read/Write Timing of i80 System Interface

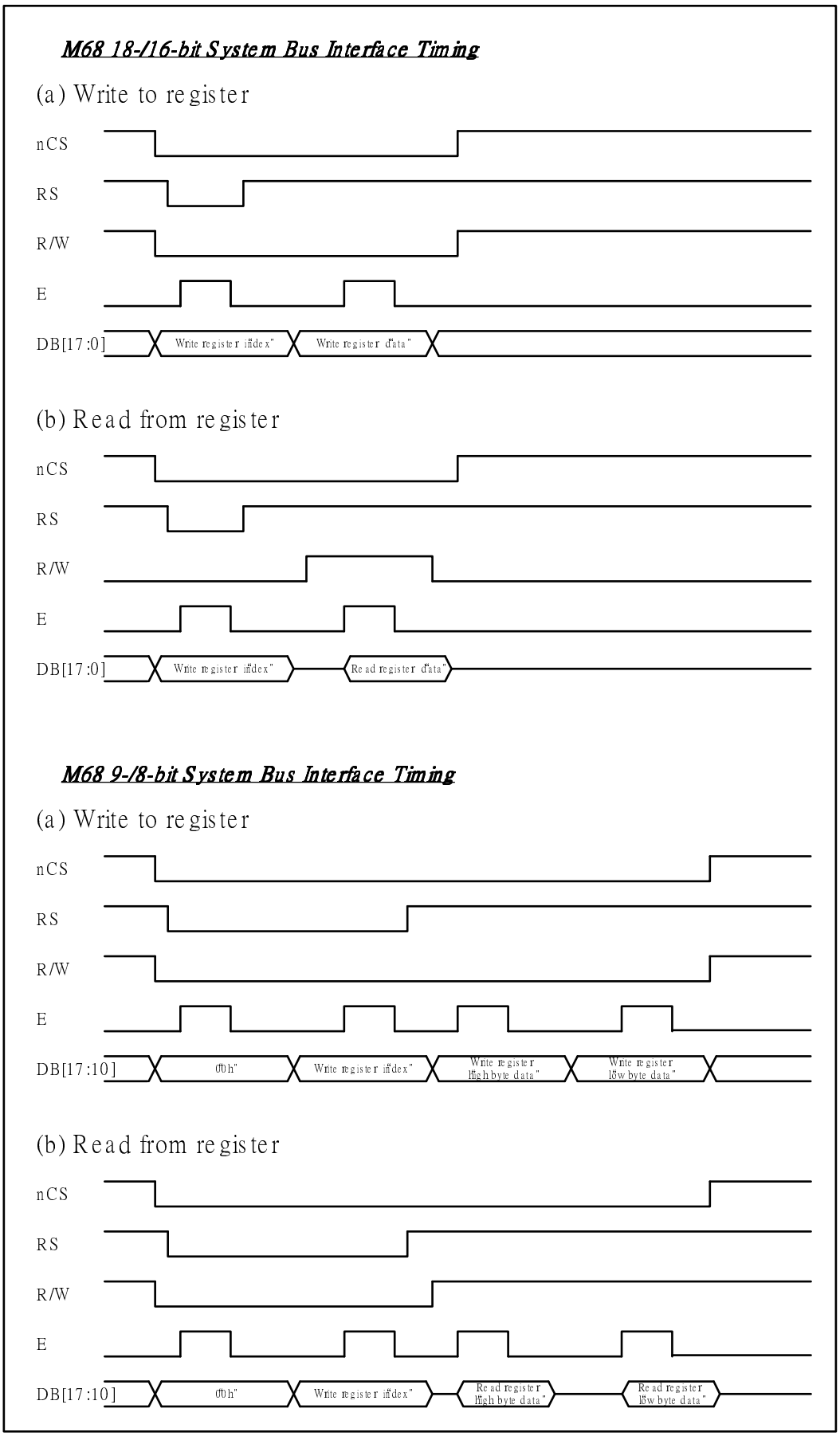


Figure23 Register Read/Write Timing of M68 System Interface

8.2. Instruction Descriptions

No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index	W	0	0	0	0	0	0	0	0	0	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
00h	Driver Code Read	R	1	1	0	0	1	0	0	1	0	0	0	1	0	0	1	1	0
01h	Driver Output Control	W	1	VSPL (0)	HSPL (0)	DPL (0)	EPL (0)	0	SM (0)	GS (0)	SS (0)	0	0	0	NL4 (1)	NL3 (1)	NL2 (1)	NL1 (0)	NL0 (0)
02h	LCD AC Driving Control	W	1	0	0	0	0	0	0	INV1 (0)	INV0 (1)	0	0	0	0	0	0	0	FLD (0)
03h	Entry Mode	W	1	0	0	0	BGR (0)	0	0	MDT1 (0)	MDT0 (0)	0	0	ID1 (1)	ID0 (1)	AM (0)	0	0	0
07h	Display Control 1	W	1	0	0	0	TEMON (0)	0	0	0	0	0	0	0	GON (0)	CL (0)	REV (0)	D1 (0)	D0 (0)
08h	Blank Period Control 1	W	1	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)
0Bh	Frame Cycle Control	W	1	NO3 (0)	NO2 (0)	NO1 (1)	NO0 (1)	SDT3 (0)	SDT2 (0)	SDT1 (0)	SDT0 (1)	0	0	0	0	RTN3 (0)	RTN2 (0)	RTN1 (0)	RTN0 (0)
0Ch	Interface Control	W	1	0	0	0	0	0	0	0	RM (0)	0	0	0	DM (0)	0	0	RIM1 (0)	RIM0 (0)
0Fh	Oscillation Control	W	1	0	0	0	0	FOSC3 (0)	FOSC2 (1)	FOSC1 (1)	FOSC0 (1)	0	0	0	0	0	0	0	OSC_ON(1)
10h	Power Control 1	W	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	STB (0)
11h	Power Control 2	W	1	0	0	0	APON (0)	0	0	0	0	0	1	0	0	0	0	0	1
12h	Power Control 3	W	1	0	BT2 (0)	BT1 (1)	BT0 (0)	0	0	0	0	0	0	0	1	0	0	1	0
13h	Power Control 4	W	1	0	0	0	0	0	0	0	0	0	GVD6 (1)	GVD5 (1)	GVD4 (0)	GVD3 (0)	GVD2 (1)	GVD1 (1)	GVD0 (0)
14h	Power Control 5	W	1	VCOMG (0)	VCM6 (1)	VCM5 (0)	VCM4 (1)	VCM3 (0)	VCM2 (0)	VCM1 (0)	VCM0 (1)	0	VML6 (1)	VML5 (1)	VML4 (0)	VML3 (1)	VML2 (0)	VML1 (0)	VML0 (1)
20h	RAM Address Set 1	W	1	0	0	0	0	0	0	0	0	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)
21h	RAM Address Set 2	W	1	0	0	0	0	0	0	0	0	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)
22h	Write Data to GRAM	W	1	WD[17:0]: Pin assignment varies according to the interface method.															
22h	Read Data to GRAM	R	1	RD[17:0]: Pin assignment varies according to the interface method.															

No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
30h	Gate Scan Control	W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)
31h	Vertical Scroll Control 1	W	1	0	0	0	0	0	0	0	0	SEA7 (1)	SEA6 (1)	SEA5 (0)	SEA4 (1)	SEA3 (1)	SEA2 (0)	SEA1 (1)	SEA0 (1)
32h	Vertical Scroll Control 2	W	1	0	0	0	0	0	0	0	0	SSA7 (0)	SSA6 (0)	SSA5 (0)	SSA4 (0)	SSA3 (0)	SSA2 (0)	SSA1 (0)	SSA0 (0)
33h	Vertical Scroll Control 3	W	1	0	0	0	0	0	0	0	0	SST7 (0)	SST6 (0)	SST5 (0)	SST4 (0)	SST3 (0)	SST2 (0)	SST1 (0)	SST0 (0)
34h	Partial Driving Position -1	W	1	0	0	0	0	0	0	0	0	SE17 (1)	SE16 (1)	SE15 (0)	SE14 (1)	SE13 (1)	SE12 (0)	SE11 (1)	SE10 (1)
35h	Partial Driving Position -2	W	1	0	0	0	0	0	0	0	0	SS17 (0)	SS16 (0)	SS15 (0)	SS14 (0)	SS13 (0)	SS12 (0)	SS11 (0)	SS10 (0)
36h	Horizontal Window Address -1	W	1	0	0	0	0	0	0	0	0	HEA7 (1)	HEA6 (0)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)
37h	Horizontal Window Address -2	W	1	0	0	0	0	0	0	0	0	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)
38h	Vertical Window Address -1	W	1	0	0	0	0	0	0	0	0	VEA7 (1)	VEA6 (1)	VEA5 (0)	VEA4 (1)	VEA3 (1)	VEA2 (0)	VEA1 (1)	VEA0 (1)
39h	Vertical Window Address -2	W	1	0	0	0	0	0	0	0	0	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)
50h	Gamma Control 1	W	1	0	0	0	0	KP13 (0)	KP12 (0)	KP11 (0)	KP10 (0)	0	0	0	0	KP03 (0)	KP02 (0)	KP01 (0)	KP00 (0)
51h	Gamma Control 2	W	1	0	0	0	0	KP33 (1)	KP32 (0)	KP31 (0)	KP30 (0)	0	0	0	0	KP23 (1)	KP22 (0)]	KP21 (0)	KP20 (0)
52h	Gamma Control 3	W	1	0	0	0	0	KP53 (1)	KP52 (0)	KP51 (0)	KP50 (0)	0	0	0	0	KP43 (1)	KP42 (0)	KP41 (1)	KP40 (0)
53h	Gamma Control 4	W	1	0	0	0	0	RP13 (0)	RP12 (0)	RP11 (0)	RP10 (0)	0	0	0	0	RP03 (1)	RP02 (0)	RP01 (1)	RP00 (0)
54h	Gamma Control 5	W	1	0	0	0	0	KN13 (1)	KN12 (0)	KN11 (1)	KN10 (0)	0	0	0	0	KN03 (1)	KN02 (0)	KN01 (0)	KN00 (0)
55h	Gamma Control 6	W	1	0	0	0	0	KN33 (1)	KN32 (0)	KN31 (0)	KN30 (0)	0	0	0	0	KN23 (1)	KN22 (0)	KN21 (0)	KN20 (0)
56h	Gamma Control 7	W	1	0	0	0	0	KN53 (0)	KN52 (0)	KN51 (0)	KN50 (0)	0	0	0	0	KN43 (0)	KN42 (0)	KN41 (0)	KN40 (0)
57h	Gamma Control 8	W	1	0	0	0	0	RN13 (1)	RN12 (0)	RN11 (1)	RN10 (0)	0	0	0	0	RN03 (0)	RN02 (0)	RN01 (0)	RN00 (0)

No.	Registers Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
58h	Gamma Control 9	W	1	0	0	0	VRP14 (0)	VRP13 (0)	VRP12 (1)	VRP11 (1)	VRP10 (1)	0	0	0	VRP04 (1)	VRP03 (0)	VRP02 (0)	VRP01 (0)	VRP00 (0)
59h	Gamma Control 10	W	1	0	0	0	VRN14 (0)	VRP13 (0)	VRP12 (1)	VRP11 (1)	VRP10 (1)	0	0	0	VRN04 (1)	VRN03 (0)	VRN02 (0)	VRN01 (0)	VRN00 (0)
60h	NV Memory Data Programming	W	1	0	0	0	0	0	0	0	0	NVM_ D7	NVM_ D6	NVM_ D5	NVM_ D4	NVM_ D3	NVM_ D2	NVM_ D1	NVM_ D0
61h	NV Memory Control	W	1	0	0	0	0	0	0	0	VCM_ SEL	0	0	0	0	0	0	ID_PGM_ EN	VCM_ PGM_EN
62h	NV Memory Status	W	1	0	0	PGM_ CNT2	PGM_ CNT1	0	0	0	0	0	VCM_ D6	VCM_ D5	VCM_ D4	VCM_ D3	VCM_ D2	VCM_ D1	VCM_ D0
63h	NV Memory Protection Key	R		KEY 15	KEY 14	KEY 13	KEY 12	KEY 11	KEY 10	KEY 9	KEY 8	KEY 7	KEY 6	KEY 5	KEY 4	KEY 3	KEY 2	KEY 1	KEY 0
65h	ID Code	R		0	0	0	0	0	0	0	0	0	0	0	0	ID3	ID2	ID1	ID0
66h	SPI Read/Write Control	R		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/WX (0)

8.2.1. Index (IR)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	0	-	-	-	-	-	-	-	-	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the address of register (R00h ~ RFFh) or RAM which will be accessed.

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8.2.2. Chip ID Code (R00h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	1
R	1	1	0	0	1	0	0	1	0	0	0	1	0	0	1	1	0

The device code “9226”h is read out when read this register.

8.2.3. Driver Output Control (R01h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	VSPL	HSPL	DPL	EPL	0	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0

VSPL: Inverts the polarity of signals from the VSYNC pin.

VSPL = ”0” : Low active.

VSPL = ”1” : High active.

HSPL: Inverts the polarity of signals from the HSYNC pin.

HSPL = ”0” : Low active.

HSPL = ”1” : High active.

DPL: Inverts the polarity of signals from the DOTCLK pin.

DPL = ”0” : Data are read on the rising edge of the DOTCLK.

DPL = ”1” : Data are read on the falling edge of the DOTCLK.

EPL: Set the polarity of the signal from the ENABLE pin in RGB interface mode. .

EPL = “0”:

ENABLE = “Low” / Write data to DB[17:0]

ENABLE = “High” / Inhibit data write operation

EPL =”1”:

ENABLE = “High” / Write data to DB[17:0]

ENABLE = “Low” / Inhibit data write operation

The following table shows the relationship between the EPL, ENABLE bits, and RAM access.

EPL	ENABLE	RAM write	RAM address
0	0	Enabled	Updated
0	1	Inhibited	Retained
1	0	Inhibited	Retained
1	1	Enabled	Updated

SS: Select the shift direction of outputs from the source driver.

When SS = 0, the shift direction of outputs is from S1 to S528

When SS = 1, the shift direction of outputs is from S528 to S1.

In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, B dots to the source driver pins.

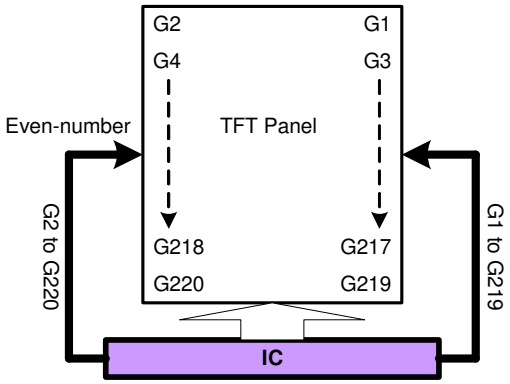
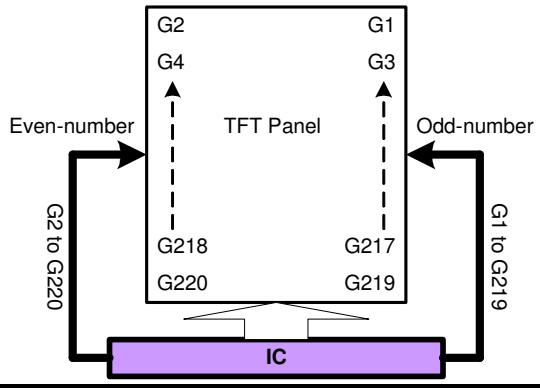
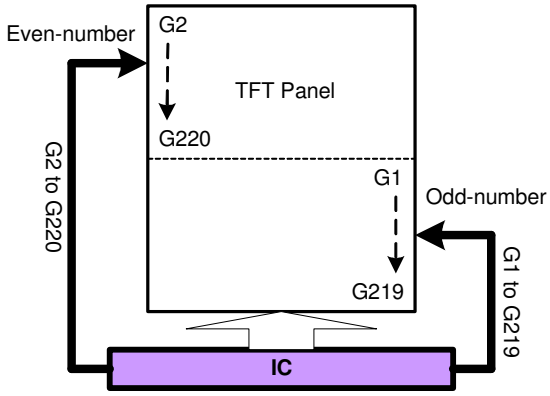
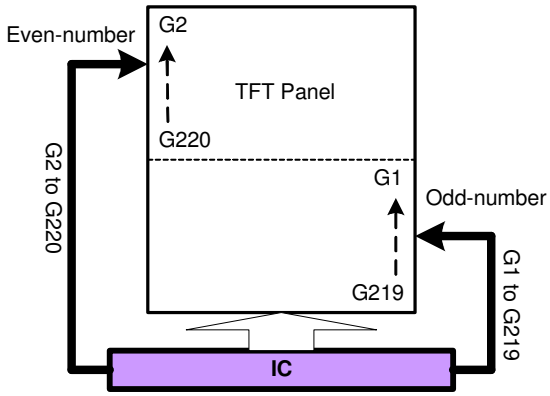
To assign R, G, B dots to the source driver pins interchangeably from S1, set SS = 0, BGR = 0.

To assign R, G, B dots to the source driver pins interchangeably from S528, set SS = 1, BGR = 1.

When changing SS or BGR bits, RAM data must be rewritten.

GS: Select the shift direction of outputs from the gate driver. The scan order is changeable in accordance to the scan mode by the gate driver. Select an optimum shift direction for the assembly.

SM: Set the scan order by the gate driver. Select an optimum scan order for the assembly.

SM	GS	Scan Direction	Gate Output Sequence
0	0		G1, G2, G3, G4, …,G216 G217, G218, G219, G220
0	1		G220, G219, G218, …, G6, G5, G4, G3, G2, G1
1	0		G1, G3, G5, G7, …,G211 G213, G215, G217, G219 G2, G4, G6, G8, …,G212 G214, G216, G218, G220
1	1		G220, G218, G216, …, G10, G8, G6, G4, G2 G219, G217, G215, …, G9, G78, G5, G3, G1

NL[4:0] Set the active gate driver line to drive the liquid crystal display panel with 8 multiples as the following

table. The GRAM address mapping is independent from the number of gate lines set with the NL[4:0] bits.

NL4	NL3	NL2	NL1	NL0	Display Size	Number of LCD Driver Lines	Gate Driver Used
0	0	0	0	0	Reserved		
0	0	0	0	1	528 * 8 dots	8	G1~G8
0	0	0	1	0	528 * 16 dots	16	G1~G16
0	0	0	1	1	528 * 24 dots	24	G1~G24
0	0	1	0	0	528 * 32 dots	32	G1~G32
0	0	1	0	1	528 * 40 dots	40	G1~G40
0	0	1	1	0	528 * 48 dots	48	G1~G48
0	0	1	1	1	528 * 56 dots	56	G1~G56
0	1	0	0	0	528 * 64 dots	64	G1~G64
0	1	0	0	1	528 * 72 dots	72	G1~G72
0	1	0	1	0	528 * 80 dots	80	G1~G80
0	1	0	1	1	528 * 88 dots	88	G1~G88
0	1	1	0	0	528 * 96 dots	96	G1~G96
0	1	1	0	1	528 * 104 dots	104	G1~G104
0	1	1	1	0	528 * 112 dots	112	G1~G112
0	1	1	1	1	528 * 120 dots	120	G1~G120
1	0	0	0	0	528 * 128 dots	128	G1~G128
1	0	0	0	1	528 * 136 dots	136	G1~G136
1	0	0	1	0	528 * 144 dots	144	G1~G144
1	0	0	1	1	528 * 152 dots	152	G1~G152
1	0	1	0	0	528 * 160 dots	160	G1~G160
1	0	1	0	1	528 * 168 dots	168	G1~G168
1	0	1	1	0	528 * 176 dots	176	G1~G176
1	0	1	1	1	528 * 184 dots	184	G1~G184
1	1	0	0	0	528 * 192 dots	192	G1~G200
1	1	0	0	1	528 * 200 dots	200	G1~G208
1	1	0	1	0	528 * 208 dots	208	G1~G216
1	***1***	***0***	***1***	***1***	528 * 216 dots	216	G1~G220
1	1	1	0	0	528 * 220 dots	220	G1~G220

8.2.4. LCD Driving Waveform Control (R02h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	INV1	INV0	0	0	0	0	0	0	0	FLD

Set LCD inversion method as show below.

Enables or disables 3-field interlaced scanning function like below.

INV[1:0]	FLD	Description
00	0	Frame Inversion – 1 field interlace
	1	3 field interlace
01	0	Line Inversion – 1 field interlace
	1	Setting Disable
10	0	Two Line Inversion – 1 field interlace
	1	Setting Disable
11	0	No Inversion. Active with positive polarity (VCOM = Low)
	1	No Inversion. Active with negative polarity (VCOM = High)

GS = 0"					
FLD	0"	1"			
Gate \ Field	-	1	2	3	4
G1	*	*			*
G2	*		*		
G3	*			*	
G4	*	*			*
G5	*		*		
G6	*			*	
G7	*	*			*
G8	*		*		
G9	*			*	
G10	*	*			*
	⋮	⋮	⋮	⋮	⋮
G217	*	*		*	
G218	*		*		*
G219	*			*	
G220	*	*			*

GS = 1"					
FLD	0"	1"			
Gate \ Field	-	1	2	3	4
G220	*	*			*
G219	*		*		
G218	*			*	
G217	*	*			*
G216	*		*		
G215	*			*	
G214	*	*			*
G213	*		*		
G212	*			*	
G211	*	*			*
	⋮	⋮	⋮	⋮	⋮
G4	*	*		*	
G3	*		*		*
G2	*			*	
G1	*	*			*

Figure24 Interlace Scan of AC Drive

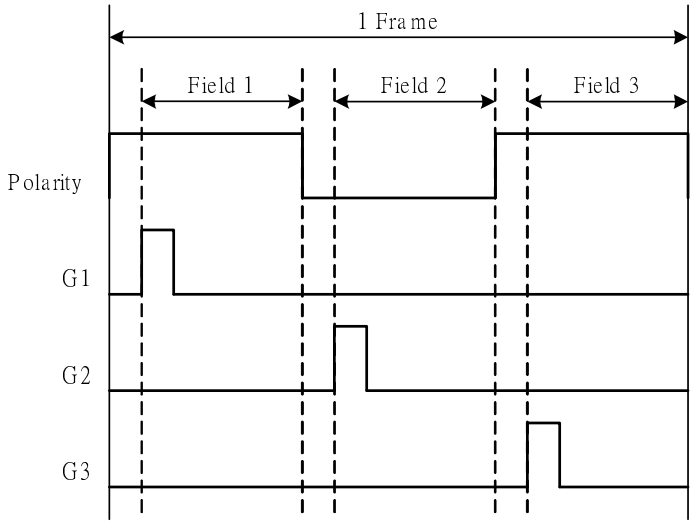


Figure25 Output Timing of Interlace Gate Signals (Three-field is selected)

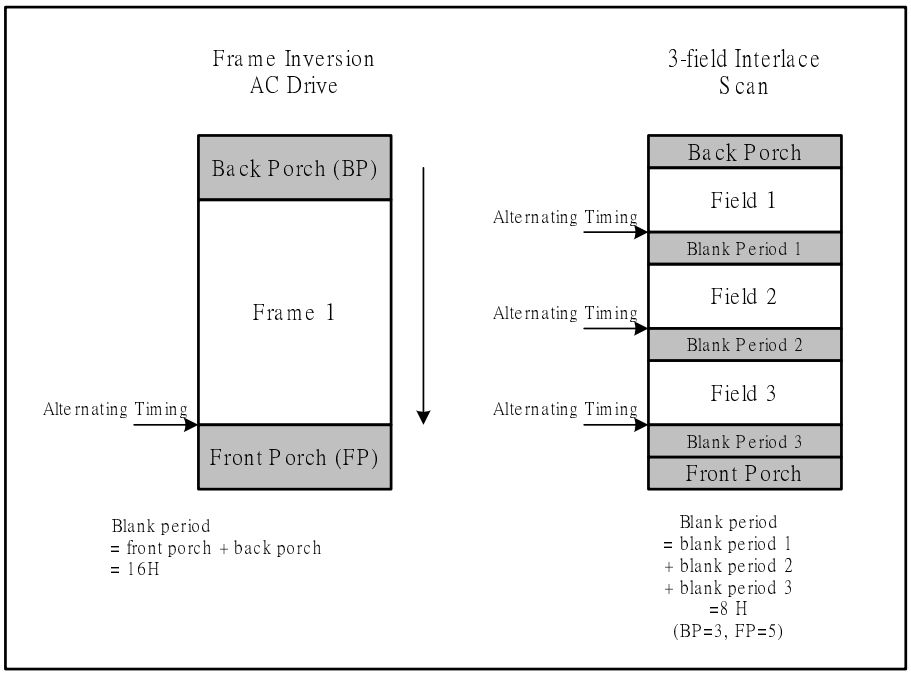


Figure26 AC Driving Alternating Timing

8.2.5. Entry Mode (R03h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	BGR	0	0	MDT1	MDT0	0	0	I/D1	I/D0	AM	0	0	0

AM Control the GRAM update direction. When AM = “0”, the address is updated in horizontal writing direction. When AM = “1”, the address is updated in vertical writing direction. When a window area is set by registers R36h/R37h and R38h/R39h, only the addressed GRAM area is updated based on I/D[1:0] and AM bits setting.

I/D[1:0] Control the address counter (AC) to automatically increase or decrease by 1 when update one pixel display data. Refer to the following figure for the details.

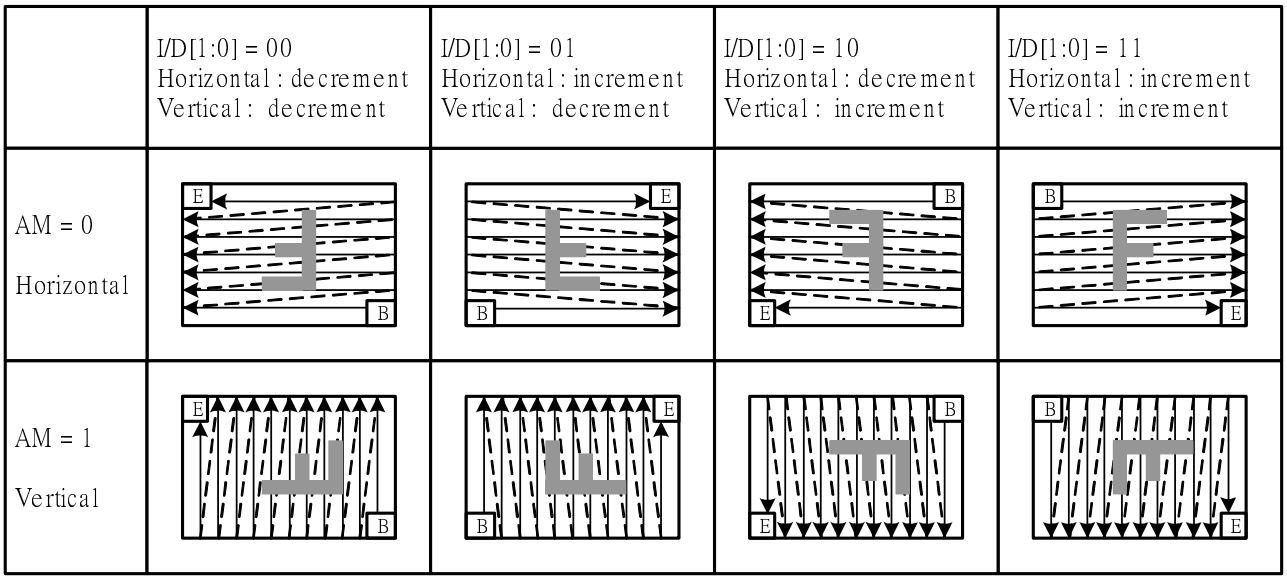


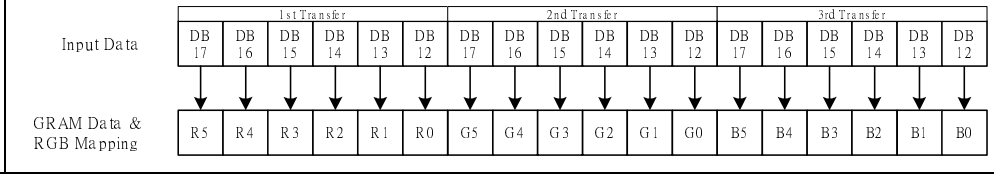
Figure27 GRAM Access Direction Setting

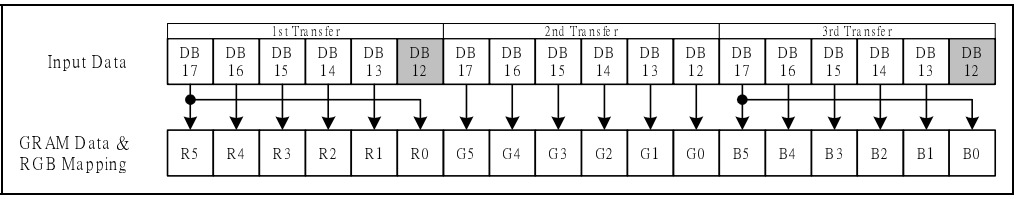
AM	I/D[1:0]	Register R20/R21 Start Address	
0/1	00	R20	00AFh
		R21	00DBh
	01	R20	0000h
		R21	00DBh
	10	R20	00Afh
		R21	0000h
	11	R20	0000h
		R21	0000h

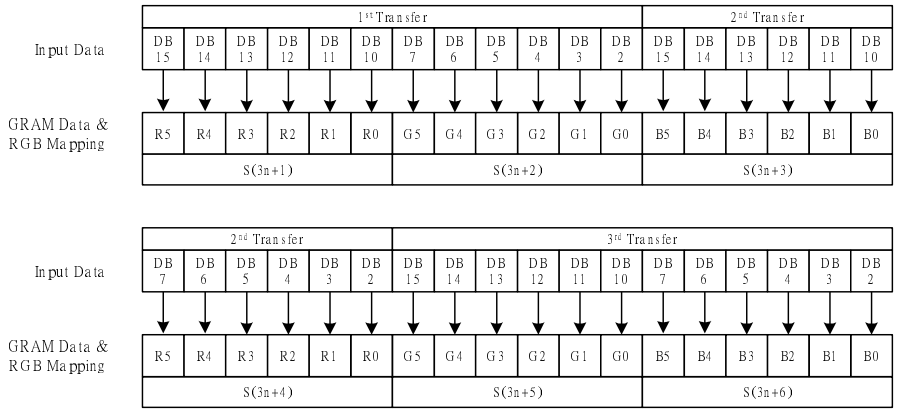
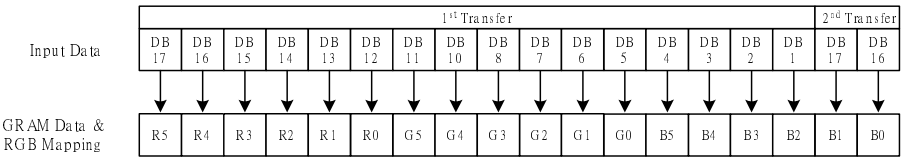
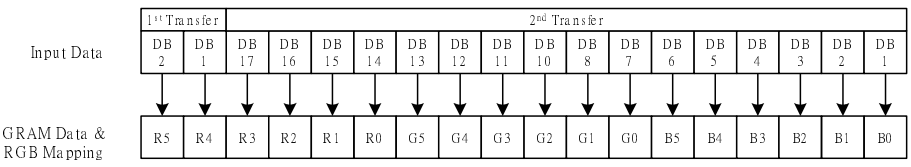
MDT1: This bit is active on the 80-system of 8-bit bus and the data for 1-pixel is transported to the memory for 3 write cycles. This bit is on the 80-system of 16-bit bus, and the data for 1-pixel is transported to the memory for 2 write cycles. When the 80-system interface mode is not set in the 8-bit or16-bit mode, set MDT1 bit to be “0”.

MDT0: When 8-bit or16-bit 80 interface mode and MDT1 bit =1, MDT0 defines color depth for the IC.

BGR Swap the R and B order of written data.

Interface Mode	MDT1	MDT0	Write data to GRAM
*	0	0	Default transfer value. Multiple data transfer (MDT[1:0]) function is not available. Data transfer is controlled by interface mode.
	0	1	Multiple data transfer (MDT[1:0]) function is not available.
80-system 8-bit	1	0	

	1	1	

Interface Mode	MDT1	MDT0	Write data to GRAM
80-system 16-bit	0	1	
	1	0	
	1	1	

8-bit (80-system), MDT0 = 0: 262k-color mode (3 times of 6-bit data transfer to GRAM)

8-bit (80-system), MDT0 = 1: 65k-color mode (5-bit, 6-bit, 5-bit data transfer to GRAM)

16-bit (80-system), MDT0 = 0: 262k-color mode (16-bit, 2-bit data transfer to GRAM)

16-bit (80-system), MDT1 = 1: 262k-color mode (2-bit, 16-bit data transfer to GRAM)

8.2.6. Display Control 1 (R07h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	TEMON	0	0	0	0	0	0	0	GON	CL	REV	D1	D0

D[1:0] Set D[1:0]="11" to turn on the display panel, and D[1:0]="00" to turn off the display panel.

D1	D0	GON	Source Output	Gate Output	VCOM Output	Display
0	0	X	VSS	VGL	VSS	Off
0	1	0	VSS	VGL	VSS	Off
		1	VSS	Operate	VSS	Off
1	0	0	White on Normally WhitePanel Black on Normally Black Panel	VGL	Operate	Off
		1	White on Normally WhitePanel Black on Normally Black Panel	Operate	Operate	Off
1	1	0	Normal Display	VGL	Operate	Off
		1	Normal Display	Operate	Operate	On

Note: data write operation from the microcontroller is performed irrespective of the setting of D[1:0] bits.

GON Set the output level of gate driver G1 ~ G220 as follows

GON	G1 ~G220 Gate Output
0	VGL
1	**Normal Display**

CL When CL = "1", the 8-color display mode is selected.

CL	Colors
0	262,144
1	8

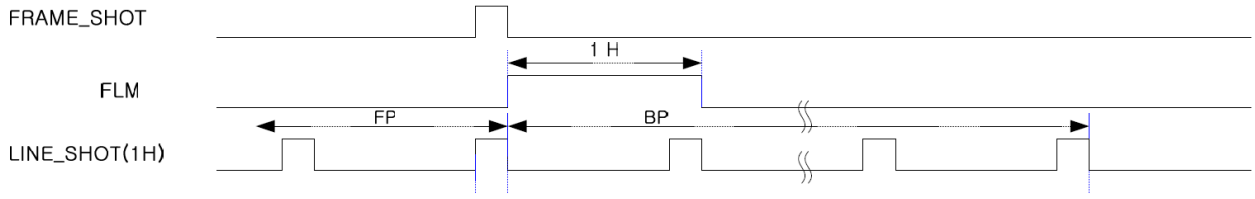
REV When REV = "1", the grayscale levels can be inverted.

REV	GRAM Data	Source Output in Display Area	
		Positive polarity	negative polarity
0	18'h00000	V63	V0
	.	.	.
	.	.	.
	.	.	.
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	.	.	.
	.	.	.
	.	.	.
	18'h3FFFF	V63	V0

TEMON :

TEMON = 1, Enable the Frame flag output signal from the FLM signal line for preventing Tearing Effect.

TEMON = 0, Disable the Frame flag output signal from the FLM signal line for preventing Tearing Effect.



8.2.7. Display Control 2 (R08h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

FP[3:0]/BP[3:0]

The FP[3:0] and BP[3:0] bits specify the line number of front and back porch periods respectively.

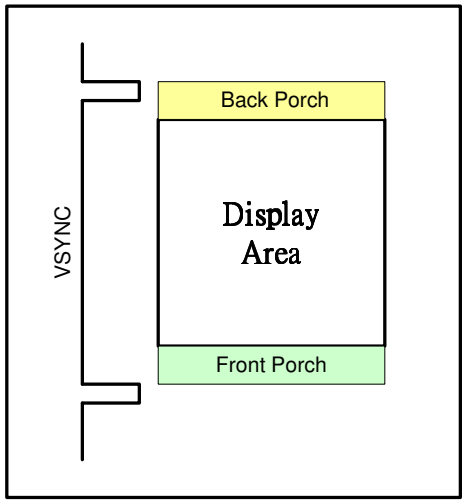
When setting the FP[3:0] and BP[3:0] value, the following conditions shall be met:

BP + FP ≤ 16 lines

FP ≥ 2 lines

BP ≥ 2 lines

FP[3:0]	Number of lines for Front Porch
BP[3:0]	Number of lines for Back Porch
0000	Setting Prohibited
0001	Setting Prohibited
0010	2 lines
0011	3 lines
0100	4 lines
0101	5 lines
0110	6 lines
0111	7 lines
1000	8 lines
1001	9 lines
1010	10 lines
1011	11 lines
1100	12 lines
1101	13 lines
1110	14 lines
1111	Setting Prohibited



Note: The output timing to the LCD is delayed by 2 lines period from the input of synchronizing signal.

Set the BP[3:0] and FP[3:0] bits as below for each operation mode

Operation Mode	Number of Interlace Scan Field	BP	FP	BP+FP
I80/M68 System Interface	**FLD = "0"**	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
	FLD = "1"	BP = 3 lines	FP = 5 lines	-
RGB interface		BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines

8.2.8. Frame Cycle Control (R0Bh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

W	1	NO3	NO2	NO1	NO0	SDT3	SDT2	SDT1	SDT0	0	0	0	0	RTN3	RTN2	RTN1	RTN0

RTN[3:0] Set the clock cycle number of one display line.

RTN[3:0]	Clock Cycles per line
4'h0	16 clocks
4'h1	17 clocks
4'h2	18 clocks
4'h3	19 clocks
4'h4	20 clocks
4'h5	21 clocks
4'h6	22 clocks
4'h7	23 clocks
4'h8	24 clocks
4'h9	25 clocks
4'hA	26 clocks
4'hB	27 clocks
4'hC	28 clocks
4'hD	29 clocks
4'hE	30 clocks
4'hF	31 clocks

NO[3:0]: Set amount of non-overlay for the gate output.

	Gate output delay period		
NO[3:0]	System Interface Mode	18/16-bit RGB Interface Mode	6-bit RGB Interface Mode
4'h0	Setting disable	Setting disable	Setting disable
4'h1	1 clock	8 clocks	8*3 clocks
4'h2	2 clocks	16 clocks	16*3 clocks
4'h3	3 clocks	24 clocks	24*3 clocks
4'h4	4 clocks	32 clocks	32*3 clocks
4'h5	5 clocks	40 clocks	40*3 clocks
4'h6	6 clocks	48 clocks	48*3 clocks
4'h7	7 clocks	56 clocks	56*3 clocks
4'h8	8 clocks	64 clocks	64*3 clocks
4'h9	9 clocks	72 clocks	72*3 clocks
4'hA	10 clocks	80 clocks	80*3 clocks
4'hB	Setting disable	88 clocks	88*3 clocks
4'hC	Setting disable	96 clocks	96*3 clocks
4'hD	Setting disable	104 clocks	104*3 clocks
4'hE	Setting disable	112 clocks	112*3 clocks
4'hF	Setting disable	120 clocks	120*3 clocks

SDT[3:0]: Set delay amount from gate edge (end) to source output.

	Source output delay period		
SDT[3:0]	System Interface Mode	18/16-bit RGB Interface Mode	6-bit RGB Interface Mode
4'h0	Setting disable	Setting disable	Setting disable
4'h1	1 clock	8 clocks	8*3 clocks
4'h2	2 clocks	16 clocks	16*3 clocks
4'h3	3 clocks	24 clocks	24*3 clocks

4'h4	4 clocks	32 clocks	32*3 clocks
4'h5	5 clocks	40 clocks	40*3 clocks
4'h6	6 clocks	48 clocks	48*3 clocks
4'h7	Setting disable	Setting disable	Setting disable
4'h8	Setting disable	Setting disable	Setting disable
4'h9	Setting disable	Setting disable	Setting disable
4'hA	Setting disable	Setting disable	Setting disable
4'hB	Setting disable	Setting disable	Setting disable
4'hC	Setting disable	Setting disable	Setting disable
4'hD	Setting disable	Setting disable	Setting disable
4'hE	Setting disable	Setting disable	Setting disable
4'hF	Setting disable	Setting disable	Setting disable

8.2.9. RGB Input Interface Control 1 (R0Ch)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	RM	0	0	0	DM	0	0	RIM1	RIM0

RIM[1:0] Select the data bus width of RGB interface modes.

RIM1	RIM0	RGB Interface Mode
0	0	18-bit RGB interface (one transfer/pixel)
0	1	16-bit RGB interface (one transfer/pixel)
1	0	6-bit RGB interface (three transfers/pixel)
1	1	Setting disabled

Note1: Registers are set only by the system interface.

Note2: Be sure that one pixel (3 dots) data transfer finished when interface switch.

DM Select the display operation mode.

DM	Display Interface
0	Internal system clock
1	RGB interface

RM Select the interface to access the GRAM.

RM	Interface for RAM Access
0	Internal system clock interface
1	RGB interface (when writing display data by the RGB interface.)

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM)]

Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM = 0)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM = 1)
Rewrite still picture area while RGB interface Displaying moving pictures. RGB interface (2)		System interface (RM = 0)	RGB interface (DM = 1)

Note 1) Registers are set only via the system interface or SPI interface.

Note 2) Refer to the flowcharts of "RGB Input Interface" section for the mode switch.

8.2.10. Oscillator Control (R0Fh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	FOSC[3]	FOSC[2]	FOSC[1]	FOSC[0]	0	0	0	0	0	0	0	OSC_EN

FOSC[3:0]: Select the oscillation frequency of internal oscillator.

FR_SEL[3:0]	Frame Rate
0000	33Hz
0001	41 Hz
0010	46 Hz
0011	50 Hz
0100	56 Hz
0101	62 Hz
0110	66 Hz
0111 (default)	71 Hz
1000	76 Hz
1001	81 Hz
1010	88 Hz
1011	96 Hz
1100	106 Hz
1101	118 Hz
1110	132 Hz
1111	Setting prohibited

**Note: This table is calculated in BP+FP=16 lines condition*

OSC_EN

This instruction starts the oscillator from the Halt State in the standby mode. After this instruction,

Wait at least 10 ms for oscillation to stabilize before giving the next instruction.

OSC_EN	OSC Control
0	OSC. Off
1	OSC. On

8.2.11. Power Control 1 (R10h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	STB

STB: When STB = 1, the ILI9225G enters the standby mode, where display operation completely stops, halting all the internal operations including the internal oscillator. Further, no external clock pulses are supplied.

Outputs	Conditions
VCOM	GND
Gate	GND
Source	GND

8.2.12. Power Control 2 (R11h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	APON	0	0	0	0	0	1	0	0	0	0	0	1

APON: This is an automatic-boosting-operation-starting bit for the booster circuits. In case of APON=0, the auto booster sequence circuit is stopped. In case of APON=1, booster circuits are automatically and sequentially operated.

8.2.13. Power Control 3 (R12h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	BT2	BT1	BT0	0	0	0	0	0	0	0	1	0	0	1	0

BT[2:0] The output factor of step-up circuit is selected. Adjust scale factor of the step-up circuit by the voltage used. Lower amplification of the step-up circuit consumes less current.

BT2	BT1	BT0	Circuit1 AVDD	Circuit4 VCL	Circuit2 VGH	Circuit3 VGL
0	0	0	2 x VCI	-1 x VCI	6 x VCI	-5 x VCI
0	0	1	2 x VCI	-1 x VCI	7 x VCI	-5 x VCI
0	1	0	2 x VCI	-1 x VCI	6 x VCI	-6 x VCI
0	1	1	2 x VCI	-1 x VCI	7 x VCI	-6 x VCI
1	0	0	2 x VCI	-1 x VCI	6 x VCI	-7 x VCI
1	0	1	2 x VCI	-1 x VCI	7 x VCI	-7 x VCI
1	1	0	2 x VCI	-1 x VCI	6 x VCI	No define
1	1	1	2 x VCI	-1 x VCI	7 x VCI	No define

Note: The conditions of AVDD≦ 5.5V and VGH ≦15.5V must be satisfied.

8.2.14. Power Control 4 (R13h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	GVD6	GVD5	GVD4	GVD3	GVD2	GVD1	GVD0

GVD[6:0]: Set the amplifying factor of the GVDD voltage (the voltage for the Gamma voltage). It allows ranging from 2.66V to 5.5V.

GVD[6:0]	GVDD	GVD[6:0]	GVDD	GVD[6:0]	GVDD	GVD[6:0]	GVDD
7'h00	5.05V	7'h20	3.10V	7'h40	3.74V	7'h60	4.38V
7'h01	5.10V	7'h21	3.12V	7'h41	3.76V	7'h61	4.40V
7'h02	5.15V	7'h22	3.14V	7'h42	3.78V	7'h62	4.42V
7'h03	5.20V	7'h23	3.16V	7'h43	3.80V	7'h63	4.44V
7'h04	5.25V	7'h24	3.18V	7'h44	3.82V	7'h64	4.46V
7'h05	5.30V	7'h25	3.20V	7'h45	3.84V	7'h65	4.48V
7'h06	5.35V	7'h26	3.22V	7'h46	3.86V	7'h66	4.50V
7'h07	5.40V	7'h27	3.24V	7'h47	3.88V	7'h67	4.52V
7'h08	5.45V	7'h28	3.26V	7'h48	3.90V	7'h68	4.54V
7'h09	5.50V	7'h29	3.28V	7'h49	3.92V	7'h69	4.56V
7'hA	2.66V	7'h2A	3.30V	7'h4A	3.94V	7'h6A	4.58V
7'hB	2.68V	7'h2B	3.32V	7'h4B	3.96V	7'h6B	4.60V
7'hC	2.70V	7'h2C	3.34V	7'h4C	3.98V	7'h6C	4.62V
7'hD	2.72V	7'h2D	3.36V	7'h4D	4.00V	7'h6D	4.64V
7'hE	2.74V	7'h2E	3.38V	7'h4E	4.02V	7'h6E	4.66V
7'hF	2.76V	7'h2F	3.40V	7'h4F	4.04V	7'h6F	4.68V
7'h10	2.78V	7'h30	3.42V	7'h50	4.06V	7'h70	4.70V
7'h11	2.80V	7'h31	3.44V	7'h51	4.08V	7'h71	4.72V
7'h12	2.82V	7'h32	3.46V	7'h52	4.10V	7'h72	4.74V
7'h13	2.84V	7'h33	3.48V	7'h53	4.12V	7'h73	4.76V
7'h14	2.86V	7'h34	3.50V	7'h54	4.14V	7'h74	4.78V
7'h15	2.88V	7'h35	3.52V	7'h55	4.16V	7'h75	4.80V
7'h16	2.90V	7'h36	3.54V	7'h56	4.18V	7'h76	4.82V
7'h17	2.92V	7'h37	3.56V	7'h57	4.20V	7'h77	4.84V
7'h18	2.94V	7'h38	3.58V	7'h58	4.22V	7'h78	4.86V
7'h19	2.96V	7'h39	3.60V	7'h59	4.24V	7'h79	4.88V
7'h1A	2.98V	7'h3A	3.62V	7'h5A	4.26V	7'h7A	4.90V
7'h1B	3.00V	7'h3B	3.64V	7'h5B	4.28V	7'h7B	4.92V
7'h1C	3.02V	7'h3C	3.66V	7'h5C	4.30V	7'h7C	4.94V
7'h1D	3.04V	7'h3D	3.68V	7'h5D	4.32V	7'h7D	4.96V
7'h1E	3.06V	7'h3E	3.70V	7'h5E	4.34V	7'h7E	4.98V
7'h1F	3.08V	7'h3F	3.72V	7'h5F	4.36V	7'h7F	5.00V

8.2.15. Power Control 5 (R14h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	VCOMG	VCM6	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	0	VML6	VML5	VML4	VML3	VML2	VML1	VML0

VCOMG: When VCOMG = 1, low level of VCOM signal is to be fixed at GND. Therefore, the amplitude of VCOM signal is determined as |VCOMH – GND| regardless of VML setting. In this case, VCOML pin can be open or connected to GND, because VCOML amp is off and VCOML output is floated. When VCOMG=0, the amplitude of VCOM signal is determined as |VCOMH – VCOML|.

VCM[6:0]: Set the VCOMH voltage (a high level voltage at the Vcom alternating drive), these bits amplify the VcomH voltage from 0.4015 to 1.1000 times the GVDD voltage.

VCM[6:0]	VCOMH Voltage
7'h00	GVDD x 0.4015
7'h01	GVDD x 0.4070
7'h02	GVDD x 0.4125
7'h03	GVDD x 0.4180
. .	. .
7'h7A	GVDD x 1.0725
7'h7B	GVDD x 1.0780
7'h7C	GVDD x 1.0835
7'h7D	GVDD x 1.0890
7'h7E	GVDD x 1.0945
7'h7F	GVDD x 1.100

[NOTE]

1. ***VcomH = GVDD x (0.4015 + 0.0055 x VCM)***
2. When using VCI recycling function, VCOMH voltage should be higher than VCI.
3. VCM[6:0] register set is invalid when VCM_SEL=1.

VML[6:0]: Set the alternating amplitudes of VCOM at the VCOM alternating drive. These bits amplify VCOM from 0.534 to 1.20 times the GVDD voltage. When the VCOM alternation is not driven, the settings become invalid.

VML[6:0]	VCOM Amplitude Voltage
7'h00~7'0F	Setting prohibited
7'h10	GVDD x 0.534
7'h11	GVDD x 0.540
7'h12	GVDD x 0.546
. .	. .
7'h7A	GVDD x 1.170
7'h7B	GVDD x 1.176
7'h7C	GVDD x 1.182
7'h7D	GVDD x 1.188
7'h7E	GVDD x 1.194
7'h7F	GVDD x 1.200

[NOTE]

1. ***VCOM amplitude = GVDD x (0.534 + 0.006(VML-16))***
2. Adjust the settings between GVDD and VML[6:0] so that the Vcom amplitudes are lower than 6.0 V.
3. VCOML voltage should be satisfied the following condition. : 0.0V > VCOML > VCL+0.5V

8.2.16. RAM Address Set (R20h, R21h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	x	x	x	x	x	x	x	x	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
W	1	x	x	x	x	x	x	x	x	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

AD[15:0] Set the initial value of address counter (AC).

The address counter (AC) is automatically updated in accordance to the setting of the AM, I/D bits as data is written to the internal GRAM. The address counter is not automatically updated when read data from the internal GRAM.

Note1:GRAM address setting is not allowed in standby mode. Ensure that the address is set within the specified window area specified with VSA, VEA, HAS and HEA.

Note2: When the RGB interface is selected (RM = "1"), the address AD[15:0] is set to the address counter every frame on the falling edge of VSYNC.

Note3: When the internal clock operation or the VSYNC interface mode is selected (RM = "0"), the address AD[15:0] is set upon the execution of an instruction.

GRAM Address Range

AD[15:0]	Gram setting
"0000H" to "00AF"H	Bitmap data for G1
"0100H" to "01AF"H	Bitmap data for G2
"0200H" to "02AF"H	Bitmap data for G3
"0300H" to "03AF"H	Bitmap data for G4
:	:
"0800H" to "D8AF"H	Bitmap data for G217
"0900H" to "D9AF"H	Bitmap data for G218
"0A00H" to "DAAF"H	Bitmap data for G219
"0B00H" to "DBAF"H	Bitmap data for G220

8.2.17. Write Data to GRAM (R22h)

R/W	RS	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	RAM write data (WD[17:0], the DB[17:0] pin assignment differs for each interface.																	

This register is the GRAM access port. When update the display data through this register, the address counter (AC) is increased/decreased automatically.

8.2.18. Read Data from GRAM (R22h)

R/W	RS	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	RAM Read Data (RD[17:0], the DB[17:0] pin assignment differs for each interface.																	

RD[17:0] Read 18-bit data from GRAM through the read data register (RDR).

8.2.19. Gate Scan Control (R30h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0

SCN[4:0] The ILI9225G allows specifying the gate line from which the gate driver starts scan by setting the SCN[4:0] bits.

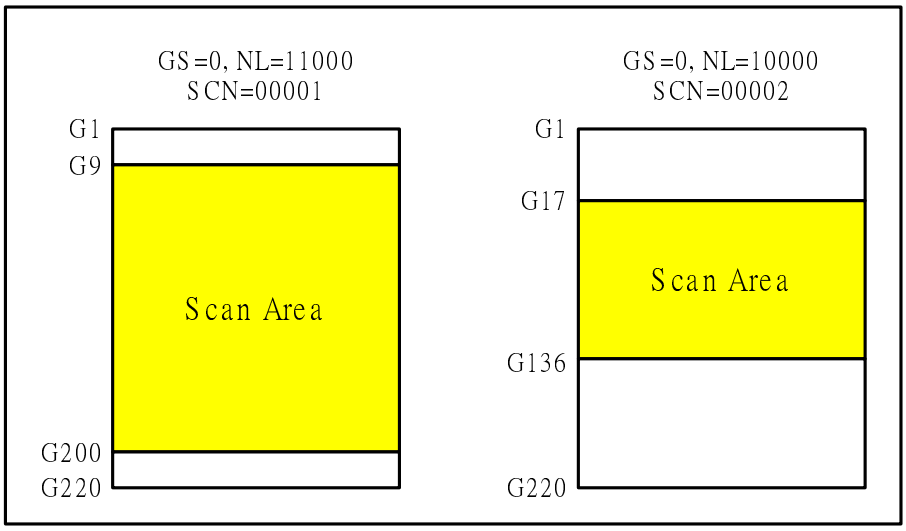


Figure28 Scanning Start Position for Gate Driver

Note: Don't set NL[4:0], SCN[4:0] over the end position of gate line (G220)

Note: Set NL[4:0] and SCN[4:0] to let the number for the end position of the gate line scans will not exceed 220.

SCN4	SCN3	SCN2	SCN1	SCN0	Scanning Start Position			
					SM=0 GS=0	SM=0 GS=1	SM=1 GS=0	SM=1 GS=1
0	0	0	0	0	G1	G220	G1	G220
0	0	0	0	1	G9	G212	G17	G204
0	0	0	1	0	G17	G204	G33	G188
0	0	0	1	1	G25	G196	G49	G172
0	0	1	0	0	G33	G188	G65	G156
0	0	1	0	1	G41	G180	G81	G140
0	0	1	1	0	G49	G172	G97	G124
0	0	1	1	1	G57	G164	G113	G108
0	1	0	0	0	G65	G156	G129	G92
0	1	0	0	1	G73	G148	G145	G76
0	1	0	1	0	G81	G140	G161	G60
0	1	0	1	1	G89	G132	G177	G44
0	1	1	0	0	G97	G124	G193	G28
0	1	1	0	1	G105	G116	G209	G12
0	1	1	1	0	G113	G108	G2	G219
0	1	1	1	1	G121	G100	G18	G203
1	0	0	0	0	G129	G92	G34	G187
1	0	0	0	1	G137	G84	G50	G171
1	0	0	1	0	G145	G76	G66	G155
1	0	0	1	1	G153	G68	G82	G139
1	0	1	0	0	G161	G60	G98	G123
1	0	1	0	1	G169	G52	G114	G107
1	0	1	1	0	G177	G44	G130	G91

1	0	1	1	1	G185	G36	G146	G75
1	1	0	0	0	G193	G28	G162	G59
1	1	0	0	1	G201	G20	G178	G43
1	1	0	1	0	G209	G12	G194	G27
1	1	0	1	1	G217	G4	G210	G11

8.2.20. Vertical Scroll Control 1 (R31h, R32h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	SEA7	SEA6	SEA5	SEA4	SESA3	SEA2	SEA1	SEA0
W	1	0	0	0	0	0	0	0	0	SSA7	SSA6	SSA5	SSA4	SSA3	SSA2	SSA1	SSA0

SSA[7:0]: Specify scroll start address at the scroll display for vertical smooth scrolling.

SSA7	SSA 6	SSA 5	SSA 4	SSA 3	SSA 2	SSA 1	SSA 0	Scroll Start Lines
0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	1	0	2 lines
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	0	1	1	0	1	0	218 lines
1	1	0	1	1	0	1	1	219 lines

SEA[7:0]: Specify scroll end address at the scroll display for vertical smooth scrolling.

SEA7	SEA 6	SEA 5	SEA 4	SEA 3	SEA 2	SEA 1	SEA 0	Scroll End Lines
0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	1	0	2 lines
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	0	1	1	0	1	0	218 lines
1	1	0	1	1	0	1	1	219 lines

NOTE]

Do not set any higher raster-row than 219 (“DB”H).

Set SS17-10 ≤ SSA7-0, if set out of range, SSA7-0 = SS17-10.

Set SE17-10 ≥ SEA7-0, if set out of range, SEA7-0 = SE17-10

8.2.21. Vertical Scroll Control 1 (R33h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	SST7	SST6	SST5	SST4	SST3	SST2	SST1	SST0

SST8-0: Specify scroll start and step at the scroll display for vertical smooth scrolling. Any line from the 1st to 220th can be scrolled for the number of the raster-row. After 219th line is displayed, the display restarts from the first raster-row. When SST7-0 = 00000000, Vertical Scroll Function is disabled.

SST7	SST 6	SST 5	SST 4	SST 3	SST 2	SST 1	SST 0	Scrolling Lines
0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	1	0	2 lines
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	0	1	1	0	1	0	218 lines
1	1	0	1	1	0	1	1	219 lines

[NOTE]

Do not set any higher raster-row than 219 (“DB”H)

Set SS17-10 < SSA7-0 + SST7-0 ≤ SEA7-0 ≤ SE17-10, if set out of range, Scroll function is disabled

8.2.22. Partial Screen Driving Position (R34h, R35h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
W	1	0	0	0	0	0	0	0	0	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10

SE1[7:0]: Specify the driving end position for the screen in a line unit. The LCD driving is performed to the ‘set value + 1’ gate driver. For example, when SS1[7:0] = 019h and SE1[7:0] = 029h are set, the LCD driving is performed from G26 to G42, and non-display driving is performed for G1 to G25, G43, and others. Ensure that SS1[7:0] ≤ SE1[7:0] ≤DBh.

SS1[7:0]: Specify the drive starting position for the first screen in a line unit. The LCD driving starts from the ‘set value +1’ gate driver.

Note: Do not set the partial setting when the operation is in the normal display condition. Set this register only when in the partial display condition.

Ex) SS1[7:0]=07h and SE1[7:0]=10h are performed from G8 to G17.

8.2.23. Horizontal and Vertical RAM Address Position (R36h/R37h, R38h/R39h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0
W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
W	1	0	0	0	0	0	0	0	0	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0
W	1	0	0	0	0	0	0	0	0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

HSA[7:0]/HEA[7:0] HSA[7:0] and HEA[7:0] represent the respective addresses at the start and end of the window address area in horizontal direction. By setting HSA and HEA bits, it is possible to limit the area on the GRAM horizontally for writing data. The HSA and HEA bits must be set before starting RAM write operation. In setting these bits, be sure “00”h ≤ HSA[7:0]< HEA[7:0] ≤ “AF”h.

VSA[7:0]/VEA[7:0] VSA[7:0] and VEA[7:0] represent the respective addresses at the start and end of the window address area in vertical direction. By setting VSA and VEA bits, it is possible to limit the area on the GRAM vertically for writing data. The VSA and VEA bits must be set before starting RAM write operation. In setting, be sure “00”h ≤ VSA[7:0]< VEA[7:0] ≤ “DB”h.

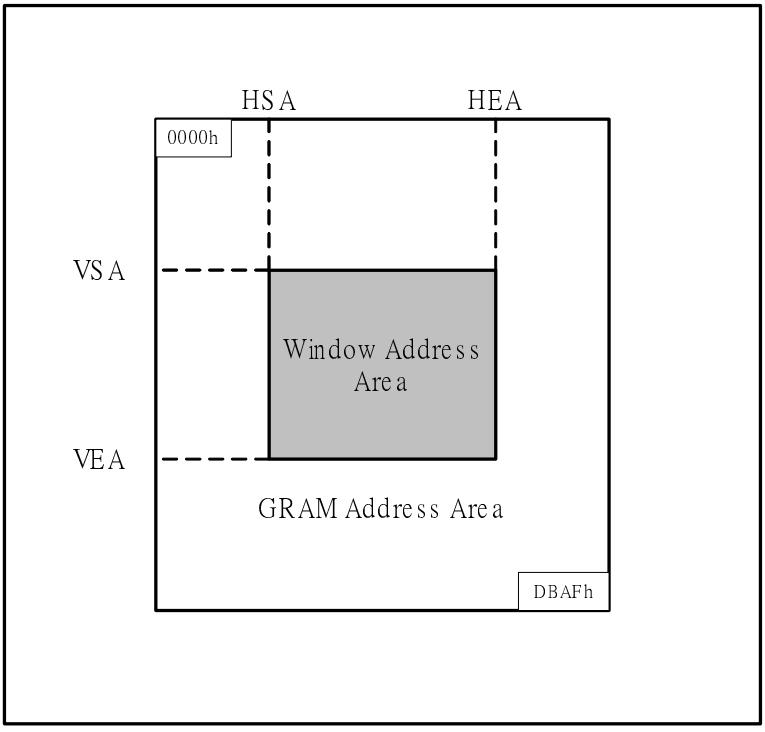


Figure29 GRAM Access Range configuration

“00”h ≤HAS[7:0] ≤HEA[7:0] ≤”AF”h
“00”h ≤VSA[7:0] ≤VEA[7:0] ≤”DB”h

Note1. The window address range must be within the GRAM address space.

Note2. Data are written to GRAM in four-words when operating in high speed mode, the dummy write operations should be inserted depending on the window address area. For details, see the High-Speed RAM Write Function section.

8.2.24. Gamma Control (R50h ~ R59h)

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R50h	W	1	0	0	0	0	KP13	KP12	KP11	KP10	0	0	0	0	KP03	KP02	KP01	KP00
R51h	W	1	0	0	0	0	KP33	KP32	KP31	KP30	0	0	0	0	KP23	KP22	KP21	KP20
R52h	W	1	0	0	0	0	KP53	KP52	KP51	KP50	0	0	0	0	KP43	KP42	KP41	KP40
R53h	W	1	0	0	0	0	RP13	RP12	RP11	RP10	0	0	0	0	RP03	RP02	RP01	RP00
R54h	W	1	0	0	0	0	KN13	KN12	KN11	KN10	0	0	0	0	KN03	KN02	KN01	KN00
R55h	W	1	0	0	0	0	KN33	KN32	KN31	KN30	0	0	0	0	KN23	KN22	KN21	KN20
R56h	W	1	0	0	0	0	KN53	KN52	KN51	KN50	0	0	0	0	KN43	KN42	KN41	KN40
R57h	W	1	0	0	0	0	RN13	RN12	RN11	RN10	0	0	0	0	RN03	RN02	RN01	RN00
R58h	W	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	VRP 04	VRP 03	VRP 02	VRP 01	VRP 00
R59h	W	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	VRN 04	VRN 03	VRN 02	VRN 01	VRN 00

KP53-00: The gamma fine adjustoment register for the positive polarity output

*Initial Value: R50h = 0000

*Initial Value: R51h = 0808

*Initial Value: R52h = 080A

RP13-00: The gradient adjustment register for the positive polarity output.

*Initial Value: R53h = 000A

.

KN53-00: The gamma fine adjustment register for the negative polarity output.

*Initial Value: R54h = 0A08

*Initial Value: R55h = 0808

*Initial Value: R56h = 0000

RN13-00: The gradient adjustment register for the negative polarity output

*Initial Value: R57h= 0A00

VRP14-00: The amplitude adjustment register for the positive polarity output.

*Initial Value: R58h = 0710

VRN14-00: The amplitude adjustment register for the negative polarity output

*Initial Value: R59h = 0710

8.2.25. NV Memory Data Programming (R60h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	NVM_ D7	NVM_ D6	NVM_ D5	NVM_ D4	NVM_ D3	NVM_ D2	NVM_ D1	NVM_ D0

NVM_D[7:0]: NV memory data programming.

8.2.26. NV Memory Control (R61h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	VCM_ SEL	0	0	0	0	0	0	ID_ PGM_EN	VCM_ PGM_EN

VCM_PGM_EN: VCM OTP programming enable. When writing the VCOMH NV memory, the bit must be set as '1'.

ID_PGM_EN: ID OTP programming enable. When writing the ID code NV memory, the bit must be set as '1'.

ID_PGM_EN	VCM_PGM_EN	OTP Programming Selection
0	0	NV Memory programming disabled
0	1	VCM (VCOMH) NV Memory programming enable
1	0	ID code NV Memory programming enable
1	1	Setting Prohibited

VCM_SEL: Select the VCOMH voltage setting.

VCM_SEL	VCM Selection
0	Use the register R14 to adjust the VCOMH voltage (default)
1	Use the NV memory to adjust the VCOMH voltage

Note: When the VCM NV memory had been programmed, the VCM_SEL bit will be set as '1' automatically..

8.2.27. NV Memory Status (R62h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	PGM_ CNT2	PGM_ CNT1	0	0	0	0	0	VCM_ D6	VCM_ D5	VCM_ D4	VCM_ D3	VCM_ D2	VCM_ D1	VCM_ D0

PGM_CNT[1:0]: VCM NV memory programmed record, the NV memory can be programmed 2 times to adjust the VCOMH voltage. These bits are read only.

PGM_CNT[1:0]	Description
00	OTP clean
01	OTP programmed 1 time
10	OTP programmed 2 times

VCM_D[6:0]: OTP VCM data read value. These bits are read only.

8.2.28. NV memory Protection Key (R63h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	KEY 15	KEY 14	KEY 13	KEY 12	KEY 11	KEY 10	KEY 9	KEY 8	KEY 7	KEY 6	KEY 5	KEY 4	KEY 3	KEY 2	KEY 1	KEY 0

KEY[15:0]: NV memory protection key. When programming the NV memory, the KEY[15:0] must set as 0xAA55 value first to make NV memory programming successfully.

8.2.29. ID Code (R65h, Read Only)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	ID3	ID2	ID1	ID0

ID[3:0]: This ID code is stored in the VN memory to record the LCM vender code (read only).

8.2.30. SPI Read/Write Control (R66h, Write Only)

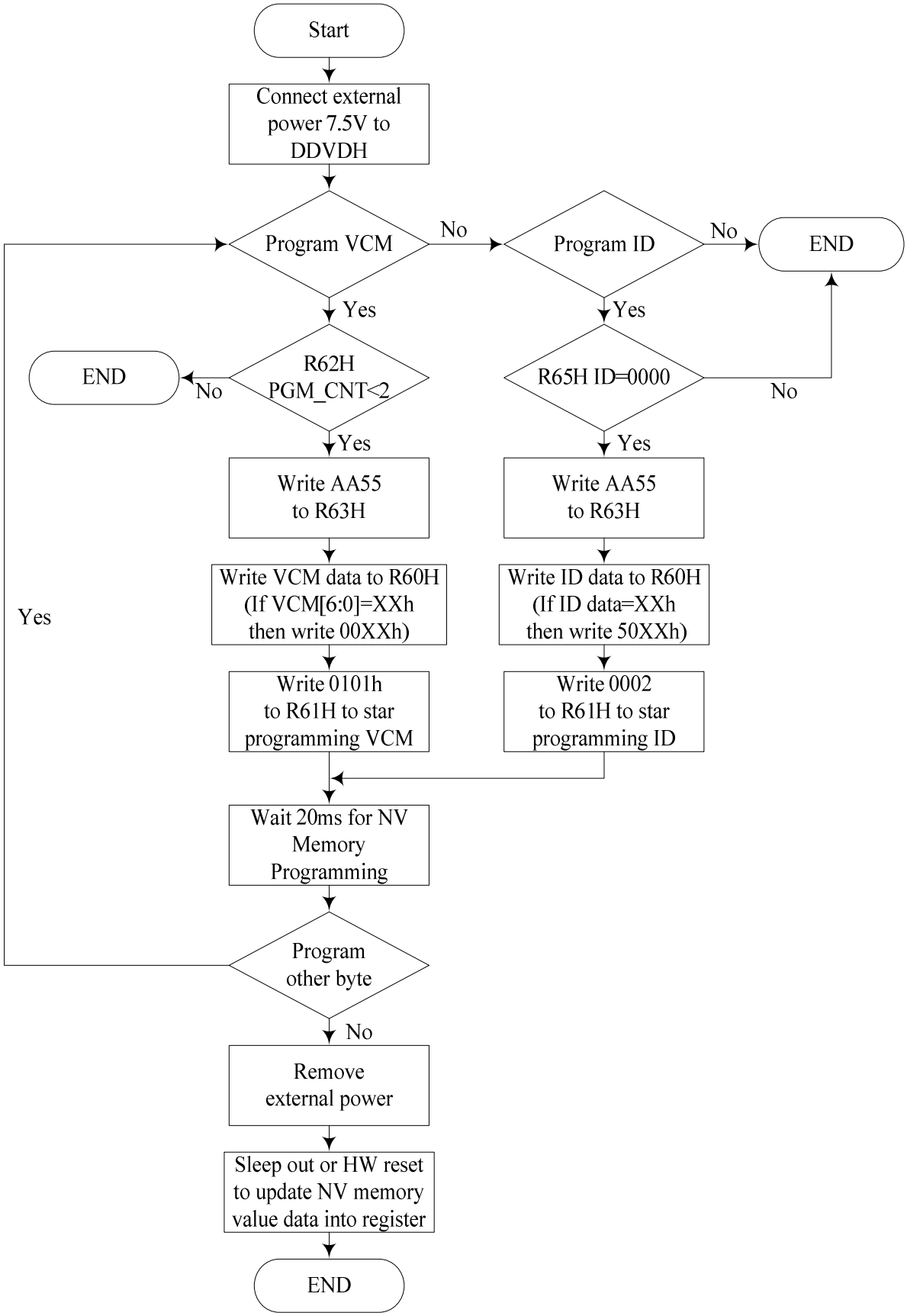
R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/WX

This register is used to control the read/write function of registers when the 8/9-bit serial interface is used.

If users need to read back the register data by the 8/9-bit serial interface, the R/WX bit must be set as '1'.

R/WX	Description
0	Register write mode (default)
1	Register read mode

9. NV Memory Programming Flow



Note: When the VCM NV memory had been programmed, the VCM_SEL bit will be set as "1" automatically.

10. GRAM Address Map & Read/Write

ILI9225G has an internal graphics RAM (GRAM) of 87,120 bytes to store the display data and one pixel is constructed of 18 bits. The GRAM can be accessed through the i80/M68 system, SPI and RGB interfaces.

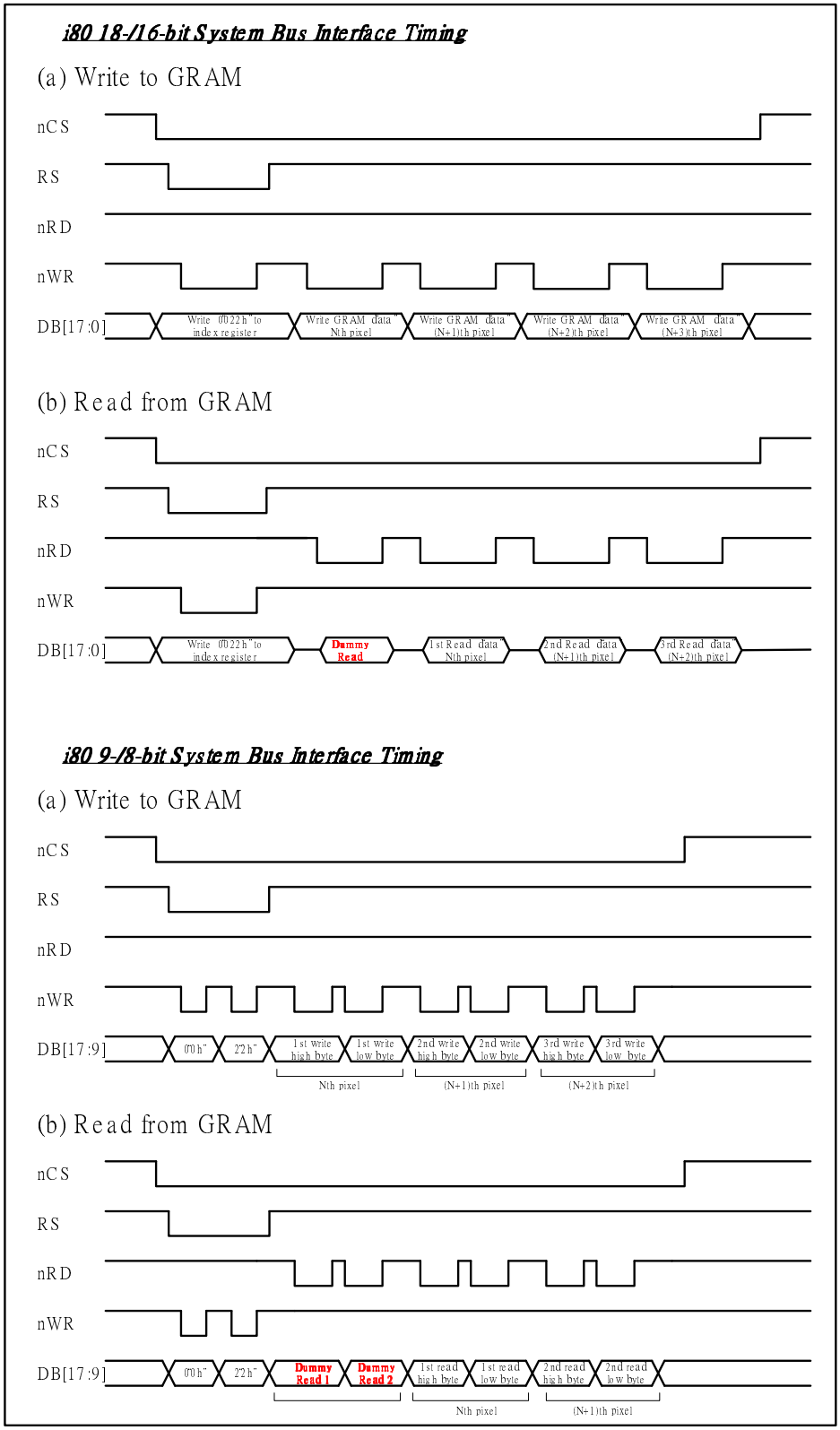


Figure30 GRAM Read/Write Timing of i80-System Interface

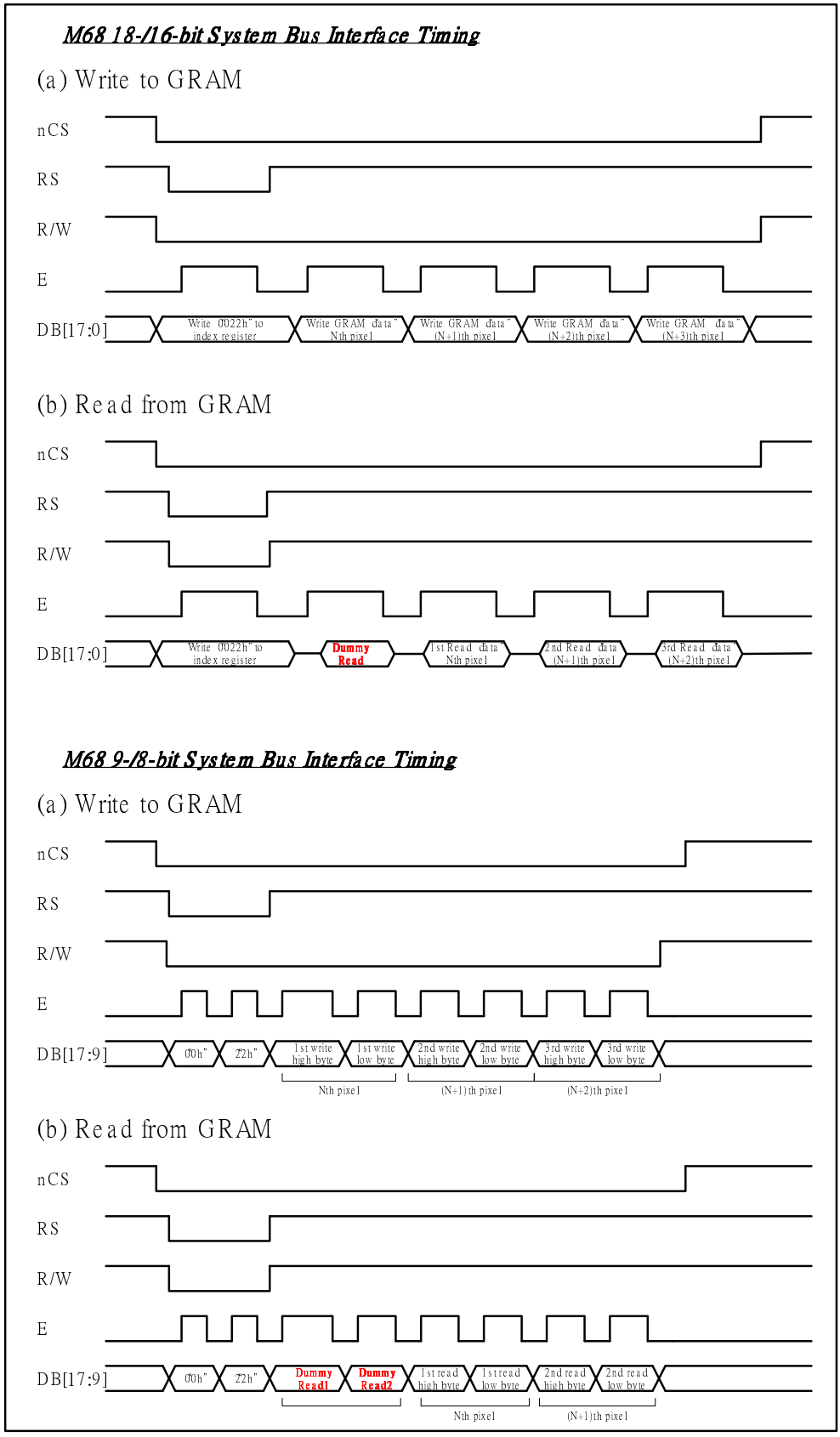


Figure31 GRAM Read/Write Timing of M68-System Interface

GRAM address map table of SS=0, BGR=0

SS=0, BGR=0		S1…S3	S4…S6	S7…S9	S10…S12	…	S517…S519	S520…S522	S523…S525	S526…S528
GS=0	GS=1	DB17…0	DB17…0	DB17…0	DB17…0	…	DB17…0	DB17…0	DB17…0	DB17…0
G1	G220	“0000h”	“0001h”	“0002h”	“0003h”	…	“00Ach”	“00Adh”	“00Aeh”	“00Afh”
G2	G219	“0100h”	“0101h”	“0102h”	“0103h”	…	“01Ach”	“01Adh”	“01Aeh”	“01Afh”
G3	G218	“0200h”	“0201h”	“0202h”	“0203h”	…	“02Ach”	“02Adh”	“02Aeh”	“02Afh”
G4	G217	“0300h”	“0301h”	“0302h”	“0303h”	…	“03Ach”	“03Adh”	“03Aeh”	“03Afh”
G5	G216	“0400h”	“0401h”	“0402h”	“0403h”	…	“04Ach”	“04Adh”	“04Aeh”	“04Afh”
G6	G215	“0500h”	“0501h”	“0502h”	“0503h”	…	“05Ach”	“05Adh”	“05Aeh”	“05Afh”
G7	G214	“0600h”	“0601h”	“0602h”	“0603h”	…	“06Ach”	“06Adh”	“06Aeh”	“06Afh”
G8	G213	“0700h”	“0701h”	“0702h”	“0703h”	…	“07Ach”	“07Adh”	“07Aeh”	“07Afh”
G9	G212	“0800h”	“0801h”	“0802h”	“0803h”	…	“08Ach”	“08Adh”	“08Aeh”	“08Afh”
G10	G211	“0900h”	“0901h”	“0902h”	“0903h”	…	“09Ach”	“09Adh”	“09Aeh”	“09Afh”
. . .	. . .	. . .	. . .	. . .	. . .	…	. . .	. . .	. . .	. . .
G211	G10	“D200h”	“D201h”	“D202h”	“D203h”	…	“D2Ach”	“D2Adh”	“D2Aeh”	“D2Afh”
G212	G9	“D300h”	“D301h”	“D302h”	“D303h”	…	“D3Ach”	“D3Adh”	“D3Aeh”	“D3Afh”
G213	G8	“D400h”	“D401h”	“D402h”	“D403h”	…	“D4Ach”	“D4Adh”	“D4Aeh”	“D4Afh”
G214	G7	“D500h”	“D501h”	“D502h”	“D503h”	…	“D5Ach”	“D5Adh”	“D5Aeh”	“D5Afh”
G215	G6	“D600h”	“D601h”	“D602h”	“D603h”	…	“D6Ach”	“D6Adh”	“D6Aeh”	“D6Afh”
G216	G5	“D700h”	“D701h”	“D702h”	“D703h”	…	“D7Ach”	“D7Adh”	“D7Aeh”	“D7Afh”
G217	G4	“D800h”	“D801h”	“D802h”	“D803h”	…	“D8Ach”	“D8Adh”	“D8Aeh”	“D8Afh”
G218	G3	“D900h”	“D901h”	“D902h”	“D903h”	…	“D9Ach”	“D9Adh”	“D9Aeh”	“D9Afh”
G219	G2	“DA00h”	“DA01h”	“DA02h”	“DA03h”	…	“DAACh”	“DAADh”	“DAAEh”	“DAAFh”
G220	G1	“DB00h”	“DB01h”	“DB02h”	“DB03h”	…	“DBACh”	“DBADh”	“DBAEh”	“DBAFh”

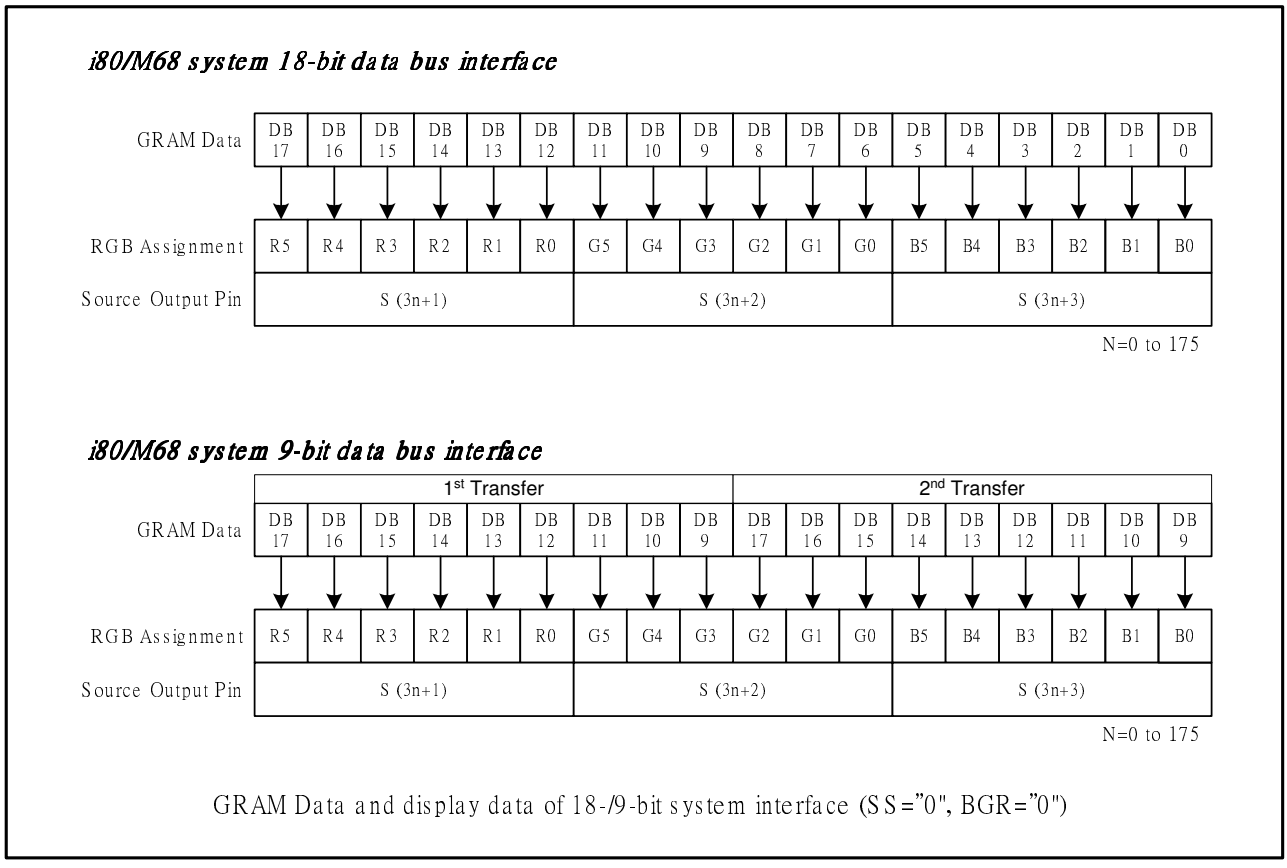


Figure32 i80-System Interface with 18-/9-bit Data Bus (SS=”0”, BGR=”0”)

GRAM address map table of SS=1, BGR=1

SS=1, BGR=1		S1…S3	S4…S6	S7…S9	S10…S12	…	S517…S519	S520…S522	S523…S525	S526…S528
GS=0	GS=1	DB17…0	DB17…0	DB17…0	DB17…0	…	DB17…0	DB17…0	DB17…0	DB17…0
G1	G220	“00Afh”	“00Aeh”	“00Adh”	“00Ach”	…	“0003h”	“0002h”	“0001h”	“0000h”
G2	G219	“01Afh”	“01Aeh”	“01Adh”	“01Ach”	…	“0103h”	“0102h”	“0101h”	“0100h”
G3	G218	“02Afh”	“02Aeh”	“02Adh”	“02Ach”	…	“0203h”	“0202h”	“0201h”	“0200h”
G4	G217	“03Afh”	“03Aeh”	“03Adh”	“03Ach”	…	“0303h”	“0302h”	“0301h”	“0300h”
G5	G216	“04Afh”	“04Aeh”	“04Adh”	“04Ach”	…	“0403h”	“0402h”	“0401h”	“0400h”
G6	G215	“05Afh”	“05Aeh”	“05Adh”	“05Ach”	…	“0503h”	“0502h”	“0501h”	“0500h”
G7	G214	“06Afh”	“06Aeh”	“06Adh”	“06Ach”	…	“0603h”	“0602h”	“0601h”	“0600h”
G8	G213	“07Afh”	“07Aeh”	“07Adh”	“07Ach”	…	“0703h”	“0702h”	“0701h”	“0700h”
G9	G212	“08Afh”	“08Aeh”	“08Adh”	“08Ach”	…	“0803h”	“0802h”	“0801h”	“0800h”
G10	G211	“09Afh”	“09Aeh”	“09Adh”	“09Ach”	…	“0903h”	“0902h”	“0901h”	“0900h”
. . .	. . .	. . .	. . .	. . .	. . .	…	. . .	. . .	. . .	. . .
G211	G10	“D2Afh”	“D2Aeh”	“D2Adh”	“D2Ach”	…	“D203h”	“D202h”	“D201h”	“D200h”
G212	G9	“D3Afh”	“D3Aeh”	“D3Adh”	“D3Ach”	…	“D303h”	“D302h”	“D301h”	“D300h”
G213	G8	“D4Afh”	“D4Aeh”	“D4Adh”	“D4Ach”	…	“D403h”	“D402h”	“D401h”	“D400h”
G214	G7	“D5Afh”	“D5Aeh”	“D5Adh”	“D5Ach”	…	“D503h”	“D502h”	“D501h”	“D500h”
G215	G6	“D6Afh”	“D6Aeh”	“D6Adh”	“D6Ach”	…	“D603h”	“D602h”	“D601h”	“D600h”
G216	G5	“D7Afh”	“D7Aeh”	“D7Adh”	“D7Ach”	…	“D703h”	“D702h”	“D701h”	“D700h”
G217	G4	“D8Afh”	“D8Aeh”	“D8Adh”	“D8Ach”	…	“D803h”	“D802h”	“D801h”	“D800h”
G218	G3	“D9Afh”	“D9Aeh”	“D9Adh”	“D9Ach”	…	“D903h”	“D902h”	“D901h”	“D900h”
G219	G2	“DAAFh”	“DAAEh”	“DAADh”	“DAACh”	…	“DA03h”	“DA02h”	“DA01h”	“DA00h”
G220	G1	“DBAFh”	“DBAEh”	“DBADh”	“DBACh”	…	“DB03h”	“DB02h”	“DB01h”	“DB00h”

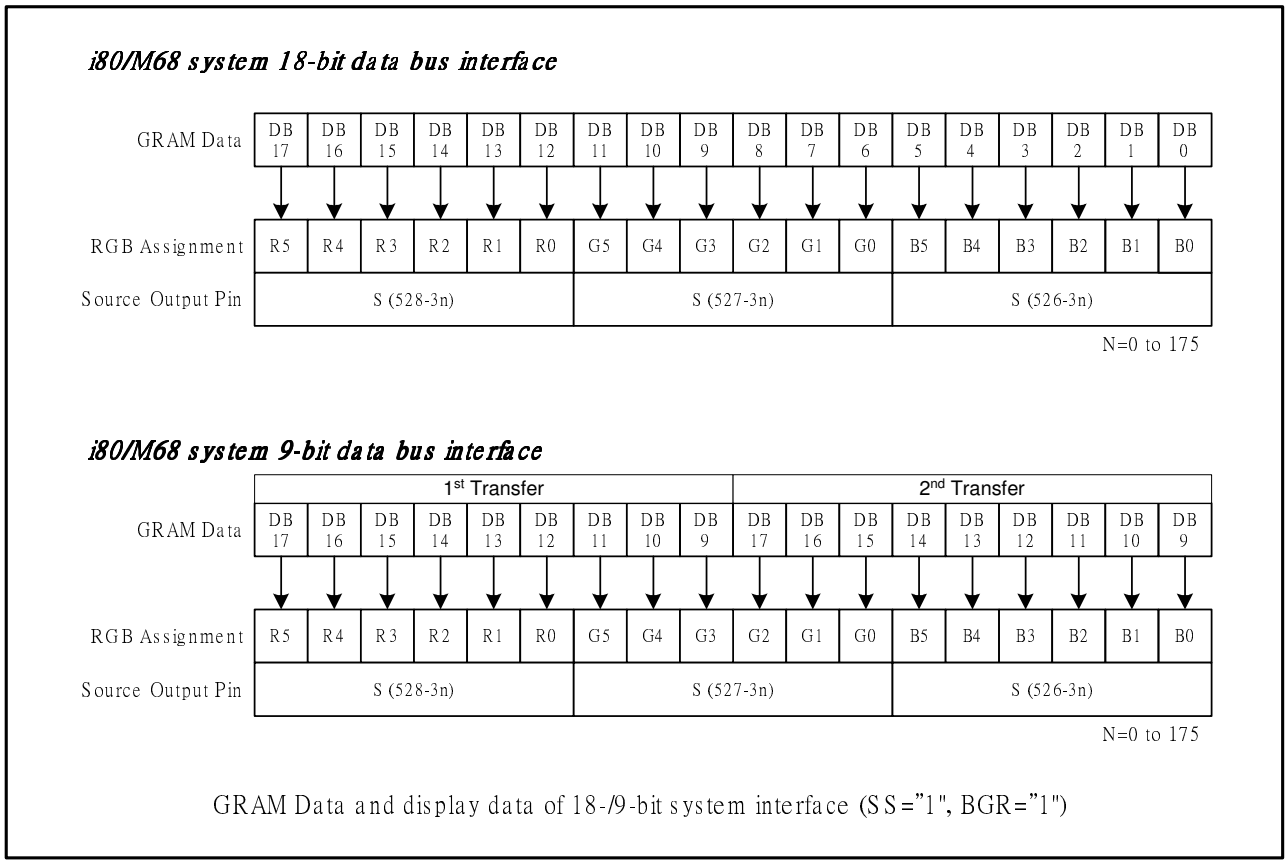


Figure33 i80-System Interface with 18-/9-bit Data Bus (SS=”1”, BGR=”1”)

11. Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made on the internal RAM. The window address area is made by setting the horizontal address register (start: HSA[7:0], end: HEA[7:0] bits) and the vertical address register (start: VSA[7:0], end: VEA[7:0] bits). The AM bit sets the transition direction of RAM address (either increment or decrement). These bits enable the ILI9225G to write data including image data consecutively not taking data wrap positions into account.

The window address area must be made within the GRAM address map area. Also, the AD[15:0] bits (RAM address set register) must be an address within the window address area.

[Window address setting area]

(Horizontal direction) 00H ≤ HSA[7:0] ≤ HEA[7:0] ≤ "AF"H

(Vertical direction) 00H ≤ VSA[7:0] ≤ VEA[7:0]≤ "DB"H

[RAM address, AD[15:0] (an address within a window address area)]]

(RAM address) HSA[7:0] ≤ AD[7:0] ≤ HEA[7:0]

VSA[7:0] ≤ AD[15:8] ≤ VEA[7:0]

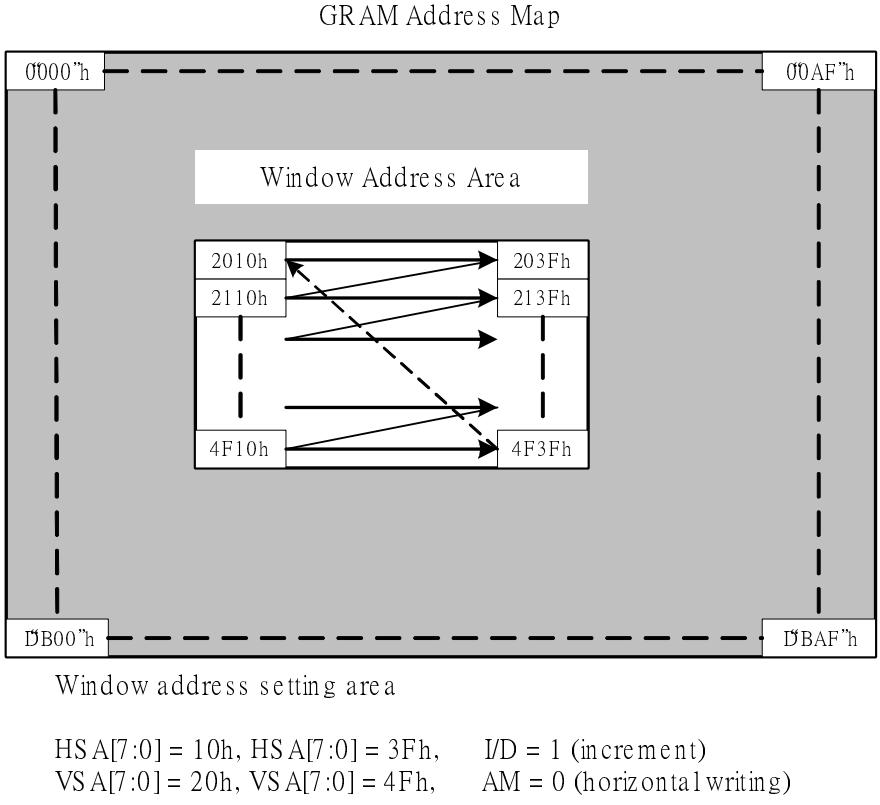


Figure34 GRAM Access Window Map

12. Gamma Correction

ILI9225G incorporates the γ-correction function to display 262,144 colors for the LCD panel. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make ILI9225G available with liquid crystal panels of various characteristics.

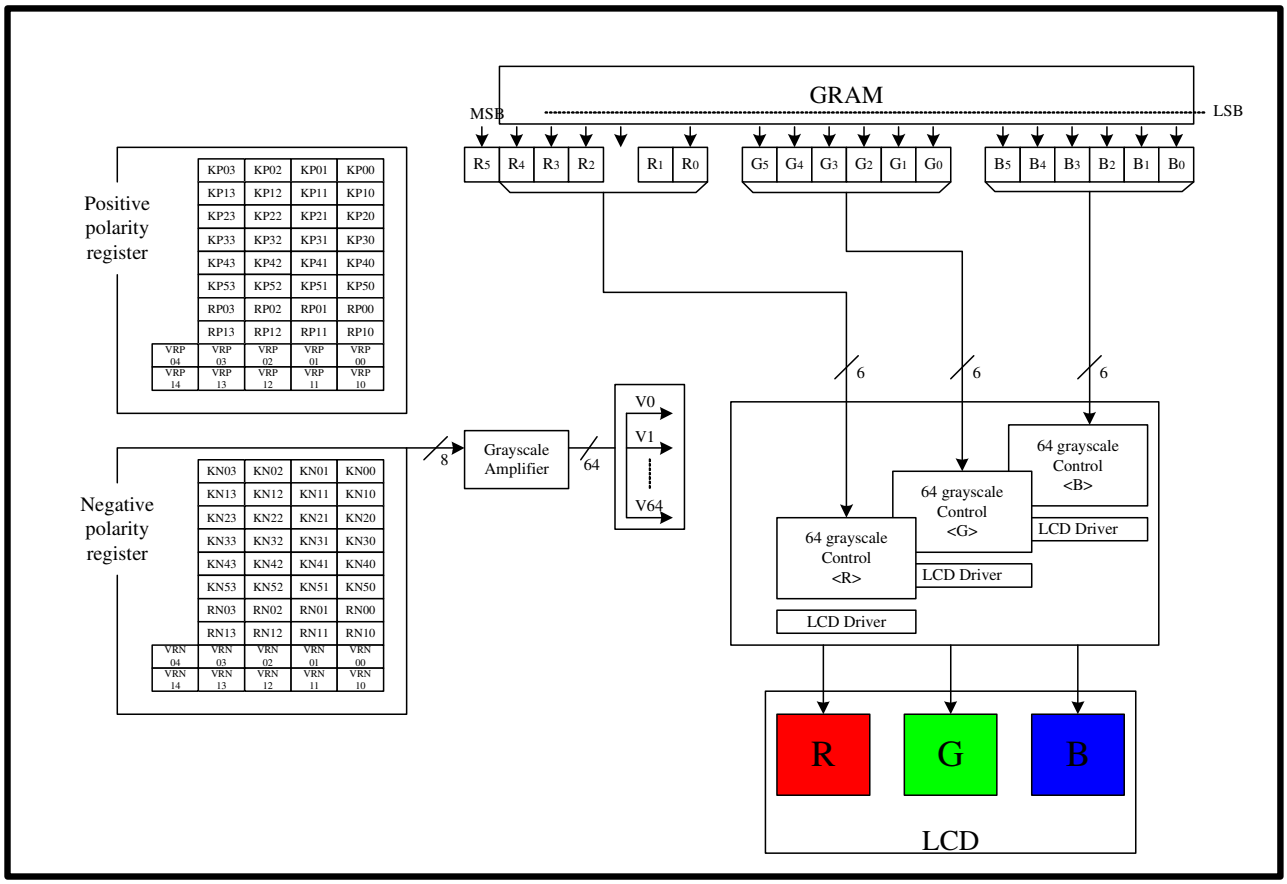


Figure35 Grayscale Mapping

Grayscale Voltage Generator Configuration

The following figure illustrates the grayscale voltage generator function of the ILI9225G. To generate 64 grayscale voltages (V0~V63), ILI9225G first generates eight reference grayscale voltages (VgP/N0, VgP/N1, VgP/N8, VgP/N20, VgP/N43, VgP/N55, VgP/N62, VgP/N63) and the grayscale amplifier unit then divides eight reference grayscale voltages with the ladder resistors incorporated therein. Total 64 grayscale levels are generated from the γ-correction function and used for the LCD source driver.

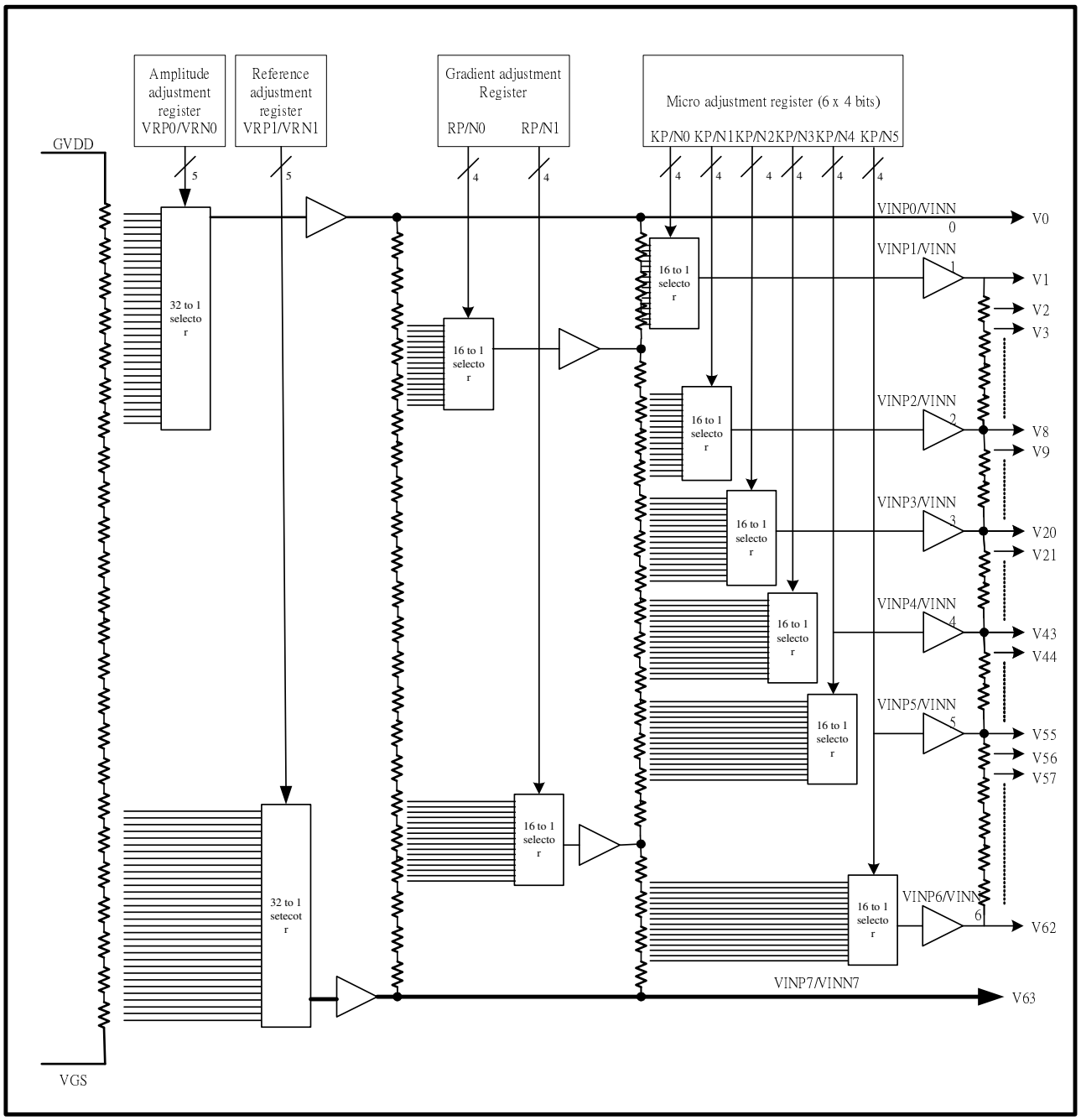


Figure36 Grayscale Voltage Generation

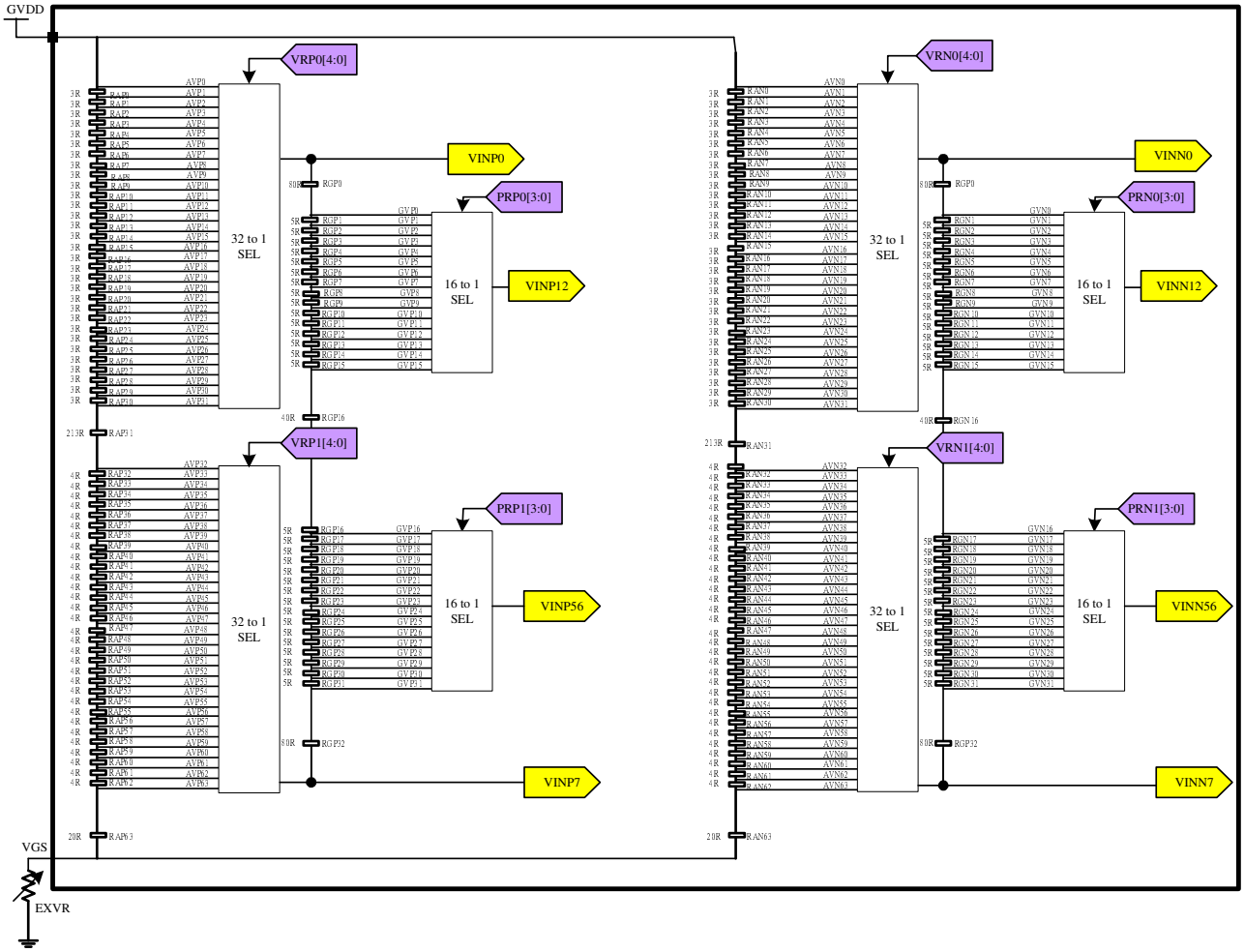


Figure37 Grayscale Voltage Adjustment 1

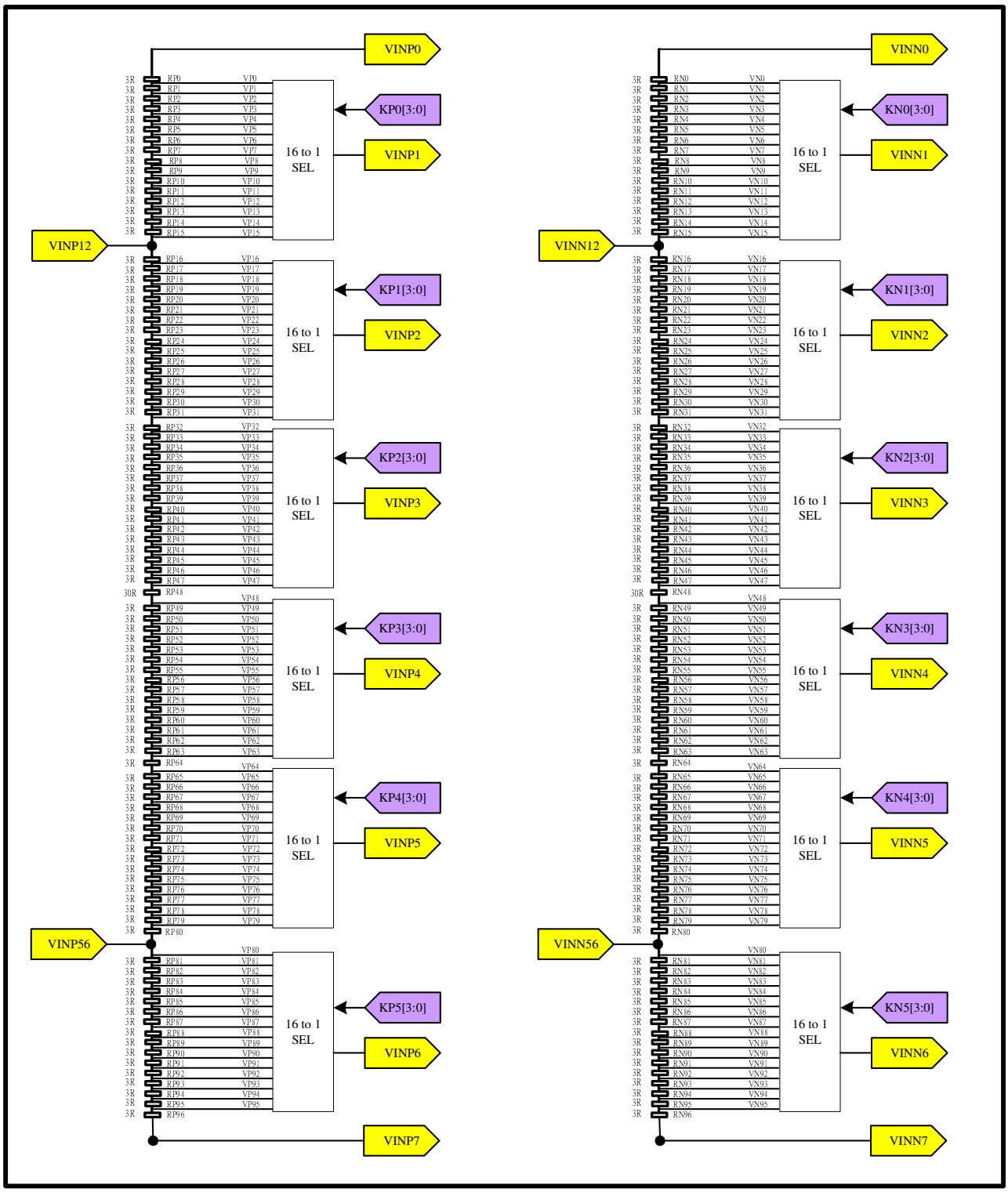


Figure38 Grayscale Voltage Adjustment 2

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale reference voltage level. To accomplish the adjustment, it controls the VINP12/VINN12 and VINP56/VINN56 voltage level by the 16 to 1 selector towards the 16-leveled reference voltage generated from the resistor ladder between VINP0/VINN0 and VINP7/VINN7. Also, there is an independent register on the positive/negative polarities in order for corresponding to asymmetry drive.

2. Reference adjusting register

The Reference adjustment register is to adjust the reference of the grayscale voltage. To accomplish the adjustoment, it controls the VINP7/VINN7 voltage level by 32 to 1 selector towards the 32-leveled voltage generated from the resistor ladder between GVDD and VGS.

3. Amplitude adjustment registers

The Amplitude adjustment register is to adjust the amplitude of the grayscale voltage. To accomplish the adjustment, it controls the VINP0/VINN0 voltage level by 32 to 1 selector towards the 32-leveled reference voltage generated from the resistor ladder between GVDD and VGS.

4. Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 16 levels for each register generated from the ladder resistor, in respective 16-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

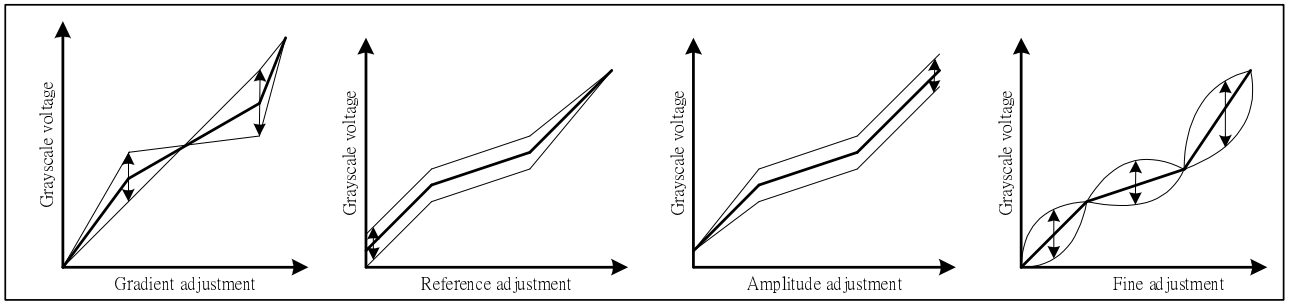


Figure39 Gamma Curve Adjustment

Gamma Adjustment Register

Register	Positive polarity	Negative polarity	Set-up contents
Gradient adjustment	PRP0[3:0]	PRN0[3:0]	The volateg of VINP12/VINN12 is elected by the 16 to 1 selector
	PRP1[3:0]	PRN1[3:0]	The volateg of VINP56/VINN56 is elected by the 16 to 1 selector
Reference adjustment	VRP1[4:0]	VRN11[4:0]	The volateg of VINP7/VINN7 is elected by the 32 to 1 selector
Amplitude adjustment	VRP0[4:0]	VRN0[4:0]	The voltage of VINP0/VINN0 is elected by the 32 to 1 selector
Fine adjustment	PKP0[3:0]	PKN0[3:0]	The voltage of grayscale number 1 is selected by the 16 to 1 selector
	PKP1[3:0]	PKN1[3:0]	The voltage of grayscale number 20 is selected by the 16 to 1 selector
	PKP2[3:0]	PKN2[3:0]	The voltage of grayscale number 43 is selected by the 16 to 1 selector
	PKP3[3:0]	PKN3[3:0]	The voltage of grayscale number 55 is selected by the 16 to 1 selector
	PKP4[3:0]	PKN4[3:0]	The voltage of grayscale number 1 is selected by the 16 to 1 selector
	PKP5[3:0]	PKN5[3:0]	The voltage of grayscale number 62 is selected by the 16 to 1 selector

RESISTOR LADDER NETWORK / SELECTOR

This block outputs the refernce voltage of the grayscale voltage. There are four ladder resistors including the 8 to 1 selector selecting voltage generated by the ladder resistance voltage. Also, there are pins that connect to the external volume resistor. In addition, it allows compensating the dispersion of length between one panel and another.

Resistor ladder network 1 /selector

There are 4 adjustments that are for the gradient adjustment (VRHP(N)/VRLP(N)) and for the reference / amplitude adjustment(VRP(N)1 / VRP(N)0). The voltage level is set by the gradient adjustment register and the reference / amplitude adjustment registers as below.

Amplitude Adjustment

Register value VRP(N)0 [4:0]	Selected voltage VINP(N)0	Formula of VINP(N)0
00000	AVP(N)0	(450R/450R) * (GVDD-VGS) + VGS
00001	AVP(N)1	(447R/450R) * (GVDD-VGS) + VGS
00010	AVP(N)2	(444R/450R) * (GVDD-VGS) + VGS
00011	AVP(N)3	(441R/450R) * (GVDD-VGS) + VGS
00100	AVP(N)4	(438R/450R) * (GVDD-VGS) + VGS
00101	AVP(N)5	(435R/450R) * (GVDD-VGS) + VGS
00110	AVP(N)6	(432R/450R) * (GVDD-VGS) + VGS
00111	AVP(N)7	(429R/450R) * (GVDD-VGS) + VGS
01000	AVP(N)8	(426R/450R) * (GVDD-VGS) + VGS
01001	AVP(N)9	(423R/450R) * (GVDD-VGS) + VGS
01010	AVP(N)10	(420R/450R) * (GVDD-VGS) + VGS
01011	AVP(N)11	(417R/450R) * (GVDD-VGS) + VGS
01100	AVP(N)12	(414R/450R) * (GVDD-VGS) + VGS
01101	AVP(N)13	(411R/450R) * (GVDD-VGS) + VGS
01110	AVP(N)14	(408R/450R) * (GVDD-VGS) + VGS
01111	AVP(N)15	(405R/450R) * (GVDD-VGS) + VGS
10000	AVP(N)16	(402R/450R) * (GVDD-VGS) + VGS
10001	AVP(N)17	(399R/450R) * (GVDD-VGS) + VGS
10010	AVP(N)18	(396R/450R) * (GVDD-VGS) + VGS
10011	AVP(N)19	(393R/450R) * (GVDD-VGS) + VGS
10100	AVP(N)20	(390R/450R) * (GVDD-VGS) + VGS
10101	AVP(N)21	(387R/450R) * (GVDD-VGS) + VGS
10110	AVP(N)22	(384R/450R) * (GVDD-VGS) + VGS
10111	AVP(N)23	(381R/450R) * (GVDD-VGS) + VGS
11000	AVP(N)24	(378R/450R) * (GVDD-VGS) + VGS
11001	AVP(N)25	(375R/450R) * (GVDD-VGS) + VGS
11010	AVP(N)26	(372R/450R) * (GVDD-VGS) + VGS
11011	AVP(N)27	(369R/450R) * (GVDD-VGS) + VGS
11100	AVP(N)28	(366R/450R) * (GVDD-VGS) + VGS
11101	AVP(N)29	(363R/450R) * (GVDD-VGS) + VGS
11110	AVP(N)30	(360R/450R) * (GVDD-VGS) + VGS
11111	AVP(N)31	(357R/450R) * (GVDD-VGS) + VGS

Reference Adjustment

Register value VRP(N)1 [4:0]	Selected voltage VINP(N)7	Formula of VINP(N)7
00000	AVP(N)63	(20R/450R) * (GVDD-VGS) + VGS
00001	AVP(N)62	(24R/450R) * (GVDD-VGS) + VGS
00010	AVP(N)61	(28R/450R) * (GVDD-VGS) + VGS
00011	AVP(N)60	(32R/450R) * (GVDD-VGS) + VGS
00100	AVP(N)59	(36R/450R) * (GVDD-VGS) + VGS
00101	AVP(N)58	(40R/450R) * (GVDD-VGS) + VGS
00110	AVP(N)57	(44R/450R) * (GVDD-VGS) + VGS
00111	AVP(N)56	(48R/450R) * (GVDD-VGS) + VGS
01000	AVP(N)55	(52R/450R) * (GVDD-VGS) + VGS
01001	AVP(N)54	(56R/450R) * (GVDD-VGS) + VGS
01010	AVP(N)53	(60R/450R) * (GVDD-VGS) + VGS
01011	AVP(N)52	(64R/450R) * (GVDD-VGS) + VGS
01100	AVP(N)51	(68R/450R) * (GVDD-VGS) + VGS
01101	AVP(N)50	(72R/450R) * (GVDD-VGS) + VGS
01110	AVP(N)49	(76R/450R) * (GVDD-VGS) + VGS
01111	AVP(N)48	(80R/450R) * (GVDD-VGS) + VGS
10000	AVP(N)47	(84R/450R) * (GVDD-VGS) + VGS
10001	AVP(N)46	(88R/450R) * (GVDD-VGS) + VGS
10010	AVP(N)45	(92R/450R) * (GVDD-VGS) + VGS
10011	AVP(N)44	(96R/450R) * (GVDD-VGS) + VGS
10100	AVP(N)43	(100R/450R) * (GVDD-VGS) + VGS
10101	AVP(N)42	(104R/450R) * (GVDD-VGS) + VGS
10110	AVP(N)41	(108R/450R) * (GVDD-VGS) + VGS
10111	AVP(N)40	(112R/450R) * (GVDD-VGS) + VGS
11000	AVP(N)39	(116R/450R) * (GVDD-VGS) + VGS
11001	AVP(N)38	(120R/450R) * (GVDD-VGS) + VGS
11010	AVP(N)37	(124R/450R) * (GVDD-VGS) + VGS
11011	AVP(N)36	(128R/450R) * (GVDD-VGS) + VGS
11100	AVP(N)35	(132R/450R) * (GVDD-VGS) + VGS
11101	AVP(N)34	(136R/450R) * (GVDD-VGS) + VGS
11110	AVP(N)33	(140R/450R) * (GVDD-VGS) + VGS
11111	AVP(N)32	(144R/450R) * (GVDD-VGS) + VGS

Gradient Adjustment (1)

Register value PRP(N)0 [2:0]	Selected voltage VINP(N)12	Formula of VINP(N)12
0000	GVP(N)0	(270R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0001	GVP(N)1	(265R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0010	GVP(N)2	(260R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0011	GVP(N)3	(255R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0100	GVP(N)4	(250R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0101	GVP(N)5	(245R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0110	GVP(N)6	(240R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0111	GVP(N)7	(235R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1000	GVP(N)8	(230R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1001	GVP(N)9	(225R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1010	GVP(N)10	(220R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1011	GVP(N)11	(215R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1100	GVP(N)12	(210R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1101	GVP(N)13	(205R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1110	GVP(N)14	(200R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1111	GVP(N)15	(195R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7

Reference Adjustment (2)

Register value PRP(N)1 [2:0]	Selected voltage VINP(N)56	Formula of VINP(N)56
0000	GVP(N)0	(80R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0001	GVP(N)1	(85R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0010	GVP(N)2	(90R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0011	GVP(N)3	(95R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0100	GVP(N)4	(100R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0101	GVP(N)5	(105R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0110	GVP(N)6	(110R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
0111	GVP(N)7	(115R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1000	GVP(N)8	(120R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1001	GVP(N)9	(125R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1010	GVP(N)10	(130R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1011	GVP(N)11	(135R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1100	GVP(N)12	(140R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1101	GVP(N)13	(145R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1110	GVP(N)14	(150R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7
1111	GVP(N)15	(155R/350R)*(VINP(N)0-VINP(N)7)+VINP(N)7

Resistor ladder network 2/selector

In the 16-to-1 selector, the voltage level must be selected by the given ladder resistance and the micro-adjustment register and output the six types of the reference volateg, VIN1 to VIN6.

Followin figure explains the relationship between the micro-adjustment register and the selected voltage.

Relationship between Fine-adjustoment Register and Selected Voltage

Register Value PKP(N) [3:0]	Selected Voltage					
	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
0000	KVP(N)0	KVP(N)16	KVP(N)32	KVP(N)63	KVP(N)79	KVP(N)95
0001	KVP(N)1	KVP(N)17	KVP(N)33	KVP(N)62	KVP(N)78	KVP(N)94
0010	KVP(N)2	KVP(N)18	KVP(N)34	KVP(N)61	KVP(N)77	KVP(N)93
0011	KVP(N)3	KVP(N)19	KVP(N)35	KVP(N)60	KVP(N)76	KVP(N)92
0100	KVP(N)4	KVP(N)20	KVP(N)36	KVP(N)59	KVP(N)75	KVP(N)91
0101	KVP(N)5	KVP(N)21	KVP(N)37	KVP(N)58	KVP(N)74	KVP(N)90
0110	KVP(N)6	KVP(N)22	KVP(N)38	KVP(N)57	KVP(N)73	KVP(N)89
0111	KVP(N)7	KVP(N)23	KVP(N)39	KVP(N)56	KVP(N)72	KVP(N)88
1000	KVP(N)8	KVP(N)24	KVP(N)40	KVP(N)55	KVP(N)71	KVP(N)87
1001	KVP(N)9	KVP(N)25	KVP(N)41	KVP(N)54	KVP(N)70	KVP(N)86
1010	KVP(N)10	KVP(N)26	KVP(N)42	KVP(N)53	KVP(N)69	KVP(N)85
1011	KVP(N)11	KVP(N)27	KVP(N)43	KVP(N)52	KVP(N)68	KVP(N)84
1100	KVP(N)12	KVP(N)28	KVP(N)44	KVP(N)51	KVP(N)67	KVP(N)83
1101	KVP(N)13	KVP(N)29	KVP(N)45	KVP(N)50	KVP(N)66	KVP(N)82
1110	KVP(N)14	KVP(N)30	KVP(N)46	KVP(N)49	KVP(N)65	KVP(N)81
1111	KVP(N)15	KVP(N)31	KVP(N)47	KVP(N)48	KVP(N)64	KVP(N)80

[NOTE] The grayscale levels are determined by the following formulas listed in the next pages.

Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 1

Pins	Formula	Micro-adjusting Register value	Reference Voltage
KVP0	(45R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0000”	VINP1
KVP1	(42R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0001”	
KVP2	(39R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0010”	
KVP3	(36R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0011”	
KVP4	(33R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0100”	
KVP5	(30R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0101”	
KVP6	(27R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0110”	
KVP7	(24R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “0111”	
KVP8	(21R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “1000”	
KVP9	(18R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “1001”	
KVP10	(15R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “1010”	
KVP11	(12R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “1011”	
KVP12	(9R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “1100”	
KVP13	(6R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “1101”	
KVP14	(3R/48R) * (VINP0 – VINP12) + VINP12	PKP0[3:0] = “1110”	
KVP15	VINP12	PKP0[3:0] = “1111”	
KVP16	(219R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0000”	VINP2
KVP17	(216R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0001”	
KVP18	(213R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0010”	
KVP19	(210R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0011”	
KVP20	(207R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0100”	
KVP21	(204R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0101”	
KVP22	(201R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0110”	
KVP23	(198R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “0111”	
KVP24	(195R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1000”	
KVP25	(192R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1001”	
KVP26	(189R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1010”	
KVP27	(186R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1011”	
KVP28	(183R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1100”	
KVP29	(180R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1101”	
KVP30	(177R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1110”	
KVP31	(174R/222R) * (VINP12-VINP56) + VINP56	PKP1[3:0] = “1111”	
KVP32	(171R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0000”	VINP3
KVP33	(168R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0001”	
KVP34	(165R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0010”	
KVP35	(162R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0011”	
KVP36	(159R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0100”	
KVP37	(156R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0101”	
KVP38	(153R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0110”	
KVP39	(150R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “0111”	
KVP40	(147R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1000”	
KVP41	(144R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1001”	
KVP42	(141R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1010”	
KVP43	(138R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1011”	
KVP44	(135R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1100”	
KVP45	(132R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1101”	
KVP46	(129R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1110”	
KVP47	(126R/222R) * (VINP12-VINP56) + VINP56	PKP2[3:0] = “1111”	

Pins	Formula	Fine-adjusting register value	Reference voltage
KVP48	(96R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="1111"	VINP4
KVP49	(93R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="1110"	
KVP50	(90R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="1101"	
KVP51	(87R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="1100"	
KVP52	(84R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="1011"	
KVP53	(81R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="1010"	
KVP54	(78R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="1001"	
KVP55	(75R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="1000"	
KVP56	(72R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="0111"	
KVP57	(69R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="0110"	
KVP58	(66R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="0101"	
KVP59	(63R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="0100"	
KVP60	(60R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="0011"	
KVP61	(57R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="0010"	
KVP62	(54R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="0001"	
KVP63	(51R/222R)*(VINP12-VINP56)+VINP56	PKP3[3:0]="0000"	
KVP64	(48R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="1111"	VINP5
KVP65	(45R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="1110"	
KVP66	(42R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="1101"	
KVP67	(39R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="1100"	
KVP68	(36R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="1011"	
KVP69	(33R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="1010"	
KVP70	(30R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="1001"	
KVP71	(27R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="1000"	
KVP72	(24R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="0111"	
KVP73	(21R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="0110"	
KVP74	(18R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="0101"	
KVP75	(15R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="0100"	
KVP76	(12R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="0011"	
KVP77	(9R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="0010"	
KVP78	(6R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="0001"	
KVP79	(3R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]="0000"	
KVP80	VINP56	PKP5[3:0]="1111"	VINP6
KVP81	(45R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="1110"	
KVP82	(42R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="1101"	
KVP83	(39R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="1100"	
KVP84	(36R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="1011"	
KVP85	(33R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="1010"	
KVP86	(30R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="1001"	
KVP87	(27R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="1000"	
KVP88	(24R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="0111"	
KVP89	(21R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="0110"	
KVP90	(18R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="0101"	
KVP91	(15R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="0100"	
KVP92	(12R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="0011"	
KVP93	(9R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="0010"	
KVP94	(6R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="0001"	
KVP95	(3R/48R)*(VINP56-VINP7)+VINP7	PKP5[3:0]="0000"	

Formulas for Calculating Gamma Adjusting Voltage (Positive Polarity) 2

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP0	V32	V20-(V20-V43)*(12/23)
V1	VINP1	V33	V20-(V20-V43)*(13/23)
V2	V1-(V1-V8)*(28/96)	V34	V20-(V20-V43)*(14/23)
V3	V1-(V1-V8)*(42/96)	V35	V20-(V20-V43)*(15/23)
V4	V1-(V1-V8)*(60/96)	V36	V20-(V20-V43)*(16/23)
V5	V1-(V1-V8)*(69/96)	V37	V20-(V20-V43)*(17/23)
V6	V1-(V1-V8)*(78/96)	V38	V20-(V20-V43)*(18/23)
V7	V1-(V1-V8)*(87/96)	V39	V20-(V20-V43)*(19/23)
V8	VINP2	V40	V20-(V20-V43)*(20/23)
V9	V8-(V8-V20)*(2/24)	V41	V20-(V20-V43)*(21/23)
V10	V8-(V8-V20)*(4/24)	V42	V20-(V20-V43)*(22/23)
V11	V8-(V8-V20)*(6/24)	V43	VINP4
V12	V8-(V8-V20)*(8/24)	V44	V43-(V43-V55)*(2/24)
V13	V8-(V8-V20)*(10/24)	V45	V43-(V43-V55)*(4/24)
V14	V8-(V8-V20)*(12/24)	V46	V43-(V43-V55)*(6/24)
V15	V8-(V8-V20)*(14/24)	V47	V43-(V43-V55)*(8/24)
V16	V8-(V8-V20)*(16/24)	V48	V43-(V43-V55)*(10/24)
V17	V8-(V8-V20)*(18/24)	V49	V43-(V43-V55)*(12/24)
V18	V8-(V8-V20)*(20/24)	V50	V43-(V43-V55)*(14/24)
V19	V8-(V8-V20)*(22/24)	V51	V43-(V43-V55)*(16/24)
V20	VINP3	V52	V43-(V43-V55)*(18/24)
V21	V20-(V20-V43)*(1/23)	V53	V43-(V43-V55)*(20/24)
V22	V20-(V20-V43)*(2/23)	V54	V43-(V43-V55)*(22/24)
V23	V20-(V20-V43)*(3/23)	V55	VINP5
V24	V20-(V20-V43)*(4/23)	V56	V55-(V55-V62)*(9/96)
V25	V20-(V20-V43)*(5/23)	V57	V55-(V55-V62)*(18/96)
V26	V20-(V20-V43)*(6/23)	V58	V55-(V55-V62)*(27/96)
V27	V20-(V20-V43)*(7/23)	V59	V55-(V55-V62)*(36/96)
V28	V20-(V20-V43)*(8/23)	V60	V55-(V55-V62)*(45/96)
V29	V20-(V20-V43)*(9/23)	V61	V55-(V55-V62)*(54/96)
V30	V20-(V20-V43)*(10/23)	V62	VINP6
V31	V20-(V20-V43)*(11/23)	V63	VINP7

Formulas for Calculating Gamma Adjusting Voltage (Negative Polarity) 1

Pins	Formula	Micro-adjusting register value	Reference voltage
KVN0	(45R/48R) * (VINP0 – VINN12) + VINN12	PKP0[3:0] = “0000”	VINN1
KVN1	(42R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0001”	
KVN2	(39R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0010”	
KVN3	(36R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0011”	
KVN4	(33R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0100”	
KVN5	(30R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0101”	
KVN6	(27R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0110”	
KVN7	(24R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “0111”	
KVN8	(21R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “1000”	
KVN9	(18R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “1001”	
KVN10	(15R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “1010”	
KVN11	(12R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “1011”	
KVN12	(9R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “1100”	
KVN13	(6R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “1101”	
KVN14	(3R/48R) * (VINN0 – VINN12) + VINN12	PKN0[3:0] = “1110”	
KVN15	VINN12	PKN0[3:0] = “1111”	
KVN16	(219R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0000”	VINN2
KVN17	(216R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0001”	
KVN18	(213R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0010”	
KVN19	(210R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0011”	
KVN20	(207R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0100”	
KVN21	(204R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0101”	
KVN22	(201R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0110”	
KVN23	(198R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “0111”	
KVN24	(195R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1000”	
KVN25	(192R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1001”	
KVN26	(189R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1010”	
KVN27	(186R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1011”	
KVN28	(183R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1100”	
KVN29	(180R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1101”	
KVN30	(177R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1110”	
KVN31	(174R/222R) * (VINN12-VINN56) + VINN56	PKN1[3:0] = “1111”	
KVN32	(171R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0000”	VINN3
KVN33	(168R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0001”	
KVN34	(165R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0010”	
KVN35	(162R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0011”	
KVN36	(159R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0100”	
KVN37	(156R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0101”	
KVN38	(153R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0110”	
KVN39	(150R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “0111”	
KVN40	(147R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1000”	
KVN41	(144R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1001”	
KVN42	(141R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1010”	
KVN43	(138R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1011”	
KVN44	(135R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1100”	
KVN45	(132R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1101”	
KVN46	(129R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1110”	
KVN47	(126R/222R) * (VINN12-VINN56) + VINN56	PKN2[3:0] = “1111”	

Pins	Formula	Fine-adjusting register value	Reference voltage
KVN48	(96R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”1111”	VINN4
KVN49	(93R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”1110”	
KVN50	(90R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”1101”	
KVN51	(87R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”1100”	
KVN52	(84R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”1011”	
KVN53	(81R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”1010”	
KVN54	(78R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”1001”	
KVN55	(75R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”1000”	
KVN56	(72R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”0111”	
KVN57	(69R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”0110”	
KVN58	(66R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”0101”	
KVN59	(63R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”0100”	
KVN60	(60R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”0011”	
KVN61	(57R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”0010”	
KVN62	(54R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”0001”	
KVN63	(51R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”0000”	
KVN64	(48R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”1111”	VINN5
KVN65	(45R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”1110”	
KVN66	(42R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”1101”	
KVN67	(39R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”1100”	
KVN68	(36R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”1011”	
KVN69	(33R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”1010”	
KVN70	(30R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”1001”	
KVN71	(27R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”1000”	
KVN72	(24R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”0111”	
KVN73	(21R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”0110”	
KVN74	(18R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”0101”	
KVN75	(15R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”0100”	
KVN76	(12R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”0011”	
KVN77	(9R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”0010”	
KVN78	(6R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”0001”	
KVN79	(3R/222R)*(VINP12-VINP56)+VINP56	PKP4[3:0]=”0000”	
KVN80	VINP56	PKP4[3:0]=”1111”	VINN6
KVN81	(45R/48R)*(VINP56-VINP7)+VINP7	PKP4[3:0]=”1110”	
KVN82	(42R/48R)*(VINP56-VINP7)+VINP7	PKP4[3:0]=”1101”	
KVN83	(39R/48R)*(VINP56-VINP7)+VINP7	PKP4[3:0]=”1100”	
KVN84	(36R/48R)*(VINP56-VINP7)+VINP7	PKP4[3:0]=”1011”	
KVN85	(33R/48R)*(VINP56-VINP7)+VINP7	PKP4[3:0]=”1010”	
KVN86	(30R/48R)*(VINP56-VINP7)+VINP7	PKP4[3:0]=”1001”	
KVN87	(27R/48R)*(VINP56-VINP7)+VINP7	PKP4[3:0]=”1000”	
KVN88	(24R/48R)*(VINP56-VINP7)+VINP7	PKP4[3:0]=”0111”	
KVN89	(21R/48R)*(VINP56-VINP7)+VINP7	PKP4[3:0]=”0110”	
KVN90	(18R/48R)*(VINP56-VINP7)+VINP7	PKP4[3:0]=”0101”	
KVN91	(15R/48R)*(VINP56-VINP7)+VINP7	PKP4[3:0]=”0100”	
KVN92	(12R/48R)*(VINP56-VINP7)+VINP7	PKP4[3:0]=”0011”	
KVN93	(9R/48R)*(VINP56-VINP7)+VINP7	PKP4[3:0]=”0010”	
KVN94	(6R/48R)*(VINP56-VINP7)+VINP7	PKP4[3:0]=”0001”	
KVN95	(3R/48R)*(VINP56-VINP7)+VINP7	PKP4[3:0]=”0000”	

Formulas for Calculating Gamma Adjusting Voltage (Negative Polarity) 2

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINN0	V32	V20-(V20-V43)*(12/23)
V1	VINN1	V33	V20-(V20-V43)*(13/23)
V2	V1-(V1-V8)*(28/96)	V34	V20-(V20-V43)*(14/23)
V3	V1-(V1-V8)*(42/96)	V35	V20-(V20-V43)*(15/23)
V4	V1-(V1-V8)*(60/96)	V36	V20-(V20-V43)*(16/23)
V5	V1-(V1-V8)*(69/96)	V37	V20-(V20-V43)*(17/23)
V6	V1-(V1-V8)*(78/96)	V38	V20-(V20-V43)*(18/23)
V7	V1-(V1-V8)*(87/96)	V39	V20-(V20-V43)*(19/23)
V8	VINN2	V40	V20-(V20-V43)*(20/23)
V9	V8-(V8-V20)*(2/24)	V41	V20-(V20-V43)*(21/23)
V10	V8-(V8-V20)*(4/24)	V42	V20-(V20-V43)*(22/23)
V11	V8-(V8-V20)*(6/24)	V43	VINN4
V12	V8-(V8-V20)*(8/24)	V44	V43-(V43-V55)*(2/24)
V13	V8-(V8-V20)*(10/24)	V45	V43-(V43-V55)*(4/24)
V14	V8-(V8-V20)*(12/24)	V46	V43-(V43-V55)*(6/24)
V15	V8-(V8-V20)*(14/24)	V47	V43-(V43-V55)*(8/24)
V16	V8-(V8-V20)*(16/24)	V48	V43-(V43-V55)*(10/24)
V17	V8-(V8-V20)*(18/24)	V49	V43-(V43-V55)*(12/24)
V18	V8-(V8-V20)*(20/24)	V50	V43-(V43-V55)*(14/24)
V19	V8-(V8-V20)*(22/24)	V51	V43-(V43-V55)*(16/24)
V20	VINN3	V52	V43-(V43-V55)*(18/24)
V21	V20-(V20-V43)*(1/23)	V53	V43-(V43-V55)*(20/24)
V22	V20-(V20-V43)*(2/23)	V54	V43-(V43-V55)*(22/24)
V23	V20-(V20-V43)*(3/23)	V55	VINN5
V24	V20-(V20-V43)*(4/23)	V56	V55-(V55-V62)*(9/96)
V25	V20-(V20-V43)*(5/23)	V57	V55-(V55-V62)*(18/96)
V26	V20-(V20-V43)*(6/23)	V58	V55-(V55-V62)*(27/96)
V27	V20-(V20-V43)*(7/23)	V59	V55-(V55-V62)*(36/96)
V28	V20-(V20-V43)*(8/23)	V60	V55-(V55-V62)*(45/96)
V29	V20-(V20-V43)*(9/23)	V61	V55-(V55-V62)*(54/96)
V30	V20-(V20-V43)*(10/23)	V62	VINN6
V31	V20-(V20-V43)*(11/23)	V63	VINN7

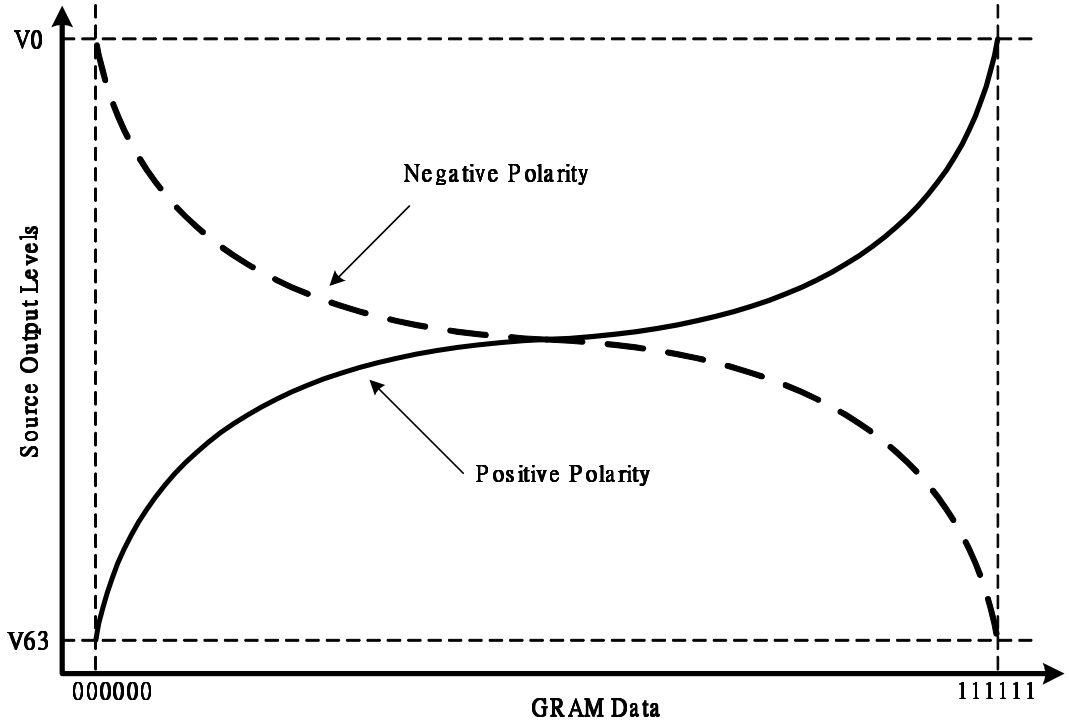


Figure40 Relationship between GRAM Data and Output Level

13. Application

13.1. Configuration of Power Supply Circuit

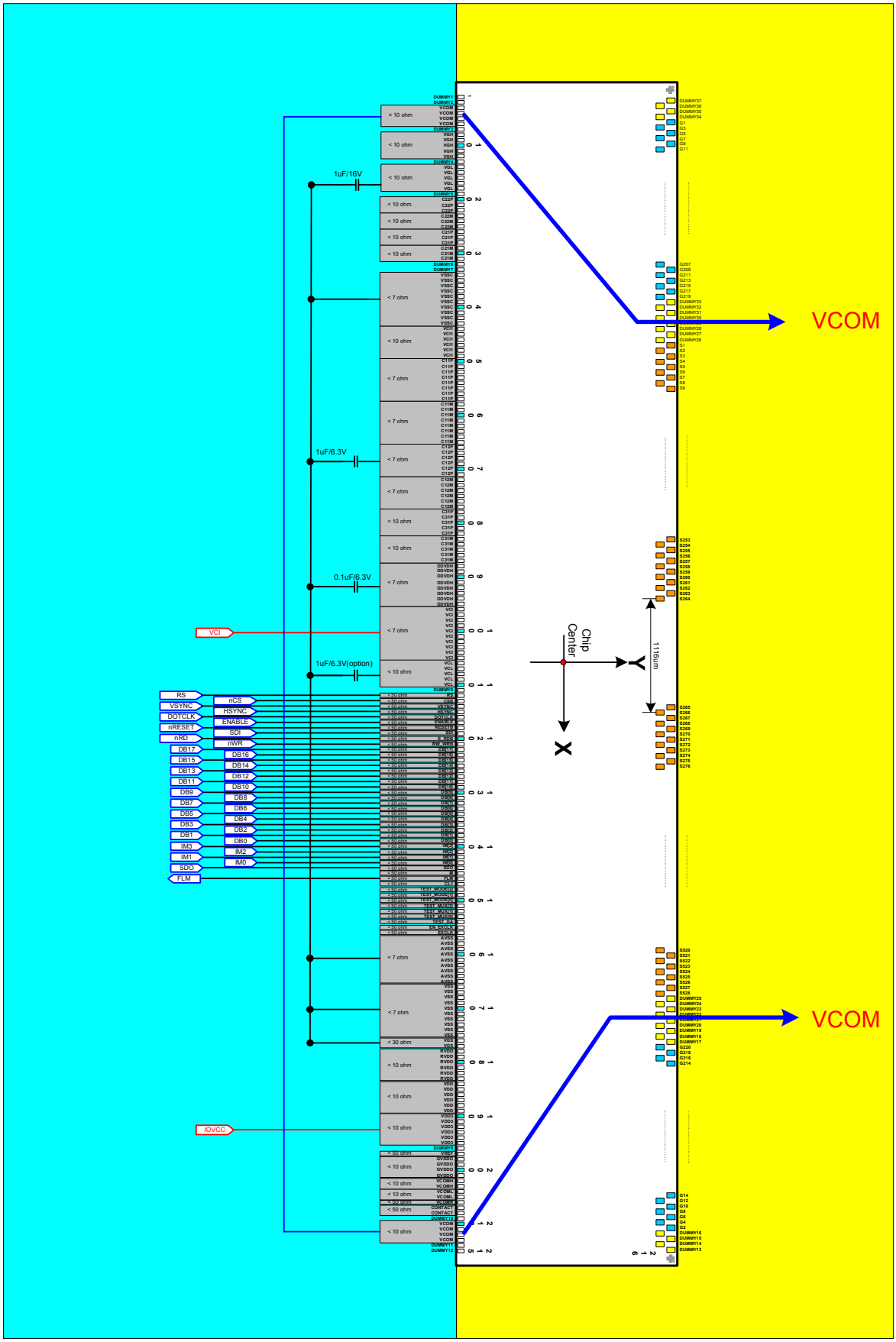


Figure41 Power Supply Circuit Block

The following table shows specifications of external elements connected to the ILI9225G's power supply circuit.

Items	Recommended Specification	Pin connection
Capacity 0.1 µF (B characteristics)	6.3V	AVDD
Capacity 1 µF (B characteristics)	16V	VGL
Capacity 1 µF (B characteristics)	6.3V	VCL(option)
Capacity 1 µF (B characteristics)	6.3V	C12P

13.2. Voltage Generation

The pattern diagram for setting the voltages and the waveforms of the voltages of the ILI9225G are as follows.

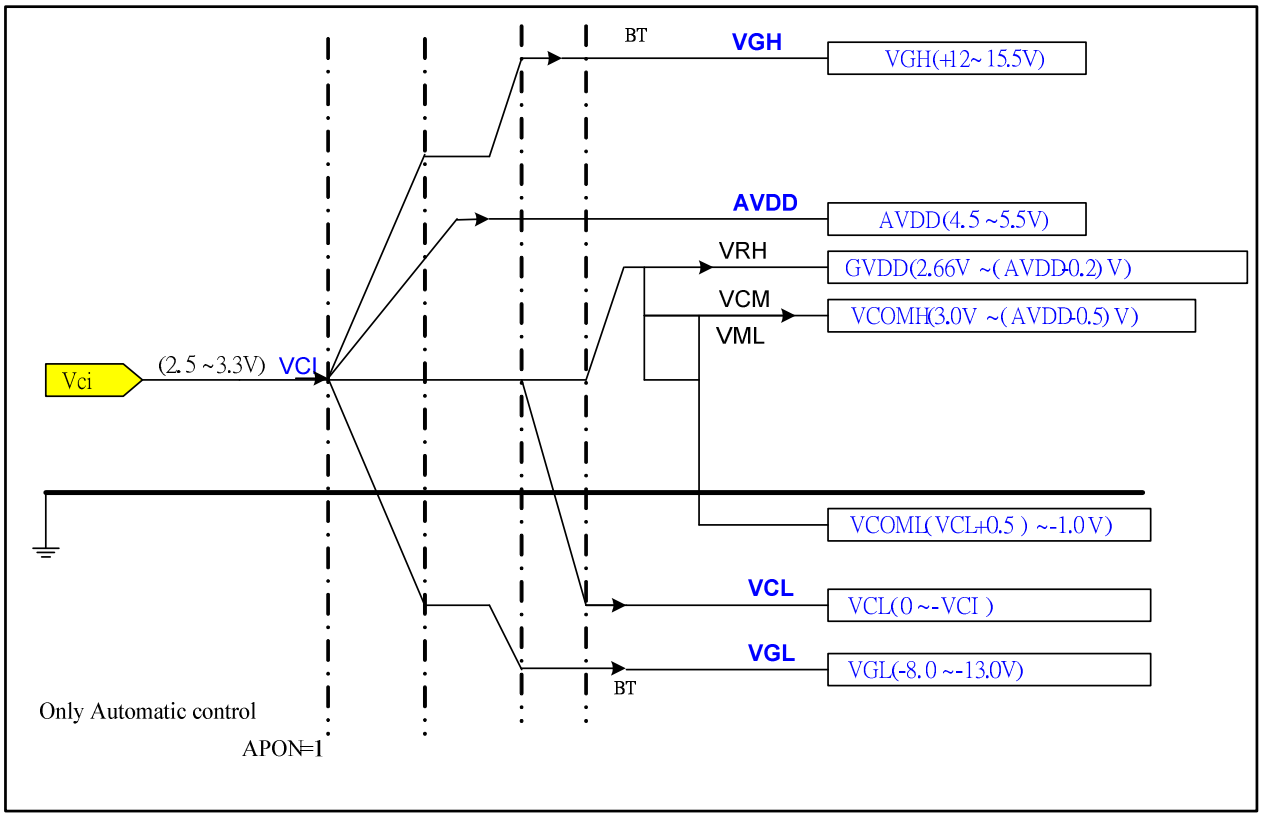


Figure42 Voltage Configuration Diagram

Note: The AVDD, VGH, VGL, and VCL output voltage levels are lower than their theoretical levels (ideal voltage levels) due to current consumption at respective outputs. The voltage levels in the following relationships (AVDD – GVDD) > 0.2V, (VCOML – VCL) > 0.5V are the actual voltage levels. When the alternating cycles of VCOM are set high (e.g. the polarity inverts every line cycle), current consumption is large. In this case, check the voltage before use.

13.3. Power Supply Configuration

When supplying and cutting off power, follow the sequence below. The setting time for step-up circuits and operational amplifiers depends on external resistance and capacitance.

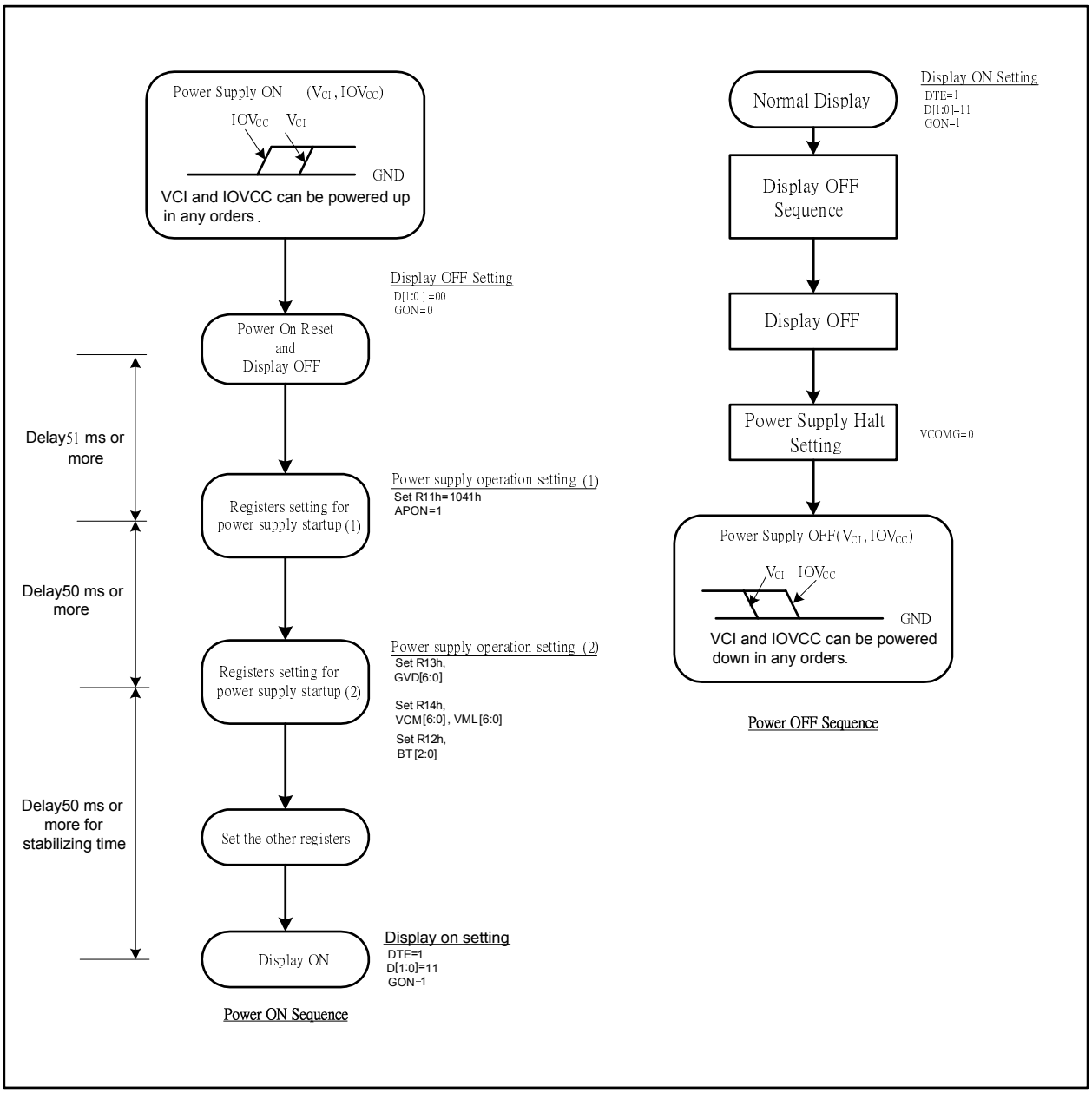


Figure43 Power On/Off Sequence

13.4. STB Mode

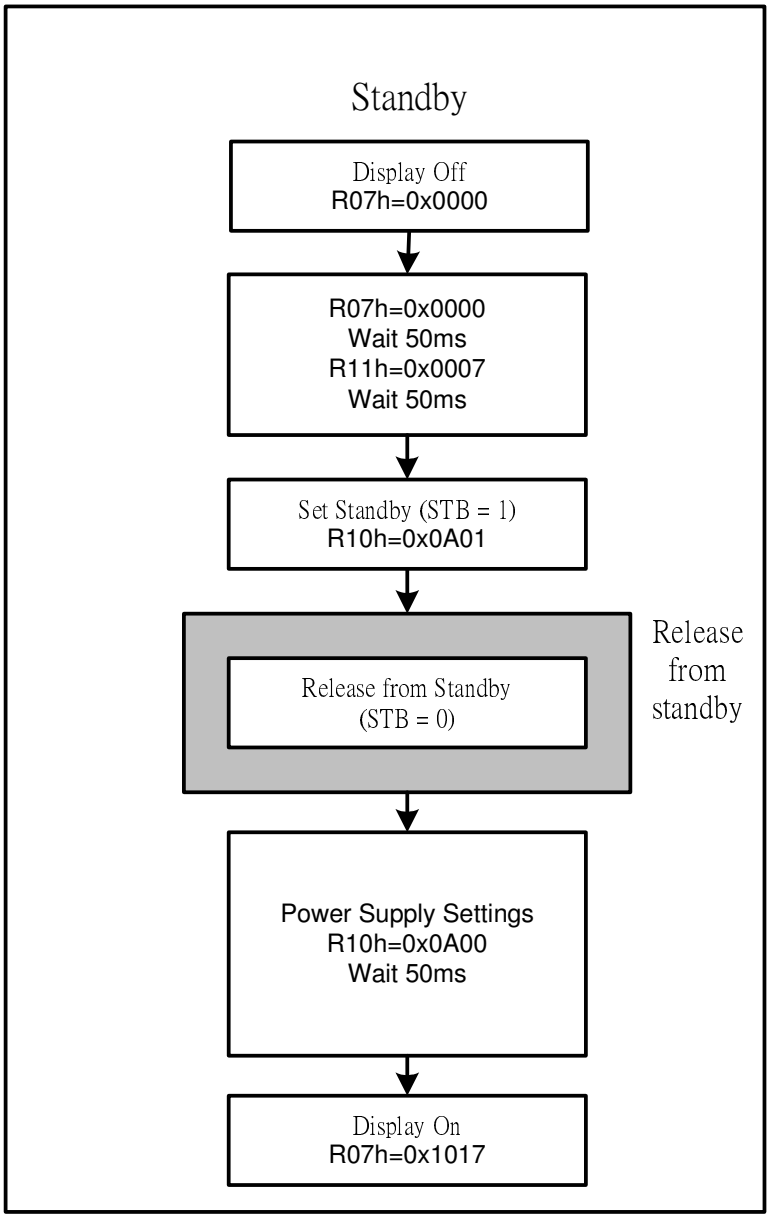


Figure44 STB Mode Register Setting Sequence

14. Electrical Characteristics

14.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9225G is used out of the absolute maximum ratings, the ILI9225G may be permanently damaged. To use the ILI9225G within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9225G will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power supply voltage (1)	IOVCC	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (1)	VCI – GND	V	-0.3 ~ + 4.6	1, 4
Power supply voltage (1)	AVDD – GND	V	-0.3 ~ + 6.0	1, 4
Power supply voltage (1)	GND –VCL	V	-0.3 ~ + 4.6	1
Power supply voltage (1)	AVDD – VCL	V	-0.3 ~ + 9.0	1, 5
Power supply voltage (1)	VGH – GND	V	-0.3 ~ + 18.5	1, 5
Power supply voltage (1)	GND – VGL	V	-0.3 ~ + 18.5	1, 6
Input voltage	Vt	V	-0.3 ~ VCI+ 0.3	1
Operating temperature	Topr	℃	-40 ~ + 85	8, 9
Storage temperature	Tstg	℃	-55 ~ + 110	8, 9

Notes:
1. VCI,GND must be maintained
2. (High) VCI ≥ GND (Low), (High) IOVCC ≥ GND (Low).
3. Make sure (High) VCI ≥ GND (Low).
4. Make sure (High) AVDD ≥ ASSD (Low).
5. Make sure (High) AVDD ≥ VCL (Low).
6. Make sure (High) VGH ≥ ASSD (Low).
7. Make sure (High) ASSD ≥ VGL (Low).
8. For die and wafer products, specified up to 85℃.
9. This temperature specifications apply to the TCP package

14.2. DC Characteristics

(VCI = 2.50 ~ 3.30V, IOVCC = 1.65 ~ 3.30V, Ta= -40 ~ 85 ℃)

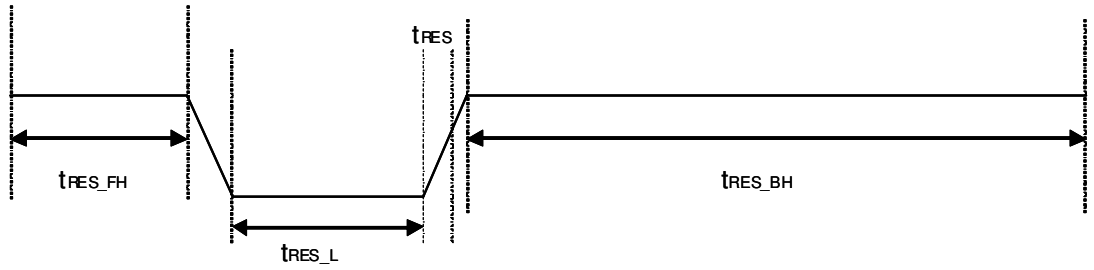
Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V_{IH}	V	IOVCC= 1.65 ~ 3.3V	0.8*IOVCC	-	IOVCC	-
Input low voltage	V_{IL}	V	IOVCC= 1.65 ~ 3.3V	0	-	0.2*IOVCC	-
Output high voltage(1) (DB0-17 Pins)	V_{OH1}	V	IOH = -0.1 mA	0.8*IOVCC	-	-	-
Output low voltage (DB0-17 Pins)	V_{OL1}	V	IOVCC=1.65~3.3V VCI= 2.5 ~ 3.3V IOL = 0.1mA	-	-	0.2*IOVCC	-
I/O leakage current	I_{LI}	µA	Vin = 0 ~ IOVCC	-0.1	-	0.1	-
Current consumption during standby mode (VCI – GND)	I_{ST}	µA	VCI=2.8V , Ta=25 ℃	-	-	100	-
LCD Driving Voltage (AVDD-GND)	AVDD	V	-	4.5	-	6	-
Output voltage deviation		mV	-	-	20	-	-
Dispersion of the Average Output Voltage	V	mV	-	-20	-	20	-

14.3. Reset Timing Characteristics

Reset Timing Charateristics (IOVCC = 1.65 ~ 3.3V)

Item	Symbol	Unit	Min.	Typ.	Max
Reset front high-levelwith	t_{RES_FH}	**ms**	**1**		
Reset low-level width	t_{RES_L}	**us**	**10**		
Reset back high-level width	t_{RES_BH}	**ms**	**50**		
Reset rise time	t_{rRES}	**us**			**10**

nRESET



14.4. AC Characteristics

14.4.1. i80-System Interface Timing Characteristics

Normal Write Mode (IOVCC = 1.65~3.3V, VCI=2.5~3.3V)

Item		Symbol	Unit	Min.	Max.	Test Condition
Bus cycle time	Write	t_{CYCW}	ns	66	-	-
	Read	t_{CYCR}	ns	300	-	-
Write low-level pulse width		PW_{LW}	ns	35	500	-
Write high-level pulse width		PW_{HW}	ns	35	-	-
Read low-level pulse width		PW_{LR}	ns	150	-	-
Read high-level pulse width		PW_{HR}	ns	150	-	
Write / Read rise / fall time		t_{WRr}/t_{WRf}	ns	-	15	
Setup time	Write (RS to nCS, E/nWR)	t_{AS}	ns	10	-	
	Read (RS to nCS, RW/nRD)			5	-	
Address hold time		t_{AH}	ns	5	-	
Write data set up time		t_{DSW}	ns	10	-	
Write data hold time		t_H	ns	15	-	
Read data delay time		t_{DDR}	ns	-	100	
Read data hold time		t_{DHR}	ns	5	-	

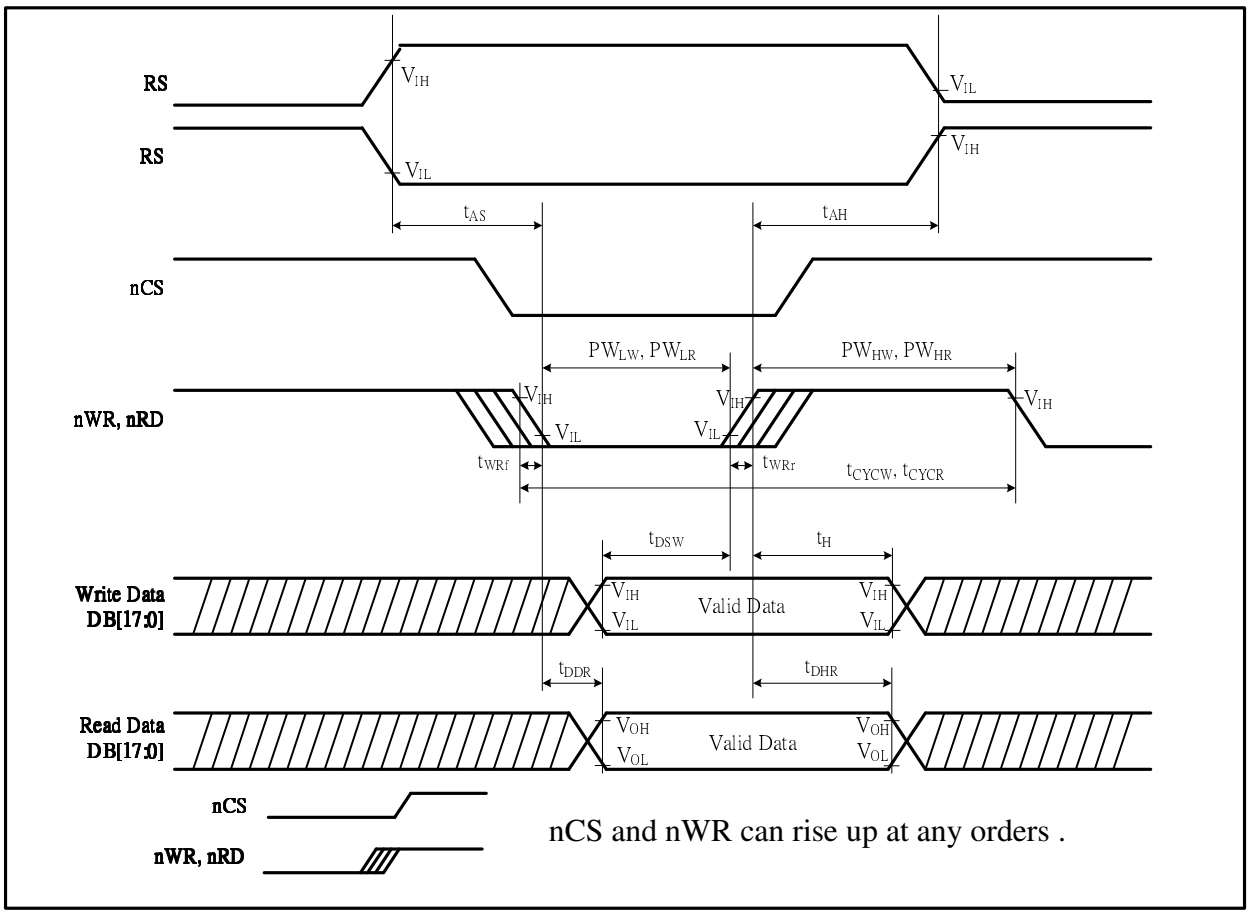


Figure45 i80-System Bus Timing

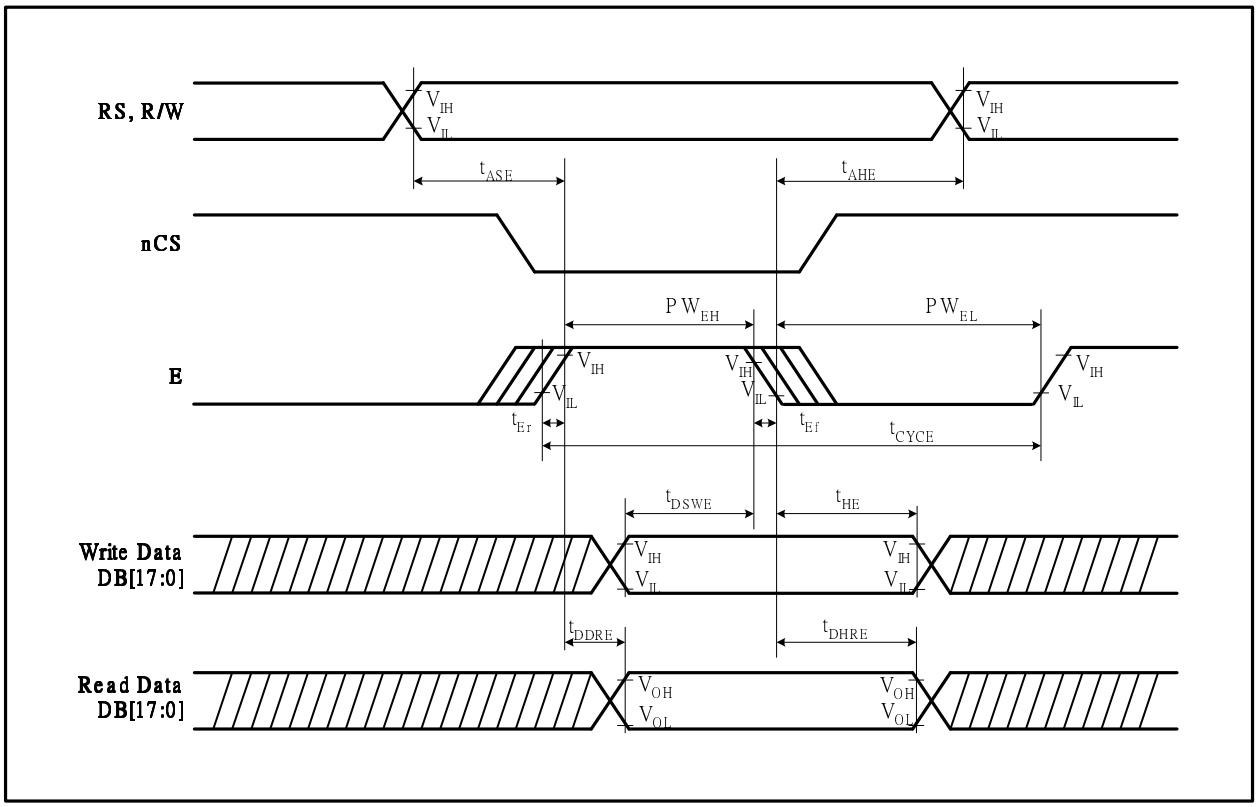


Figure46 M68-System Bus Timing

14.4.2. M68-System Interface Timing Characteristics

Normal Write Mode (IOVCC = 1.65~3.3V, VCI=2.5~3.3V)

Item		Symbol	Unit	Min.	Max.	Test Condition
Bus cycle time	Write	t_{CYCEW}	ns	66	-	-
	Read	t_{CYCER}	ns	300	-	-
Write low-level pulse width		PW_{ELW}	ns	35	500	-
Write high-level pulse width		PW_{EHW}	ns	35	-	-
Read low-level pulse width		PW_{ELR}	ns	150	-	-
Read high-level pulse width		PW_{EHR}	ns	150	-	
Write / Read rise / fall time		t_{WRr}/t_{WRf}	ns	-	15	
Setup time	Write (RS to nCS, E/nWR)	t_{ASE}	ns	10	-	
	Read (RS to nCS, RW/nRD)			10	-	
Address hold time		t_{AHE}	ns	5	-	
Write data set up time		t_{DSWE}	ns	10	-	
Write data hold time		t_{HE}	ns	15	-	
Read data delay time		t_{DDRE}	ns	-	100	
Read data hold time		t_{DHRE}	ns	5	-	

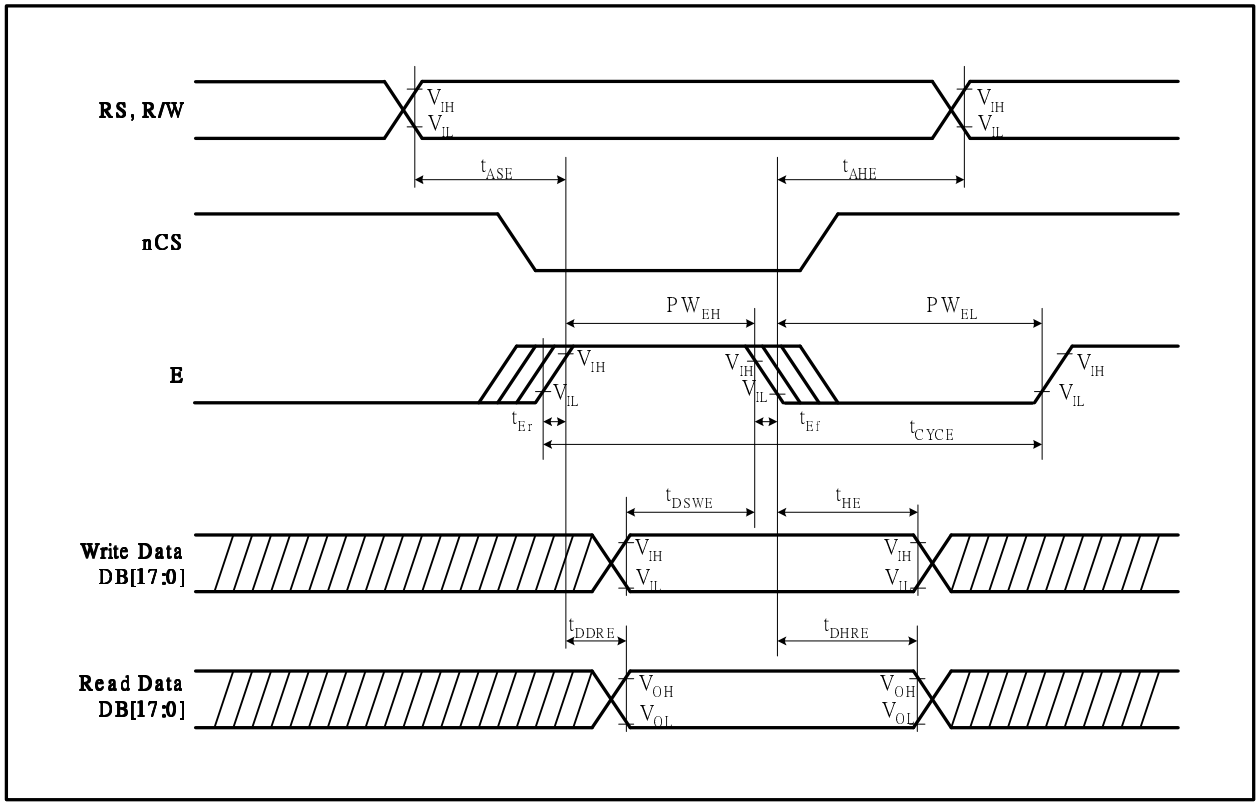


Figure47 M68-System Interface Timing

14.4.3. Serial Data Transfer Interface Timing Characteristics

(IOVCC= 1.65~3.3V and VCI=2.5~3.3V)

Item		Symbol	Unit	Min.	Max.	Test Condition
Serial clock cycle time	Write (received)	t_{SCYC}	ns	80	-	IOVCC=1.65~2.8V
	Write (received)	t_{SCYC}	ns	25		IOVCC=2.8~3.3V
	Read (transmitted)	t_{SCYC}	ns	200	-	
Serial clock high – level pulse width	Write (received)	t_{SCH}	ns	40	-	IOVCC=1.65~3.3V
	Read (transmitted)	t_{SCH}	ns	90	-	
Serial clock low – level pulse width	Write (received)	t_{SCL}	ns	40	-	IOVCC=1.65~3.3V
	Read (transmitted)	t_{SCL}	ns	90	-	
Serial clock rise / fall time		t_{SCr}, t_{SCf}	ns	-	5	
Chip select set up time		t_{CSU}	ns	10	-	
Chip select hold time		t_{CH}	ns	10	-	
Serial input data set up time		t_{SISU}	ns	5	-	
Serial input data hold time		t_{SIH}	ns	5	-	
Serial output data set up time		t_{SOD}	ns	-	200	
Serial output data hold time		t_{SOH}	ns	10	-	

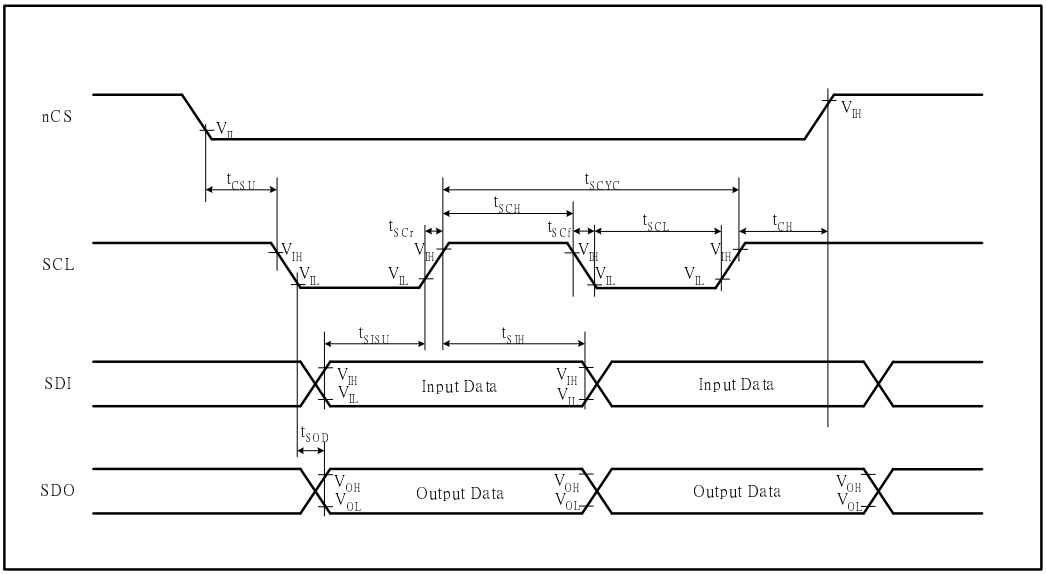


Figure48 SPI System Bus Timing

14.4.4. RGB Interface Timing Characteristics

18/16-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V, VCI=2.5~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	20	-	-	-
ENABLE hold time	t_{ENH}	ns	30	-	-	-
PD Data setup time	t_{PDS}	ns	20	-	-	-
PD Data hold time	t_{PDH}	ns	40	-	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	100	-	-	Frame rate umder 100Hz
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr}, t_{rghf}	ns	-	-	25	-

6-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V, VCI=2.5~3.3V)

Item	Symbol	Unit	Min.	Typ.	Max.	Test Condition
VSYNC/HSYNC setup time	t_{SYNCS}	ns	0	-	-	-
ENABLE setup time	t_{ENS}	ns	20	-	-	-
ENABLE hold time	t_{ENH}	ns	30	-	-	-
PD Data setup time	t_{PDS}	ns	20	-	-	-
PD Data hold time	t_{PDH}	ns	40	-	-	-
DOTCLK high-level pulse width	PWDH	ns	40	-	-	-
DOTCLK low-level pulse width	PWDL	ns	40	-	-	-
DOTCLK cycle time	t_{CYCD}	ns	100	-	-	Frame rate umder 100Hz
DOTCLK, VSYNC, HSYNC, rise/fall time	t_{rghr}, t_{rghf}	ns	-	-	25	-

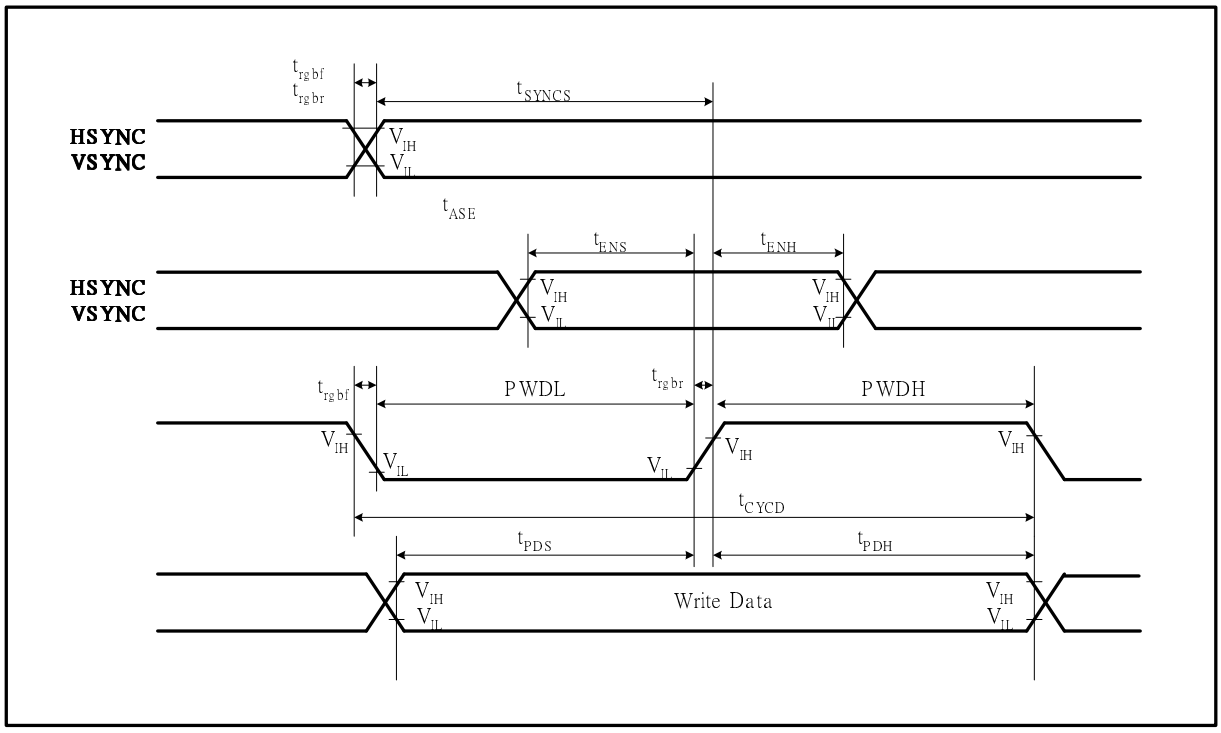


Figure49 RGB Interface Timing

Revision History

Version No.	Date	Page	Description
V0.01	2010/11/15	All	New created.
V0.02	2011/01/05	1~2	Modify index
V0.03	2011/01/07	104	Update external Cap. List
V0.04	2011/01/12	103	Update external Cap. List
V0.05	2011/01/19	109	Modify DC characteristics
V0.06	2011/02/28	53,56,103,104	Update ID code and external Cap.