

Amorphous TFT LCD Single-Chip Driver 800(RGB) x 1280 Resolution, 16.7M-color Without Internal GRAM

Specification

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1. Introduction

The ILI9881C-04 is a 16.7M single-chip (SOC) driver. It is comprised of a 2404-channel source driver (S1~S2400 and SDUM[3:0]), a gate-IC-less level shifter and a power supply circuit to drive a dot-matrix TFT LCD with 800 (RGB) x 1280 dots at maximum.

The ILI9881C-04 can configure functions via the MIPI¹ DSI² Interface; transmit video data via MIPI DSI Interface. The ILI9881C-04 supports three kinds of data types, i.e., 16-bit, 18-bit and 24-bit, for video image display in MIPI DSI interfaces. In the MIPI DSI high-speed mode, the ILI9881C-04 also provides three user-selectable hardware structures:

- ❖ Two data lane supports up to 850Mbps on the MIPI DSI link
- ❖ Three data lanes support up to 750Mbps on the MIPI DSI link
- ❖ Four data lanes support up to 650Mbps on the MIPI DSI link

The ILI9881C-04 can operate with 1.65V I/O interface voltage and supports a wide range of analog power supplies. The ILI9881C-04 supports 8 colors (Idle Mode: 8-color low power mode) display and sleep mode power management functions, ideal for portable products where battery power conservation is desirable, such as digital cellular phones, smart phones, MP3 players, personal media players and similar devices with color graphics displays.

¹ MIPI: Mobile Industry Processor Interface

² DSI: Display Serial Interface

2. Features

- ◆ Display resolution options:
 - 800 (RGB) (H) x (1024(option) + 480 + (4 x NL) +2(option))(V)
 - 768 (RGB) (H) x (1024(option) + 480 + (4 x NL) +2(option))(V)
 - 720 (RGB) (H) x (1024(option) + 480 + (4 x NL) +2(option))(V)
 - 640 (RGB) (H) x (1024(option) + 480 + (4 x NL) +2(option))(V)

- ◆ Display color modes
 - Full color mode:
 - 16.7M colors (24-bit data, R: 8-bit, G: 8-bit, B: 8-bit)
 - Reduced color modes:
 - 262K colors (18-bit data, R: 6-bit, G: 6-bit, B: 6-bit)
 - 65K colors (16-bit data, R: 5-bit, G: 6-bit, B: 5-bit)

- ◆ Display module:
 - Supports 2404 source channel outputs (S1~S2400 and SDUM[3:0])
 - Supports gate control signals to gate driver in the panel
 - Supports 1-dot , 2-dot , 4-dot , N/4-dot , N/8-dot , N/16-dot , N/32-dot , column , Zig-Zag inversion
 - Gamma correction (1 preset Gamma curve)
 - On module VCOM control

- ◆ Display interface types:
 - DSI interface (DSI version 1.01 and D-PHY version 1.00):
 - 2 data lane / maximum speed 850Mbps
 - 3 data lanes / maximum speed 750Mbps
 - 4 data lanes / maximum speed 650Mbps

- ◆ Power saving modes:
 - Sleep mode

- ◆ Other on-chip functions/Miscellaneous
 - Software programmable color depth mode
 - Oscillator for display clock generation
 - DC VCOM voltage generator and adjustment
 - CABC (Content Adaptive Brightness Control) function
 - DGC (Digital Gamma Correction) function
 - IIE (Impressive Image Enhancement) function
 - VGH/VGL voltage generator for gate control signal in panel
 - Gate control signals to gate driver in panel (GIP)
 - OTP (One-Time Programming) memory store initialization register settings
 - Provide 3 times to store DC VCOM value setting and ID1 ~ ID3
 - BIST (Built-In Self-Test Pattern) mode function

- ◆ Input power:
 - VCI = 2.5V ~ 6.6V
 - VDDI = 1.65V ~ 3.6V

- VCC1 = 1.65V ~ 6.6V
- VCC2 = 1.65V ~ 6.6V
- VDDAM = 1.65V ~ 3.6V
- VSP = 4.5V ~ 6.6V
- VSN = -6.6V ~ -4.5V
- OTP programming voltage (MTP_PWR): 8.5V

- ◆ Source/VCOM/Gate power supply voltage:
 - VCL-GND = -3.0V ~ -2.3V
 - DC VCOM = -4.0V ~ -0.2V (12mV/step); 0V
 - VREG1OUT = 3.5V ~ 5.6V (Positive source output voltage level)
 - VREG2OUT = -5.6V ~ -3.5V (Negative source output voltage level)
 - VGH-GND = 8V ~ 18V (Positive gate driver output voltage level)
 - VGL-GND = -7V ~ -18V (Negative gate driver output voltage level)

3. Device Overview

3.1. Block Diagram

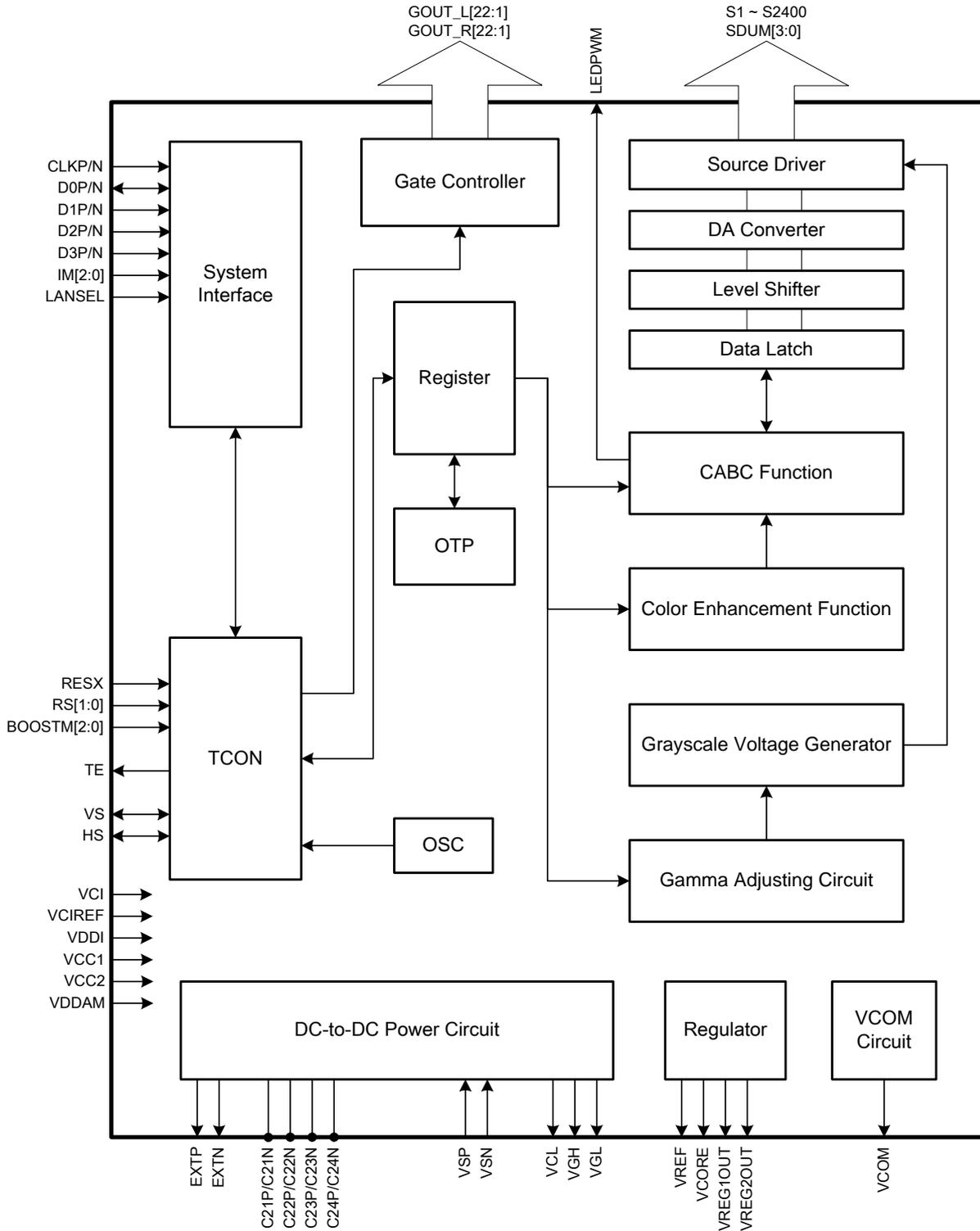


Figure 1: Block Diagram

3.2. Block Function Description

3.2.1. System Interface

The ILI9881C-04 supports DSI interfaces. The interface mode and the lane number of DSI interface can be selected by hardware pins IM[2:0], LANSEL and control register MIPI_LANE_SEL (Page4_R00h).

3.2.2. Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates a liquid crystal drive voltage that corresponds to the grayscale level set in the Gamma correction register. The ILI9881C-04 can display 16.7M colors at maximum.

3.2.3. TCON

The TCON generates timing signals for internal circuits. Timing for display operations are outputted separately so that they do not interfere with each other.

3.2.4. OSC

The ILI9881C-04 incorporates with an RC oscillator circuit. Command settings are used to change the frame frequency.

3.2.5. Source Driver Circuit

The LCD display driver circuit consists of a 2404-output source driver (S1~S2400 and SDUM[3:0]). The display pattern data is latched when 800RGB pixels of data are input. The voltage is output from the source driver according to the latched data.

3.2.6. Gate Controller Circuit

The panel control circuit outputs GOUT_L/R[22:1] signals at either the VGH or VGL level.

3.2.7. DC-to-DC Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels for driving a panel. Voltage levels are adjusted according to the register setting.

3.2.8. CABC (Content Adaptive Brightness Control)

The CABC (Content Adaptive Brightness Control) dynamic backlight control function is used to reduce the power consumption of the luminance source.

3.3. Pin Descriptions

Table 1: Pin Definition

Pin Name	I/O	Type	Descriptions																																																																																
Global Control Pins																																																																																			
IM[2:0]	I	VDDI	<p>- Interface mode select pins. Notes: (1) IM[2:0] pins are used to configure lane sequence and polarity (2) The bottom table is an example for MIPI 4 lane setting</p> <table border="1"> <thead> <tr> <th colspan="3">External Pad Set</th> <th colspan="5">Configuration of MIPI Lane</th> </tr> <tr> <th>IM2</th> <th>IM1</th> <th>IM0</th> <th>D0P/N Pin</th> <th>D1P/N Pin</th> <th>CLKP/N Pin</th> <th>D2P/N Pin</th> <th>D3P/N Pin</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>D3P/N</td> <td>D2P/N</td> <td>CLKP/N</td> <td>D1P/N</td> <td>D0P/N</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>D3N/P</td> <td>D2N/P</td> <td>CLKN/P</td> <td>D1N/P</td> <td>D0N/P</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>D0P/N</td> <td>D1P/N</td> <td>CLKP/N</td> <td>D2P/N</td> <td>D3P/N</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>D0N/P</td> <td>D1N/P</td> <td>CLKN/P</td> <td>D2N/P</td> <td>D3N/P</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>D3P/N</td> <td>D0P/N</td> <td>CLKP/N</td> <td>D1P/N</td> <td>D2P/N</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>D3N/P</td> <td>D0N/P</td> <td>CLKN/P</td> <td>D1N/P</td> <td>D2N/P</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>D2P/N</td> <td>D1P/N</td> <td>CLKP/N</td> <td>D0P/N</td> <td>D3P/N</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>D2N/P</td> <td>D1N/P</td> <td>CLKN/P</td> <td>D0N/P</td> <td>D3N/P</td> </tr> </tbody> </table>	External Pad Set			Configuration of MIPI Lane					IM2	IM1	IM0	D0P/N Pin	D1P/N Pin	CLKP/N Pin	D2P/N Pin	D3P/N Pin	0	0	0	D3P/N	D2P/N	CLKP/N	D1P/N	D0P/N	0	0	1	D3N/P	D2N/P	CLKN/P	D1N/P	D0N/P	0	1	0	D0P/N	D1P/N	CLKP/N	D2P/N	D3P/N	0	1	1	D0N/P	D1N/P	CLKN/P	D2N/P	D3N/P	1	0	0	D3P/N	D0P/N	CLKP/N	D1P/N	D2P/N	1	0	1	D3N/P	D0N/P	CLKN/P	D1N/P	D2N/P	1	1	0	D2P/N	D1P/N	CLKP/N	D0P/N	D3P/N	1	1	1	D2N/P	D1N/P	CLKN/P	D0N/P	D3N/P
External Pad Set			Configuration of MIPI Lane																																																																																
IM2	IM1	IM0	D0P/N Pin	D1P/N Pin	CLKP/N Pin	D2P/N Pin	D3P/N Pin																																																																												
0	0	0	D3P/N	D2P/N	CLKP/N	D1P/N	D0P/N																																																																												
0	0	1	D3N/P	D2N/P	CLKN/P	D1N/P	D0N/P																																																																												
0	1	0	D0P/N	D1P/N	CLKP/N	D2P/N	D3P/N																																																																												
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RS[1:0]	I	VDDI	<p>- Resolution selection pins.</p> <table border="1"> <thead> <tr> <th>RS1</th> <th>RS0</th> <th>Resolution</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>800 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line</td> </tr> <tr> <td>0</td> <td>1</td> <td>768 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line</td> </tr> <tr> <td>1</td> <td>0</td> <td>720 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line</td> </tr> <tr> <td>1</td> <td>1</td> <td>640 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line</td> </tr> </tbody> </table>	RS1	RS0	Resolution	0	0	800 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line	0	1	768 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line	1	0	720 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line	1	1	640 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line																																																																	
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1	1	640 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line																																																																																	
LANSEL	I	VDDI	<p>- MIPI DSI Lane number selection pin LANSEL="1", MIPI DSI is 2 Lane mode LANSEL="0", MIPI DSI is 3 or 4 Lane mode <i>Note: Please reference "Table 2 DSI Interface Lane Mode Selection"</i></p>																																																																																
BOOSTM[2:0]	I	VDDI	<p>- Power type selection pins</p> <table border="1"> <thead> <tr> <th>Page4_R6Eh DI_PWR_REG</th> <th>BOOSTM2</th> <th>BOOSTM1</th> <th>BOOSTM0</th> <th>NOTE</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>Power Mode 2A External VDDI, VSP and VSN (VCI=VSP) <i>Note 1</i></td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>Power Mode 4 External VDDI, VCI, VSP and VSN</td> </tr> <tr> <td>X</td> <td>0</td> <td>1</td> <td>0</td> <td>Power Mode 3 External VDDI and VCI (with ILI4003)</td> </tr> <tr> <td colspan="4" style="text-align: center;">prohibited</td> <td>-</td> </tr> </tbody> </table> <p>The default value of DI_PWR_REG is "1". <i>Note 1: VCI and VSP pads must be connected by external metal path.</i></p>	Page4_R6Eh DI_PWR_REG	BOOSTM2	BOOSTM1	BOOSTM0	NOTE	0	0	0	1	Power Mode 2A External VDDI, VSP and VSN (VCI=VSP) <i>Note 1</i>	1	0	0	1	Power Mode 4 External VDDI, VCI, VSP and VSN	X	0	1	0	Power Mode 3 External VDDI and VCI (with ILI4003)	prohibited				-																																																							
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prohibited				-																																																																															
RESX	I	VDDI	<p>- The external reset input Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power. Fix to VDDI level when not in use.</p>																																																																																
TE	O	VDDI	<p>- Tearing effect output pin. Leave the pin open when not in use.</p>																																																																																
VS	I/O	VDDI	<p>- Touch synchronization signal (VSOUT). Fix to VSS level when not in use.</p>																																																																																
HS	I/O	VDDI	<p>- Touch synchronization signal (HSOUT). Fix to VSS level when not in use.</p>																																																																																
LEDPWM	O	VDDI	<p>- LCD backlight control PWM output pin. Leave the pin open when not in use.</p>																																																																																
DSI Interface Signal Pins																																																																																			
CLKP CLKN	I	LVDSVDD	<p>- MIPI DSI differential clock pair Leave it open or fix to LVDSVSS level when not in use.</p>																																																																																
D0P D0N	I/O	LVDSVDD	<p>- MIPI DSI differential data pair. (Data lane 0) Leave it open or fix to LVDSVSS level when not in use.</p>																																																																																

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D1P D1N	I	LVDSVDD	- MIPI DSI differential data pair. (Data lane 1) Leave it open or fix to LVDSVSS level when not in use.												
D2P D2N	I	LVDSVDD	- MIPI DSI differential data pair. (Data lane 2) Leave it open or fix to LVDSVSS level when not in use.												
D3P D3N	I	LVDSVDD	- MIPI DSI differential data pair. (Data lane 3) Leave it open or fix to LVDSVSS level when not in use.												
Source / Panel Control / VCOM Signal Pins															
S[2400:1]	O	Analog	- Output source driver signals. The D/A converted 256-gray-scale analog voltage output. Source output mapping with different resolution <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Disaply resulation</th> <th>Source channels</th> </tr> </thead> <tbody> <tr> <td>800 (RGB)</td> <td>S1 ~ S2400</td> </tr> <tr> <td>768 (RGB)</td> <td>S1 ~ S1152, S1249 ~ S2400</td> </tr> <tr> <td>720 (RGB)</td> <td>S1 ~ S1080, S1321 ~ S2400</td> </tr> <tr> <td>640 (RGB)</td> <td>S1 ~ S960, S1441 ~ S2400</td> </tr> <tr> <td>800 (RGB) + Zig-Zag</td> <td>S1 ~ S2400, SDUM[2:1]</td> </tr> </tbody> </table>	Disaply resulation	Source channels	800 (RGB)	S1 ~ S2400	768 (RGB)	S1 ~ S1152, S1249 ~ S2400	720 (RGB)	S1 ~ S1080, S1321 ~ S2400	640 (RGB)	S1 ~ S960, S1441 ~ S2400	800 (RGB) + Zig-Zag	S1 ~ S2400, SDUM[2:1]
Disaply resulation	Source channels														
800 (RGB)	S1 ~ S2400														
768 (RGB)	S1 ~ S1152, S1249 ~ S2400														
720 (RGB)	S1 ~ S1080, S1321 ~ S2400														
640 (RGB)	S1 ~ S960, S1441 ~ S2400														
800 (RGB) + Zig-Zag	S1 ~ S2400, SDUM[2:1]														
SDUM[3:0]	O	Analog	- Dummy Source Leave the pin open when not in use.												
GOUT_L[22:1]	O	Analog	- Gate control signals for panel in left side of IC Leave the pin open when not in use.												
GOUT_R[22:1]	O	Analog	- Gate control signals for panel in right side of IC Leave the pin open when not in use.												
VCOM	O	Analog	- Regulator output for common voltage of panel Connect to a stabilizing capacitor between VCOM and VSSA.												
Power Supply Pins															
VCI	I	Power Supply	- Power supply for analog circuits. Connect to an external power supply of 2.5V to 6.6V												
VCIREF	I	Power Supply	- Power supply for analog circuits. Connect to an external power supply of 2.5V to 6.6V												
VDDI	I	Power Supply	- Power supply for I/O pads. Connect to an external power supply of 1.65V to 3.6V												
VCC1	I	Power Supply	- Power supply for internal logic regulator. Connect to an external power supply of 1.65V to 6.6V												
VCC2	I	Power Supply	- Power supply for internal logic regulator. Connect to an external power supply of 1.65V to 6.6V												
VDDAM	I	Power Supply	- Power supply for MIPI DSI regulator. Connect to an external power supply of 1.65V to 3.6V												
VSP	I	Power Supply	- Input voltage from step-up circuit. Connect to an external power supply of 4.5V to 6.6V												
VSN	I	Power Supply	- Input voltage from step-up circuit. Connect to an external power supply of -4.5V to -6.6V.												
VSSA	I	Ground	- System ground for the analog circuit In the case of COG, connect to GND on the FPC to prevent noise.												
VSSREF	I	Ground	- System ground for the analog circuit In the case of COG, connect to GND on the FPC to prevent noise.												
LVDSVSS	I	Ground	- System ground for MIPI DSI analog ground In the case of COG, connect to GND on the FPC to prevent noise.												
VSS	I	Ground	- System ground for digital circuit In the case of COG, connect to GND on the FPC to prevent noise.												
MTP_PWR	I	Power Supply	- Input power for OTP programming. MTP_PWR=8. 5V When not under programming, let MTP_PWR float or connect to ground.												
DC-to-DC Circuit Pins															
VREG1OUT	O	Analog	- Regulator output voltage from VSP, It's for positive gray scale voltage. Connect to a stabilizing capacitor between GVDD and VSSA.												
VREG2OUT	O	Analog	- Regulator output voltage from VSN, It's for negative gray scale voltage. Connect to a stabilizing capacitor between NGVDD and VSSA.												
VCL	O	Analog	- Output voltage from step-up circuit												

			Connect to a stabilizing capacitor between VCL and VSSA.
VGH	O	Analog	- Output voltage from step-up circuit Connect to a stabilizing capacitor between VGH and VSSA.
VGL	O	Analog	- Output voltage from step-up circuit Connect to a stabilizing capacitor between VGL and VSSA.
EXTP	O	VCI	- Control signal output to generate VSP
EXTN	O	VCI	- Control signal output to generate VSN
LVDSVDD	O	Analog	- MIPI DSI regulator output
VREF	O	Analog	- Reference voltage from internal band gap circuit (1.8V typical)
VCORE	O	Analog	- Internal logic regulator output (1.5V typical) Connect to a stabilizing capacitor between VCORE and VSSA.
C21P / C21N C22P / C22N	I/O	Step-up Capacitor	- Connect the charge-pumping capacitor for generating VGH level.
C23P / C23N C24P / C24N	I/O	Step-up Capacitor	- Connect the charge-pumping capacitor for generating VGL level.
Test / Dummy Pins			
PCLK	I	VDDI	- Test pins Unused pins should be left open.
D[7:0]	I/O	VDDI	- Test pins Unused pins should be left open or connected to VSS, VDDI.
TEST[5:0]	I/O	VDDI	- Test pins Unused pins should be left open or connected to VSS, VDDI.
TOUT[3:0]	I/O	VDDI	- Test pins Unused pins should be left open or connected to VSS, VDDI.
VTESTOUTP	O	Analog	- Analog test output pin Let it open.
VTESTOUTN	O	Analog	- Analog test output pin Let it open.
CSX	I	VDDI	- Test pins Fix to VDDI or VSS level when not in use.
DCX	I	VDDI	- Test pins Fix to VDDI or VSS level when not in use.
SCL	I	VDDI	- Test pins Fix to VDDI or VSS level when not in use.
SDI	I	VDDI	- Test pins Leave the pin open when not in use.
SDO	O	VDDI	- Test pins Leave the pin open when not in use.
TE1	O	VDDI	- Test pins. Leave the pin open when not in use.
C31P	-	-	- Dummy pins Let it open.
VCOMR	-	-	- Dummy pins Let it open.
VGLO2DUMMY	-	-	- Dummy pins Let it open.
DUMMYR1	-	Analog	- dummy pins Propose to connect these two pads separately when use for bonding resistance measurement
VSSDUMMY	-	-	- Dummy pins Let it open.
DUMMY[85:3]	-	-	- Dummy pins Let it open.
DUMMYN	-	-	- Dummy pins Let it open.
DUMMYP	-	-	- Dummy pins Let it open.
VGLO1	O	Analog	- Dummy pins

			Let it open.
C41P / C41N C42P / C42N	-	-	- Dummy pins Let it open.

3.4. Pin Assignment

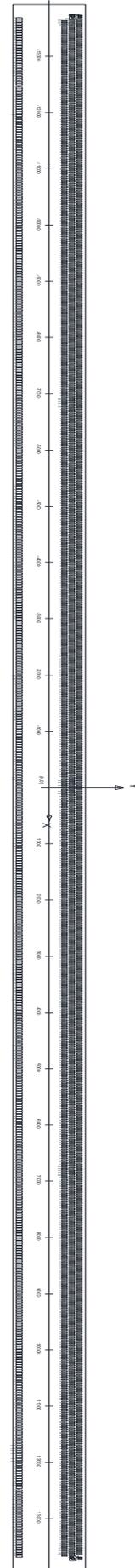
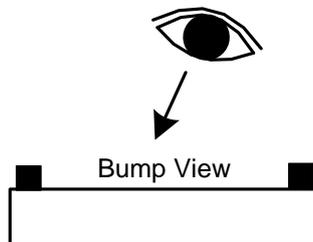
Chip Size: 27840 um x 875 um

Pad Location: Pad Center.

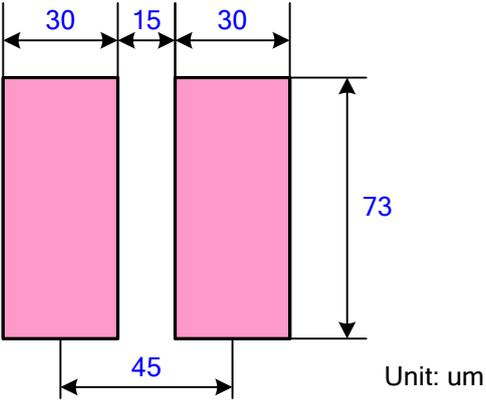
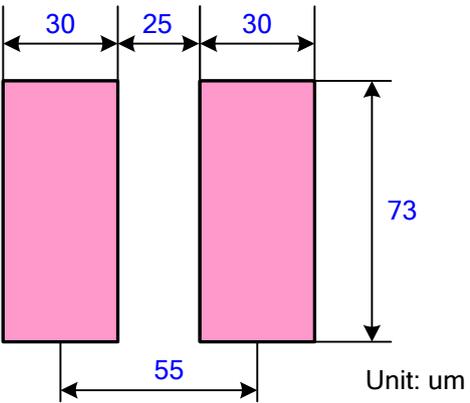
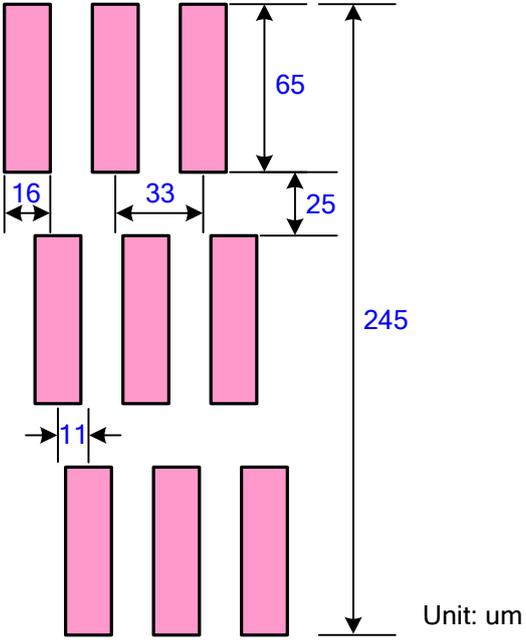
Coordinate Origin: Chip center

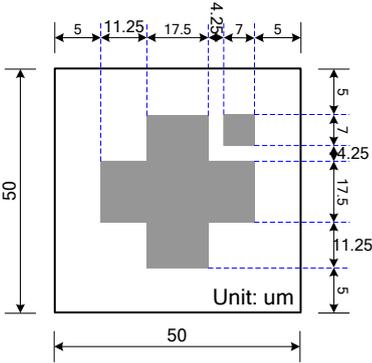
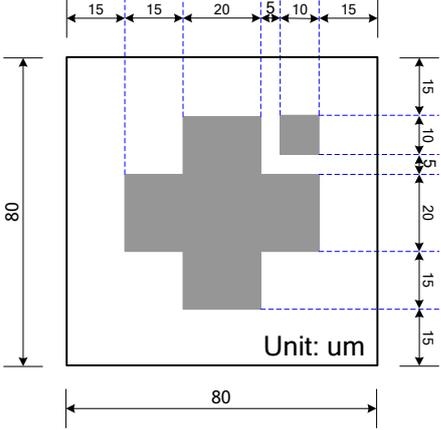
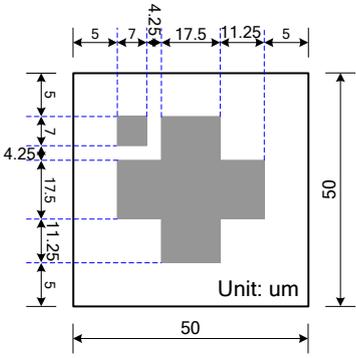
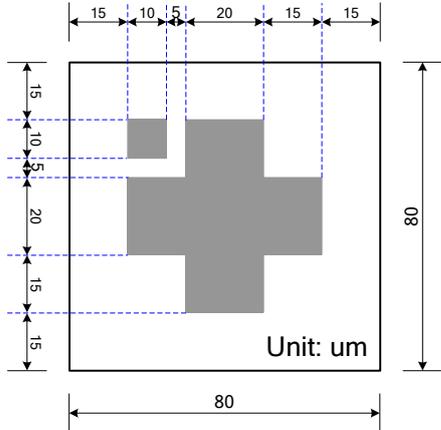
Bump Size:

1. 30um x 73um
Pad 1 to 608.
2. 16um x 65um
Pad 609 to 3092.



3.5. Bump Arrangement

<p>Input PAD (No. 1~27, 28~581, 582~608)</p>	 <p>Unit: um</p>
<p>Input PAD (No. 27~28, 581~582)</p>	 <p>Unit: um</p>
<p>Output PAD (No. 609~3092)</p>	 <p>Unit: um</p>

<p>Alignment mark R</p>	 <p>Alignment mark: (13706,372.5)</p>	 <p>Alignment mark: (13706,285.5)</p>
<p>Alignment mark L</p>	 <p>Alignment mark: (-13706,372.5)</p>	 <p>Alignment mark: (-13706,285.5)</p>

3.6. Pad Coordination

No.	Name	X	Y
1	DUMMY1	-13709.46	-361
2	DUMMY1	-13664.47	-361
3	DUMMY1	-13619.48	-361
4	GOUT L11	-13574.49	-361
5	GOUT L12	-13529.5	-361
6	GOUT L13	-13484.51	-361
7	GOUT L14	-13439.52	-361
8	GOUT L15	-13394.53	-361
9	GOUT L16	-13349.54	-361
10	GOUT L17	-13304.55	-361
11	GOUT L18	-13259.56	-361
12	GOUT L19	-13214.57	-361
13	GOUT L101	-13169.58	-361
14	GOUT L111	-13124.59	-361
15	GOUT L121	-13079.6	-361
16	GOUT L131	-13034.61	-361
17	GOUT L141	-12989.62	-361
18	GOUT L151	-12944.63	-361
19	GOUT L161	-12899.64	-361
20	GOUT L171	-12854.65	-361
21	GOUT L181	-12809.66	-361
22	GOUT L191	-12764.67	-361
23	GOUT L201	-12719.68	-361
24	GOUT L211	-12674.69	-361
25	GOUT L221	-12629.7	-361
26	VCOM	-12584.71	-361
27	VCOM	-12539.72	-361
28	VCOM	-12494.73	-361
29	VSSA	-12449.74	-361
30	VSSA	-12394.75	-361
31	VSSA	-12349.76	-361
32	VSSA	-12304.77	-361
33	VSSA	-12259.78	-361
34	VSSA	-12214.79	-361
35	VSSA	-12169.8	-361
36	VSSA	-12124.81	-361
37	VSSA	-12079.82	-361
38	VSSA	-12034.83	-361
39	VTESTOUTP	-11989.84	-361
40	VTESTOUTP	-11944.85	-361
41	LVDSVSS	-11899.86	-361
42	DN	-11854.87	-361
43	DN	-11809.88	-361
44	DN	-11764.89	-361
45	DN	-11719.9	-361
46	DN	-11674.91	-361
47	DN	-11629.92	-361
48	DOP	-11584.93	-361
49	DOP	-11539.94	-361
50	DOP	-11494.95	-361
51	DOP	-11449.96	-361
52	DOP	-11404.97	-361
53	DOP	-11359.98	-361
54	LVDSVSS	-11314.99	-361
55	DIN	-11270	-361
56	DIN	-11225.01	-361
57	DIN	-11180.02	-361
58	DIN	-11135.03	-361
59	DIN	-11090.04	-361
60	DIN	-11045.05	-361
61	DIP	-11000.06	-361
62	DIP	-10955.07	-361
63	DIP	-10910.08	-361
64	DIP	-10865.09	-361
65	DIP	-10820.1	-361
66	DIP	-10775.11	-361
67	LVDSVSS	-10730.12	-361
68	CLKN	-10685.13	-361
69	CLKN	-10640.14	-361
70	CLKN	-10595.15	-361
71	CLKN	-10550.16	-361
72	CLKN	-10505.17	-361
73	CLKN	-10460.18	-361
74	CLKP	-10415.19	-361
75	CLKP	-10370.2	-361
76	CLKP	-10325.21	-361
77	CLKP	-10280.22	-361
78	CLKP	-10235.23	-361
79	CLKP	-10190.24	-361
80	LVDSVSS	-10145.25	-361
81	D2N	-10100.26	-361
82	D2N	-10055.27	-361
83	D2N	-10010.28	-361
84	D2N	-9965.29	-361
85	D2N	-9920.3	-361
86	D2P	-9875.31	-361
87	D2P	-9830.32	-361
88	D2P	-9785.33	-361
89	D2P	-9740.34	-361
90	D2P	-9695.35	-361
91	D2P	-9650.36	-361
92	D2P	-9605.37	-361
93	LVDSVSS	-9560.38	-361
94	D3N	-9515.39	-361
95	D3N	-9470.4	-361
96	D3N	-9425.41	-361
97	D3N	-9380.42	-361
98	D3N	-9335.43	-361
99	D3N	-9290.44	-361
100	D3P	-9245.45	-361

No.	Name	X	Y
101	D3P	-9200.46	-361
102	D3P	-9155.47	-361
103	D3P	-9110.48	-361
104	D3P	-9065.49	-361
105	D3P	-9020.5	-361
106	LVDSVSS	-8975.51	-361
107	LVDSVSS	-8930.52	-361
108	LVDSVSS	-8885.53	-361
109	LVDSVSS	-8840.54	-361
110	LVDSVSS	-8795.55	-361
111	LVDSVSS	-8750.56	-361
112	LVDSVSS	-8705.57	-361
113	LVDSVSS	-8660.58	-361
114	LVDSVSS	-8615.59	-361
115	LVDSVSS	-8570.6	-361
116	LVDSVSS	-8525.61	-361
117	LVDSVSS	-8480.62	-361
118	LVDSVDD	-8435.63	-361
119	LVDSVDD	-8390.64	-361
120	LVDSVDD	-8345.65	-361
121	LVDSVDD	-8300.66	-361
122	LVDSVDD	-8255.67	-361
123	LVDSVDD	-8210.68	-361
124	LVDSVDD	-8165.69	-361
125	LVDSVDD	-8120.7	-361
126	LVDSVDD	-8075.71	-361
127	LVDSVDD	-8030.72	-361
128	LVDSVDD	-7985.73	-361
129	LVDSVDD	-7940.74	-361
130	VDDAM	-7895.75	-361
131	VDDAM	-7850.76	-361
132	VDDAM	-7805.77	-361
133	VDDAM	-7760.78	-361
134	VDDAM	-7715.79	-361
135	VDDAM	-7670.8	-361
136	VDDAM	-7625.81	-361
137	VDDAM	-7580.82	-361
138	VDDAM	-7535.83	-361
139	VDDAM	-7490.84	-361
140	VDDAM	-7445.85	-361
141	VDDAM	-7400.86	-361
142	VCC1	-7355.87	-361
143	VCC1	-7310.88	-361
144	VCC1	-7265.89	-361
145	VCC1	-7220.9	-361
146	VCC1	-7175.91	-361
147	VCC1	-7130.92	-361
148	VCC1	-7085.93	-361
149	VCC1	-7040.94	-361
150	VCC1	-6995.95	-361
151	VCC1	-6950.96	-361
152	VCC1	-6905.97	-361
153	VCC1	-6860.98	-361
154	VCC1	-6815.99	-361
155	VCC1	-6771	-361
156	VCC1	-6726.01	-361
157	VCORE	-6681.02	-361
158	VCORE	-6636.03	-361
159	VCORE	-6591.04	-361
160	VCORE	-6546.05	-361
161	VCORE	-6501.06	-361
162	VCORE	-6456.07	-361
163	VCORE	-6411.08	-361
164	VCORE	-6366.09	-361
165	VCORE	-6321.1	-361
166	VCORE	-6276.11	-361
167	VCORE	-6231.12	-361
168	VCORE	-6186.13	-361
169	VCORE	-6141.14	-361
170	VCORE	-6096.15	-361
171	VCORE	-6051.16	-361
172	VSS	-6006.17	-361
173	VSS	-5961.18	-361
174	VSS	-5916.19	-361
175	VSS	-5871.2	-361
176	VSS	-5826.21	-361
177	VSS	-5781.22	-361
178	VSS	-5736.23	-361
179	VSS	-5691.24	-361
180	VSS	-5646.25	-361
181	VSS	-5601.26	-361
182	VSS	-5556.27	-361
183	VSS	-5511.28	-361
184	VSS	-5466.29	-361
185	VSS	-5421.3	-361
186	VSS	-5376.31	-361
187	TOUTI31	-5331.32	-361
188	TOUTI31	-5286.33	-361
189	TOUTI21	-5241.34	-361
190	TOUTI21	-5196.35	-361
191	TOUTI11	-5151.36	-361
192	TOUTI11	-5106.37	-361
193	TOUTI01	-5061.38	-361
194	TOUTI01	-5016.39	-361
195	DUMMYP	-4971.4	-361
196	DUMMYP	-4926.41	-361
197	DUMMYP	-4881.42	-361
198	DUMMYP	-4836.43	-361
199	DUMMYP	-4791.44	-361
200	DUMMYP	-4746.45	-361

No.	Name	X	Y
201	DUMMYP	-4701.46	-361
202	DUMMYP	-4656.47	-361
203	DUMMYP	-4611.48	-361
204	DUMMYP	-4566.49	-361
205	DUMMYP	-4521.5	-361
206	DUMMYP	-4476.51	-361
207	DUMMYP	-4431.52	-361
208	DUMMYP	-4386.53	-361
209	DUMMYP	-4341.54	-361
210	DUMMYP	-4296.55	-361
211	DUMMYP	-4251.56	-361
212	DUMMYP	-4206.57	-361
213	DUMMYP	-4161.58	-361
214	DUMMYP	-4116.59	-361
215	DUMMYP	-4071.6	-361
216	DUMMYP	-4026.61	-361
217	DUMMYP	-3981.62	-361
218	DUMMYP	-3936.63	-361
219	DUMMYP	-3891.64	-361
220	DUMMYP	-3846.65	-361
221	DUMMYP	-3801.66	-361
222	DUMMYP	-3756.67	-361
223	DUMMYP	-3711.68	-361
224	DUMMYP	-3666.69	-361
225	DUMMYP	-3621.7	-361
226	DUMMYP	-3576.71	-361
227	DUMMYP	-3531.72	-361
228	DUMMYP	-3486.73	-361
229	DUMMYP	-3441.74	-361
230	DUMMYP	-3396.75	-361
231	DUMMYP	-3351.76	-361
232	DUMMYP	-3306.77	-361
233	DUMMYP	-3261.78	-361
234	DUMMYP	-3216.79	-361
235	DUMMYP	-3171.8	-361
236	DUMMYP	-3126.81	-361
237	DUMMYP	-3081.82	-361
238	DUMMYP	-3036.83	-361
239	DUMMYP	-2991.84	-361
240	VSS	-2946.85	-361
241	VSS	-2901.86	-361
242	DI71	-2856.87	-361
243	DI71	-2811.88	-361
244	DI61	-2766.89	-361
245	DI61	-2721.9	-361
246	DI51	-2676.91	-361
247	DI51	-2631.92	-361
248	DI41	-2586.93	-361
249	DI41	-2541.94	-361
250	DI31	-2496.95	-361
251	DI31	-2451.96	-361
252	DI21	-2406.97	-361
253	DI21	-2361.98	-361
254	DI11	-2316.99	-361
255	DI11	-2272	-361
256	DI01	-2227.01	-361
257	DI01	-2182.02	-361
258	HS	-2137.03	-361
259	HS	-2092.04	-361
260	VS	-2047.05	-361
261	VS	-2002.06	-361
262	VSSDUMMY	-1957.07	-361
263	VSSDUMMY	-1912.08	-361
264	PCLK	-1867.09	-361
265	PCLK	-1822.1	-361
266	DCX	-1777.11	-361
267	DCX	-1732.12	-361
268	CNSX	-1687.13	-361
269	CNSX	-1642.14	-361
270	SCL	-1597.15	-361
271	SCL	-1552.16	-361
272	SDI	-1507.17	-361
273	SDI	-1462.18	-361
274	SDO	-1417.19	-361
275	SDO	-1372.2	-361
276	LEDPWM	-1327.21	-361
277	LEDPWM	-1282.22	-361
278	LEDPWM	-1237.23	-361
279	LEDPWM	-1192.24	-361
280	TE	-1147.25	-361
281	TE	-1102.26	-361
282	TE	-1057.27	-361
283	TE	-1012.28	-361
284	TE	-967.29	-361
285	TE	-922.3	-361
286	TE1	-877.31	-361
287	TE1	-832.32	-361
288	TE1	-787.33	-361
289	TE1	-742.34	-361
290	TE1	-697.35	-361
291	TE1	-652.36	-361
292	RESX	-607.37	-361
293	RESX	-562.38	-361
294	RESX	-517.39	-361
295	RESX	-472.4	-361
296	TESTI51	-427.41	-361
297	TESTI41	-382.42	-361
298	TESTI31		

No.	Name	X	Y
401	VSSA	4296.55	-361
402	VSSA	4341.54	-361
403	VSSA	4386.53	-361
404	VSSA	4431.52	-361
405	VSSA	4476.51	-361
406	VSSA	4521.5	-361
407	VSSA	4566.49	-361
408	VREGIOUT	4611.48	-361
409	VREGIOUT	4656.47	-361
410	VREGIOUT	4701.46	-361
411	VREGIOUT	4746.45	-361
412	VREGIOUT	4791.44	-361
413	VREGIOUT	4836.43	-361
414	VREF	4881.42	-361
415	VREF	4926.41	-361
416	VREF	4971.4	-361
417	VSS	5016.39	-361
418	VSS	5061.38	-361
419	VSS	5106.37	-361
420	VSS	5151.36	-361
421	VSS	5196.35	-361
422	VCI	5241.34	-361
423	VCI	5286.33	-361
424	VCI	5331.32	-361
425	VCI	5376.31	-361
426	VCI	5421.3	-361
427	VCI	5466.29	-361
428	VCI	5511.28	-361
429	VCI	5556.27	-361
430	VCL	5601.26	-361
431	VCL	5646.25	-361
432	VCL	5691.24	-361
433	VCL	5736.23	-361
434	VCL	5781.22	-361
435	C41P	5826.21	-361
436	C41P	5871.2	-361
437	C41P	5916.19	-361
438	C41P	5961.18	-361
439	C41P	6006.17	-361
440	C41P	6051.16	-361
441	C41P	6096.15	-361
442	C41N	6141.14	-361
443	C41N	6186.13	-361
444	C41N	6231.12	-361
445	C41N	6276.11	-361
446	C41N	6321.1	-361
447	C41N	6366.09	-361
448	C41N	6411.08	-361
449	C42P	6456.07	-361
450	C42P	6501.06	-361
451	C42P	6546.05	-361
452	C42P	6591.04	-361
453	C42P	6636.03	-361
454	C42P	6681.02	-361
455	C42P	6726.01	-361
456	C42N	6771	-361
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1223	SI18041	6966.91	365
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1229	DUMMY13	6900.93	365
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1247	SI17981	6702.97	365
1248	SI17971	6691.98	185
1249	SI17961	6680.98	275
1250	SI17951	6669.98	365
1251	SI17941	6658.98	185
1252	SI17931	6647.99	275
1253	SI17921	6636.99	365
1254	SI17911	6625.99	185
1255	SI17901	6614.99	275
1256	SI17891	6604	365
1257	SI17881	6593	185
1258	SI17871	6582	275
1259	SI17861	6571	365
1260	SI17851	6560.01	185
1261	SI17841	6549.01	275
1262	SI17831	6538.01	365
1263	SI17821	6527.01	185
1264	SI17811	6516.02	275
1265	SI17801	6505.02	365
1266	SI17791	6494.02	185
1267	SI17781	6483.02	275
1268	SI17771	6472.03	365
1269	SI17761	6461.03	185
1270	SI17751	6450.03	275
1271	SI17741	6439.03	365
1272	SI17731	6428.04	185
1273	SI17721	6417.04	275
1274	SI17711	6406.04	365
1275	SI17701	6395.04	185
1276	SI17691	6384.05	275
1277	SI17681	6373.05	365
1278	SI17671	6362.05	185
1279	SI17661	6351.05	275
1280	SI17651	6340.06	365
1281	SI17641	6329.06	185
1282	SI17631	6318.06	275
1283	SI17621	6307.06	365
1284	SI17611	6296.07	185
1285	SI17601	6285.07	275
1286	SI17591	6274.07	365
1287	SI17581	6263.07	185
1288	SI17571	6252.08	275
1289	SI17561	6241.08	365
1290	SI17551	6230.08	185
1291	SI17541	6219.08	275
1292	SI17531	6208.09	365
1293	SI17521	6197.09	185
1294	SI17511	6186.09	275
1295	SI17501	6175.09	365
1296	SI17491	6164.1	185
1297	SI17481	6153.1	275
1298	SI17471	6142.1	365
1299	SI17461	6131.1	185
1300	SI17451	6120.11	275

No.	Name	X	Y
1301	SI17441	6109.11	365
1302	SI17431	6098.11	185
1303	SI17421	6087.11	275
1304	SI17411	6076.12	365
1305	SI17401	6065.12	185
1306	SI17391	6054.12	275
1307	SI17381	6043.12	365
1308	SI17371	6032.13	185
1309	SI17361	6021.13	275
1310	SI17351	6010.13	365
1311	SI17341	5999.13	185
1312	SI17331	5988.14	275
1313	SI17321	5977.14	365
1314	SI17311	5966.14	185
1315	SI17301	5955.14	275
1316	SI17291	5944.15	365
1317	SI17281	5933.15	185
1318	SI17271	5922.15	275
1319	SI17261	5911.15	365
1320	SI17251	5900.16	185
1321	SI17241	5889.16	275
1322	SI17231	5878.16	365
1323	SI17221	5867.16	185
1324	SI17211	5856.17	275
1325	SI17201	5845.17	365
1326	SI17191	5834.17	185
1327	SI17181	5823.17	275
1328	SI17171	5812.18	365
1329	SI17161	5801.18	185
1330	SI17151	5790.18	275
1331	SI17141	5779.18	365
1332	SI17131	5768.19	185
1333	SI17121	5757.19	275
1334	SI17111	5746.19	365
1335	SI17101	5735.19	185
1336	SI17091	5724.2	275
1337	SI17081	5713.2	365
1338	SI17071	5702.2	185
1339	SI17061	5691.2	275
1340	SI17051	5680.21	365
1341	SI17041	5669.21	185
1342	SI17031	5658.21	275
1343	SI17021	5647.21	365
1344	SI17011	5636.22	185
1345	SI17001	5625.22	275
1346	SI16991	5614.22	365
1347	SI16981	5603.22	185
1348	SI16971	5592.23	275
1349	SI16961	5581.23	365
1350	SI16951	5570.23	185
1351	SI16941	5559.23	275
1352	SI16931	5548.24	365
1353	SI16921	5537.24	185
1354	SI16911	5526.24	275
1355	SI16901	5515.24	365
1356	SI16891	5504.25	185
1357	SI16881	5493.25	275
1358	SI16871	5482.25	365
1359	SI16861	5471.25	185
1360	SI16851	5460.26	275
1361	SI16841	5449.26	365
1362	SI16831	5438.26	185
1363	SI16821	5427.26	275
1364	SI16811	5416.27	365
1365	SI16801	5405.27	185
1366	SI16791	5394.27	275
1367	SI16781	5383.27	365
1368	SI16771	5372.28	185
1369	SI16761	5361.28	275
1370	SI16751	5350.28	365
1371	SI16741	5339.28	185
1372	SI16731	5328.29	275
1373	SI16721	5317.29	365
1374	SI16711	5306.29	185
1375	SI16701	5295.29	275
1376	SI16691	5284.3	365
1377	SI16681	5273.3	185
1378	SI16671	5262.3	275
1379	SI16661	5251.3	365
1380	SI16651	5240.31	185
1381	SI16641	5229.31	275
1382	SI16631	5218.31	365
1383	SI16621	5207.31	185
1384	SI16611	5196.32	275
1385	SI16601	5185.32	365
1386	SI16591	5174.32	185
1387	SI16581	5163.32	275
1388	SI16571	5152.33	365
1389	SI16561	5141.33	185
1390	SI16551	5130.33	275
1391	SI16541	5119.33	365
1392	SI16531	5108.34	185
1393	SI16521	5097.34	275
1394	SI16511	5086.34	365
1395	SI16501	5075.34	185
1396	SI16491	5064.35	275
1397	SI16481	5053.35	365
1398	SI16471	5042.35	185
1399	SI16461	5031.35	275
1400	SI16451	5020.36	365

No.	Name	X	Y
1401	SI16441	5009.36	185
1402	SI16431	4998.36	275
1403	SI16421	4987.36	365
1404	SI16411	4976.37	185
1405	SI16401	4965.37	275
1406	SI16391	4954.37	365
1407	SI16381	4943.37	185
1408	SI16371	4932.38	275
1409	SI16361	4921.38	365
1410	SI16351	4910.38	185
1411	SI16341	4899.38	275
1412	SI16331	4888.39	365
1413	SI16321	4877.39	185
1414	SI16311	4866.39	275
1415	SI16301	4855.39	365
1416	SI16291	4844.4	185
1417	SI16281	4833.4	275
1418	SI16271	4822.4	365
1419	SI16261	4811.4	185
1420	SI16251	4800.41	275
1421	SI16241	4789.41	365
1422	SI16231	4778.41	185
1423	SI16221	4767.41	275
1424	SI16211	4756.42	365
1425	SI16201	4745.42	185
1426	SI16191	4734.42	275
1427	SI16181	4723.42	365
1428	SI16171	4712.43	185
1429	SI16161	4701.43	275
1430	SI16151	4690.43	365
1431	SI16141	4679.43	185
1432	SI16131	4668.44	275
1433	SI16121	4657.44	365
1434	SI16111	4646.44	185
1435	SI16101	4635.44	275
1436	SI16091	4624.45	365
1437	SI16081	4613.45	185
1438	SI16071	4602.45	275
1439	SI16061	4591.45	365
1440	SI16051	4580.46	185
1441	SI16041	4569.46	275
1442	SI16031	4558.46	365
1443	SI16021	4547.46	185
1444	SI16011	4536.47	275
1445	SI16001	4525.47	365
1446	SI15991	4514.47	185
1447	SI15981	4503.47	275
1448	SI15971	4492.48	365
1449	SI15961	4481.48	185
1450	SI15951	4470.48	275
1451	SI15941	4459.48	365
1452	SI15931	4448.49	185
1453	SI15921	4437.49	275
1454	SI15911	4426.49	365
1455	SI15901	4415.49	185
1456	SI15891	4404.5	275
1457	SI15881	4393.5	365
1458	SI15871	4382.5	185
1459	SI15861	4371.5	275
1460	SI15851	4360.51	365
1461	SI15841	4349.51	185
1462	SI15831	4338.51	275
1463	SI15821	4327.51	365
1464	SI15811	4316.52	185
1465	SI15801	4305.52	275
1466	SI15791	4294.52	365
1467	SI15781	4283.52	185
1468	SI15771	4272.53	

No.	Name	X	Y
1601	SI1441	2809.86	365
1602	SI1443	2798.86	185
1603	SI1442	2787.86	275
1604	SI1441	2776.87	365
1605	SI1440	2765.87	185
1606	SI1439	2754.87	275
1607	SI1438	2743.87	365
1608	SI1437	2732.88	185
1609	SI1436	2721.88	275
1610	SI1435	2710.88	365
1611	SI1434	2699.88	185
1612	SI1433	2688.89	275
1613	SI1432	2677.89	365
1614	SI1431	2666.89	185
1615	SI1430	2655.89	275
1616	SI1429	2644.9	365
1617	SI1428	2633.9	185
1618	SI1427	2622.9	275
1619	SI1426	2611.9	365
1620	SI1425	2600.91	185
1621	SI1424	2589.91	275
1622	SI1423	2578.91	365
1623	SI1422	2567.91	185
1624	SI1421	2556.92	275
1625	SI1420	2545.92	365
1626	SI1419	2534.92	185
1627	SI1418	2523.92	275
1628	SI1417	2512.93	365
1629	SI1416	2501.93	185
1630	SI1415	2490.93	275
1631	SI1414	2479.93	365
1632	SI1413	2468.94	185
1633	SI1412	2457.94	275
1634	SI1411	2446.94	365
1635	SI1410	2435.94	185
1636	SI1409	2424.95	275
1637	SI1408	2413.95	365
1638	SI1407	2402.95	185
1639	SI1406	2391.95	275
1640	SI1405	2380.96	365
1641	SI1404	2369.96	185
1642	SI1403	2358.96	275
1643	SI1402	2347.96	365
1644	SI1401	2336.97	185
1645	SI1400	2325.97	275
1646	SI1399	2314.97	365
1647	SI1398	2303.97	185
1648	SI1397	2292.98	275
1649	SI1396	2281.98	365
1650	SI1395	2270.98	185
1651	SI1394	2259.99	275
1652	SI1393	2248.99	365
1653	SI1392	2237.99	185
1654	SI1391	2226.99	275
1655	SI1390	2215.99	365
1656	SI1389	2205	185
1657	SI1388	2194	275
1658	SI1387	2183	365
1659	SI1386	2172	185
1660	SI1385	2161.01	275
1661	SI1384	2150.01	365
1662	SI1383	2139.01	185
1663	SI1382	2128.01	275
1664	SI1381	2117.02	365
1665	SI1380	2106.02	185
1666	SI1379	2095.02	275
1667	SI1378	2084.02	365
1668	SI1377	2073.03	185
1669	SI1376	2062.03	275
1670	SI1375	2051.03	365
1671	SI1374	2040.03	185
1672	SI1373	2029.04	275
1673	SI1372	2018.04	365
1674	SI1371	2007.04	185
1675	SI1370	1996.04	275
1676	SI1369	1985.05	365
1677	SI1368	1974.05	185
1678	SI1367	1963.05	275
1679	SI1366	1952.05	365
1680	SI1365	1941.06	185
1681	SI1364	1930.06	275
1682	SI1363	1919.06	365
1683	SI1362	1908.06	185
1684	SI1361	1897.07	275
1685	SI1360	1886.07	365
1686	SI1359	1875.07	185
1687	SI1358	1864.07	275
1688	SI1357	1853.08	365
1689	SI1356	1842.08	185
1690	SI1355	1831.08	275
1691	SI1354	1820.08	365
1692	SI1353	1809.09	185
1693	SI1352	1798.09	275
1694	SI1351	1787.09	365
1695	SI1350	1776.09	185
1696	SI1349	1765.1	275
1697	SI1348	1754.1	365
1698	SI1347	1743.1	185
1699	SI1346	1732.1	275
1700	SI1345	1721.11	365

No.	Name	X	Y
1701	SI1344	1710.11	185
1702	SI1343	1699.11	275
1703	SI1342	1688.11	365
1704	SI1341	1677.12	185
1705	SI1340	1666.12	275
1706	SI1339	1655.12	365
1707	SI1338	1644.12	185
1708	SI1337	1633.13	275
1709	SI1336	1622.13	365
1710	SI1335	1611.13	185
1711	SI1334	1600.13	275
1712	SI1333	1589.14	365
1713	SI1332	1578.14	185
1714	SI1331	1567.14	275
1715	SI1330	1556.14	365
1716	SI1329	1545.15	185
1717	SI1328	1534.15	275
1718	SI1327	1523.15	365
1719	SI1326	1512.15	185
1720	SI1325	1501.16	275
1721	SI1324	1490.16	365
1722	SI1323	1479.16	185
1723	SI1322	1468.16	275
1724	SI1321	1457.17	365
1725	SI1320	1446.17	185
1726	SI1319	1435.17	275
1727	SI1318	1424.17	365
1728	SI1317	1413.18	185
1729	SI1316	1402.18	275
1730	SI1315	1391.18	365
1731	SI1314	1380.18	185
1732	SI1313	1369.19	275
1733	SI1312	1358.19	365
1734	SI1311	1347.19	185
1735	SI1310	1336.19	275
1736	SI1309	1325.2	365
1737	SI1308	1314.2	185
1738	SI1307	1303.2	275
1739	SI1306	1292.2	365
1740	SI1305	1281.21	185
1741	SI1304	1270.21	275
1742	SI1303	1259.21	365
1743	SI1302	1248.21	185
1744	SI1301	1237.22	275
1745	SI1300	1226.22	365
1746	SI1299	1215.22	185
1747	SI1298	1204.22	275
1748	SI1297	1193.23	365
1749	SI1296	1182.23	185
1750	SI1295	1171.23	275
1751	SI1294	1160.23	365
1752	SI1293	1149.24	185
1753	SI1292	1138.24	275
1754	SI1291	1127.24	365
1755	SI1290	1116.24	185
1756	SI1289	1105.25	275
1757	SI1288	1094.25	365
1758	SI1287	1083.25	185
1759	SI1286	1072.25	275
1760	SI1285	1061.26	365
1761	SI1284	1050.26	185
1762	SI1283	1039.26	275
1763	SI1282	1028.26	365
1764	SI1281	1017.27	185
1765	SI1280	1006.27	275
1766	SI1279	995.27	365
1767	SI1278	984.27	185
1768	SI1277	973.28	275
1769	SI1276	962.28	365
1770	SI1275	951.28	185
1771	SI1274	940.28	275
1772	SI1273	929.29	365
1773	SI1272	918.29	185
1774	SI1271	907.29	275
1775	SI1270	896.29	365
1776	SI1269	885.3	185
1777	SI1268	874.3	275
1778	SI1267	863.3	365
1779	SI1266	852.3	185
1780	SI1265	841.31	275
1781	SI1264	830.31	365
1782	SI1263	819.31	185
1783	SI1262	808.31	275
1784	SI1261	797.32	365
1785	SI1260	786.32	185
1786	SI1259	775.32	275
1787	SI1258	764.32	365
1788	SI1257	753.33	185
1789	SI1256	742.33	275
1790	SI1255	731.33	365
1791	SI1254	720.33	185
1792	SI1253	709.34	275
1793	SI1252	698.34	365
1794	SI1251	687.34	185
1795	SI1250	676.34	275
1796	SI1249	665.35	365
1797	SI1248	654.35	185
1798	SI1247	643.35	275
1799	SI1246	632.35	365
1800	SI1245	621.36	185

No.	Name	X	Y
1801	SI1244	610.36	275
1802	SI1243	599.36	365
1803	SI1242	588.36	185
1804	SI1241	577.37	275
1805	SI1240	566.37	365
1806	SI1239	555.37	185
1807	SI1238	544.37	275
1808	SI1237	533.38	365
1809	SI1236	522.38	185
1810	SI1235	511.38	275
1811	SI1234	500.38	365
1812	SI1233	489.39	185
1813	SI1232	478.39	275
1814	SI1231	467.39	365
1815	SI1230	456.39	185
1816	SI1229	445.4	275
1817	SI1228	434.4	365
1818	SI1227	423.4	185
1819	SI1226	412.4	275
1820	SI1225	401.41	365
1821	SI1224	390.41	185
1822	SI1223	379.41	275
1823	SI1222	368.41	365
1824	SI1221	357.42	185
1825	SI1220	346.42	275
1826	SI1219	335.42	365
1827	SI1218	324.42	185
1828	SI1217	313.43	275
1829	SI1216	302.43	365
1830	SI1215	291.43	185
1831	SI1214	280.43	275
1832	SI1213	269.44	365
1833	SI1212	258.44	185
1834	SI1211	247.44	275
1835	SI1210	236.44	365
1836	SI1209	225.45	185
1837	SI1208	214.45	275
1838	SI1207	203.45	365
1839	SI1206	192.45	185
1840	SI1205	181.46	275
1841	SI1204	170.46	365
1842	SI1203	159.46	185
1843	SI1202	148.46	275
1844	SI1201	137.47	365
1845	DUMMY29	126.47	185
1846	DUMMY30	115.47	275
1847	DUMMY31	104.47	365
1848	DUMMY32	93.48	185
1849	DUMMY33	82.48	275
1850	DUMMY34	71.48	365
1851	DUMMY35	60.48	185
1852	DUMMY36	49.49	275
1853	DUMMY37	38.49	365
1854	DUMMY38	27.49	185
1855	DUMMY39	16.49	275
1856	DUMMY40	5.5	365
1857	DUMMY41	-5.5	185
1858	DUMMY42	-16.49	275
1859	DUMMY43	-27.49	365
1860	DUMMY44	-38.49	185
1861	DUMMY45	-49.49	275
1862	DUMMY46	-60.48	365
1863	DUMMY47	-71.48	185
1864	DUMMY48	-82.48	275
1865	DUMMY49	-93.48	365
1866	DUMMY50	-104.47	185
1867	DUMMY51	-115.47	275
1868	DUMMY52	-126.47	365
1869	SI1200	-137.47	185
1870	SI1199	-148.46	275
1871	SI1198	-159.46	365
1872	SI1197	-170.46	185
1873	SI1196	-181.46	275
1874	SI1195	-192.45	365
1875	SI1194	-203.45	185
1876	SI1193	-214.45	275
1877	SI1192	-225.4	

No.	Name	X	Y
2001	SI10681	-1589.14	185
2002	SI10671	-1600.13	275
2003	SI10661	-1611.13	365
2004	SI10651	-1622.13	185
2005	SI10641	-1633.13	275
2006	SI10631	-1644.12	365
2007	SI10621	-1655.12	185
2008	SI10611	-1666.12	275
2009	SI10601	-1677.12	365
2010	SI10591	-1688.11	185
2011	SI10581	-1699.11	275
2012	SI10571	-1710.11	365
2013	SI10561	-1721.11	185
2014	SI10551	-1732.11	275
2015	SI10541	-1743.11	365
2016	SI10531	-1754.11	185
2017	SI10521	-1765.11	275
2018	SI10511	-1776.09	365
2019	SI10501	-1787.09	185
2020	SI10491	-1798.09	275
2021	SI10481	-1809.09	365
2022	SI10471	-1820.08	185
2023	SI10461	-1831.08	275
2024	SI10451	-1842.08	365
2025	SI10441	-1853.08	185
2026	SI10431	-1864.07	275
2027	SI10421	-1875.07	365
2028	SI10411	-1886.07	185
2029	SI10401	-1897.07	275
2030	SI10391	-1908.06	365
2031	SI10381	-1919.06	185
2032	SI10371	-1930.06	275
2033	SI10361	-1941.06	365
2034	SI10351	-1952.05	185
2035	SI10341	-1963.05	275
2036	SI10331	-1974.05	365
2037	SI10321	-1985.05	185
2038	SI10311	-1996.04	275
2039	SI10301	-2007.04	365
2040	SI10291	-2018.04	185
2041	SI10281	-2029.04	275
2042	SI10271	-2040.03	365
2043	SI10261	-2051.03	185
2044	SI10251	-2062.03	275
2045	SI10241	-2073.03	365
2046	SI10231	-2084.02	185
2047	SI10221	-2095.02	275
2048	SI10211	-2106.02	365
2049	SI10201	-2117.02	185
2050	SI10191	-2128.01	275
2051	SI10181	-2139.01	365
2052	SI10171	-2150.01	185
2053	SI10161	-2161.01	275
2054	SI10151	-2172.01	365
2055	SI10141	-2183.01	185
2056	SI10131	-2194.01	275
2057	SI10121	-2205.01	365
2058	SI10111	-2215.99	185
2059	SI10101	-2226.99	275
2060	SI10091	-2237.99	365
2061	SI10081	-2248.99	185
2062	SI10071	-2259.98	275
2063	SI10061	-2270.98	365
2064	SI10051	-2281.98	185
2065	SI10041	-2292.98	275
2066	SI10031	-2303.97	365
2067	SI10021	-2314.97	185
2068	SI10011	-2325.97	275
2069	SI10001	-2336.97	365
2070	SI9991	-2347.96	185
2071	SI9981	-2358.96	275
2072	SI9971	-2369.96	365
2073	SI9961	-2380.96	185
2074	SI9951	-2391.95	275
2075	SI9941	-2402.95	365
2076	SI9931	-2413.95	185
2077	SI9921	-2424.95	275
2078	SI9911	-2435.94	365
2079	SI9901	-2446.94	185
2080	SI9891	-2457.94	275
2081	SI9881	-2468.94	365
2082	SI9871	-2479.93	185
2083	SI9861	-2490.93	275
2084	SI9851	-2501.93	365
2085	SI9841	-2512.93	185
2086	SI9831	-2523.92	275
2087	SI9821	-2534.92	365
2088	SI9811	-2545.92	185
2089	SI9801	-2556.92	275
2090	SI9791	-2567.91	365
2091	SI9781	-2578.91	185
2092	SI9771	-2589.91	275
2093	SI9761	-2600.91	365
2094	SI9751	-2611.91	185
2095	SI9741	-2622.91	275
2096	SI9731	-2633.91	365
2097	SI9721	-2644.91	185
2098	SI9711	-2655.89	275
2099	SI9701	-2666.89	365
2100	SI9691	-2677.89	185

No.	Name	X	Y
2101	SI9681	-2688.89	275
2102	SI9671	-2699.88	365
2103	SI9661	-2710.88	185
2104	SI9651	-2721.88	275
2105	SI9641	-2732.88	365
2106	SI9631	-2743.87	185
2107	SI9621	-2754.87	275
2108	SI9611	-2765.87	365
2109	SI9601	-2776.87	185
2110	SI9591	-2787.86	275
2111	SI9581	-2798.86	365
2112	SI9571	-2809.86	185
2113	SI9561	-2820.86	275
2114	SI9551	-2831.85	365
2115	SI9541	-2842.85	185
2116	SI9531	-2853.85	275
2117	SI9521	-2864.85	365
2118	SI9511	-2875.84	185
2119	SI9501	-2886.84	275
2120	SI9491	-2897.84	365
2121	SI9481	-2908.84	185
2122	SI9471	-2919.83	275
2123	SI9461	-2930.83	365
2124	SI9451	-2941.83	185
2125	SI9441	-2952.83	275
2126	SI9431	-2963.82	365
2127	SI9421	-2974.82	185
2128	SI9411	-2985.82	275
2129	SI9401	-2996.82	365
2130	SI9391	-3007.81	185
2131	SI9381	-3018.81	275
2132	SI9371	-3029.81	365
2133	SI9361	-3040.81	185
2134	SI9351	-3051.8	275
2135	SI9341	-3062.8	365
2136	SI9331	-3073.8	185
2137	SI9321	-3084.8	275
2138	SI9311	-3095.79	365
2139	SI9301	-3106.79	185
2140	SI9291	-3117.79	275
2141	SI9281	-3128.79	365
2142	SI9271	-3139.78	185
2143	SI9261	-3150.78	275
2144	SI9251	-3161.78	365
2145	SI9241	-3172.78	185
2146	SI9231	-3183.77	275
2147	SI9221	-3194.77	365
2148	SI9211	-3205.77	185
2149	SI9201	-3216.77	275
2150	SI9191	-3227.76	365
2151	SI9181	-3238.76	185
2152	SI9171	-3249.76	275
2153	SI9161	-3260.76	365
2154	SI9151	-3271.75	185
2155	SI9141	-3282.75	275
2156	SI9131	-3293.75	365
2157	SI9121	-3304.75	185
2158	SI9111	-3315.74	275
2159	SI9101	-3326.74	365
2160	SI9091	-3337.74	185
2161	SI9081	-3348.74	275
2162	SI9071	-3359.73	365
2163	SI9061	-3370.73	185
2164	SI9051	-3381.73	275
2165	SI9041	-3392.73	365
2166	SI9031	-3403.72	185
2167	SI9021	-3414.72	275
2168	SI9011	-3425.72	365
2169	SI9001	-3436.72	185
2170	SI8991	-3447.71	275
2171	SI8981	-3458.71	365
2172	SI8971	-3469.71	185
2173	SI8961	-3480.71	275
2174	SI8951	-3491.71	365
2175	SI8941	-3502.7	185
2176	SI8931	-3513.7	275
2177	SI8921	-3524.7	365
2178	SI8911	-3535.69	185
2179	SI8901	-3546.69	275
2180	SI8891	-3557.69	365
2181	SI8881	-3568.69	185
2182	SI8871	-3579.68	275
2183	SI8861	-3590.68	365
2184	SI8851	-3601.68	185
2185	SI8841	-3612.68	275
2186	SI8831	-3623.67	365
2187	SI8821	-3634.67	185
2188	SI8811	-3645.67	275
2189	SI8801	-3656.67	365
2190	SI8791	-3667.66	185
2191	SI8781	-3678.66	275
2192	SI8771	-3689.66	365
2193	SI8761	-3700.66	185
2194	SI8751	-3711.65	275
2195	SI8741	-3722.65	365
2196	SI8731	-3733.65	185
2197	SI8721	-3744.65	275
2198	SI8711	-3755.64	365
2199	SI8701	-3766.64	185
2200	SI8691	-3777.64	275

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2201	SI8681	-3788.64	365
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2203	SI8661	-3810.63	275
2204	SI8651	-3821.63	365
2205	SI8641	-3832.63	185
2206	SI8631	-3843.62	275
2207	SI8621	-3854.62	365
2208	SI8611	-3865.62	185
2209	SI8601	-3876.62	275
2210	SI8591	-3887.61	365
2211	SI8581	-3898.61	185
2212	SI8571	-3909.61	275
2213	SI8561	-3920.61	365
2214	SI8551	-3931.6	185
2215	SI8541	-3942.6	275
2216	SI8531	-3953.6	365
2217	SI8521	-3964.6	185
2218	SI8511	-3975.59	275
2219	SI8501	-3986.59	365
2220	SI8491	-3997.59	185
2221	SI8481	-4008.59	275
2222	SI8471	-4019.58	365
2223	SI8461	-4030.58	185
2224	SI8451	-4041.58	275
2225	SI8441	-4052.58	365
2226	SI8431	-4063.57	185
2227	SI8421	-4074.57	275
2228	SI8411	-4085.57	365
2229	SI8401	-4096.57	185
2230	SI8391	-4107.56	275
2231	SI8381	-4118.56	365
2232	SI8371	-4129.56	185
2233	SI8361	-4140.56	275
2234	SI8351	-4151.55	365
2235	SI8341	-4162.55	185
2236	SI8331	-4173.55	275
2237	SI8321	-4184.55	365
2238	SI8311	-4195.54	185
2239	SI8301	-4206.54	275
2240	SI8291	-4217.54	365
2241	SI8281	-4228.54	185
2242	SI8271	-4239.53	275
2243	SI8261	-4250.53	365
2244	SI8251	-4261.53	185
2245	SI8241	-4272.53	275
2246	SI8231	-4283.52	365
2247	SI8221	-4294.52	185
2248	SI8211	-4305.52	275
2249	SI8201	-4316.52	365
2250	SI8191	-4327.51	185
2251	SI8181	-4338.51	275
2252	SI8171	-4349.51	365
2253	SI8161	-4360.51	185
2254	SI8151	-4371.5	275
2255	SI8141	-4382.5	365
2256	SI8131	-4393.5	185
2257	SI8121	-4404.5	275
2258	SI8111	-4415.49	365
2259	SI8101	-4426.49	185
2260	SI8091	-4437.49	275
2261	SI8081	-4448.49	365
2262	SI8071	-4459.48	185
2263	SI8061	-4470.48	275
2264	SI8051	-4481.48	365
2265	SI8041	-4492.48	185
2266	SI8031	-4503.47	275
2267	SI8021	-4514.47	365
2268	SI8011	-4525.47	185
2269	SI8001	-4536.47	275
2270	SI7991	-4547.46	365
2271	SI7981	-455	

No.	Name	X	Y
2401	SI6681	-5988.14	275
2402	SI6671	-5999.13	365
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2404	SI6651	-6021.13	275
2405	SI6641	-6032.13	365
2406	SI6631	-6043.12	185
2407	SI6621	-6054.12	275
2408	SI6611	-6065.12	365
2409	SI6601	-6076.12	185
2410	SI6591	-6087.11	275
2411	SI6581	-6098.11	365
2412	SI6571	-6109.11	185
2413	SI6561	-6120.11	275
2414	SI6551	-6131.11	365
2415	SI6541	-6142.11	185
2416	SI6531	-6153.11	275
2417	SI6521	-6164.11	365
2418	SI6511	-6175.09	185
2419	SI6501	-6186.09	275
2420	SI6491	-6197.09	365
2421	SI6481	-6208.09	185
2422	SI6471	-6219.08	275
2423	SI6461	-6230.08	365
2424	SI6451	-6241.08	185
2425	SI6441	-6252.08	275
2426	SI6431	-6263.07	365
2427	SI6421	-6274.07	185
2428	SI6411	-6285.07	275
2429	SI6401	-6296.07	365
2430	SI6391	-6307.06	185
2431	SI6381	-6318.06	275
2432	SI6371	-6329.06	365
2433	SI6361	-6340.06	185
2434	SI6351	-6351.05	275
2435	SI6341	-6362.05	365
2436	SI6331	-6373.05	185
2437	SI6321	-6384.05	275
2438	SI6311	-6395.04	365
2439	SI6301	-6406.04	185
2440	SI6291	-6417.04	275
2441	SI6281	-6428.04	365
2442	SI6271	-6439.03	185
2443	SI6261	-6450.03	275
2444	SI6251	-6461.03	365
2445	SI6241	-6472.03	185
2446	SI6231	-6483.02	275
2447	SI6221	-6494.02	365
2448	SI6211	-6505.02	185
2449	SI6201	-6516.02	275
2450	SI6191	-6527.01	365
2451	SI6181	-6538.01	185
2452	SI6171	-6549.01	275
2453	SI6161	-6560.01	365
2454	SI6151	-6571.01	185
2455	SI6141	-6582.01	275
2456	SI6131	-6593.01	365
2457	SI6121	-6604.01	185
2458	SI6111	-6614.99	275
2459	SI6101	-6625.99	365
2460	SI6091	-6636.99	185
2461	SI6081	-6647.99	275
2462	SI6071	-6658.98	365
2463	SI6061	-6669.98	185
2464	SI6051	-6680.98	275
2465	SI6041	-6691.98	365
2466	SI6031	-6702.97	185
2467	SI6021	-6713.97	275
2468	SI6011	-6724.97	365
2469	DUMMY53	-6735.97	185
2470	DUMMY54	-6746.96	275
2471	DUMMY55	-6757.96	365
2472	DUMMY56	-6768.96	185
2473	DUMMY57	-6779.96	275
2474	DUMMY58	-6790.95	365
2475	DUMMY59	-6801.95	185
2476	DUMMY60	-6812.95	275
2477	DUMMY61	-6823.95	365
2478	DUMMY62	-6834.94	185
2479	DUMMY63	-6845.94	275
2480	DUMMY64	-6856.94	365
2481	DUMMY65	-6867.94	185
2482	DUMMY66	-6878.93	275
2483	DUMMY67	-6889.93	365
2484	DUMMY68	-6900.93	185
2485	DUMMY69	-6911.93	275
2486	DUMMY70	-6922.92	365
2487	SI6001	-6933.92	185
2488	SI5991	-6944.92	275
2489	SI5981	-6955.92	365
2490	SI5971	-6966.91	185
2491	SI5961	-6977.91	275
2492	SI5951	-6988.91	365
2493	SI5941	-6999.91	185
2494	SI5931	-7010.91	275
2495	SI5921	-7021.91	365
2496	SI5911	-7032.91	185
2497	SI5901	-7043.91	275
2498	SI5891	-7054.89	365
2499	SI5881	-7065.89	185
2500	SI5871	-7076.89	275

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2501	SI5861	-7087.89	365
2502	SI5851	-7098.88	185
2503	SI5841	-7109.88	275
2504	SI5831	-7120.88	365
2505	SI5821	-7131.88	185
2506	SI5811	-7142.87	275
2507	SI5801	-7153.87	365
2508	SI5791	-7164.87	185
2509	SI5781	-7175.87	275
2510	SI5771	-7186.86	365
2511	SI5761	-7197.86	185
2512	SI5751	-7208.86	275
2513	SI5741	-7219.86	365
2514	SI5731	-7230.85	185
2515	SI5721	-7241.85	275
2516	SI5711	-7252.85	365
2517	SI5701	-7263.85	185
2518	SI5691	-7274.84	275
2519	SI5681	-7285.84	365
2520	SI5671	-7296.84	185
2521	SI5661	-7307.84	275
2522	SI5651	-7318.83	365
2523	SI5641	-7329.83	185
2524	SI5631	-7340.83	275
2525	SI5621	-7351.83	365
2526	SI5611	-7362.82	185
2527	SI5601	-7373.82	275
2528	SI5591	-7384.82	365
2529	SI5581	-7395.82	185
2530	SI5571	-7406.81	275
2531	SI5561	-7417.81	365
2532	SI5551	-7428.81	185
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2534	SI5531	-7450.81	365
2535	SI5521	-7461.81	185
2536	SI5511	-7472.81	275
2537	SI5501	-7483.81	365
2538	SI5491	-7494.79	185
2539	SI5481	-7505.79	275
2540	SI5471	-7516.79	365
2541	SI5461	-7527.79	185
2542	SI5451	-7538.78	275
2543	SI5441	-7549.78	365
2544	SI5431	-7560.78	185
2545	SI5421	-7571.78	275
2546	SI5411	-7582.77	365
2547	SI5401	-7593.77	185
2548	SI5391	-7604.77	275
2549	SI5381	-7615.77	365
2550	SI5371	-7626.76	185
2551	SI5361	-7637.76	275
2552	SI5351	-7648.76	365
2553	SI5341	-7659.76	185
2554	SI5331	-7670.75	275
2555	SI5321	-7681.75	365
2556	SI5311	-7692.75	185
2557	SI5301	-7703.75	275
2558	SI5291	-7714.74	365
2559	SI5281	-7725.74	185
2560	SI5271	-7736.74	275
2561	SI5261	-7747.74	365
2562	SI5251	-7758.73	185
2563	SI5241	-7769.73	275
2564	SI5231	-7780.73	365
2565	SI5221	-7791.73	185
2566	SI5211	-7802.72	275
2567	SI5201	-7813.72	365
2568	SI5191	-7824.72	185
2569	SI5181	-7835.72	275
2570	SI5171	-7846.71	365
2571	SI5161	-7857.71	185
2572	SI5151	-7868.71	275
2573	SI5141	-7879.71	365
2574	SI5131	-7890.71	185
2575	SI5121	-7901.71	275
2576	SI5111	-7912.71	365
2577	SI5101	-7923.71	185
2578	SI5091	-7934.69	275
2579	SI5081	-7945.69	365
2580	SI5071	-7956.69	185
2581	SI5061	-7967.69	275
2582	SI5051	-7978.68	365
2583	SI5041	-7989.68	185
2584	SI5031	-8000.68	275
2585	SI5021	-8011.68	365
2586	SI5011	-8022.67	185
2587	SI5001	-8033.67	275
2588	SI4991	-8044.67	365
2589	SI4981	-8055.67	185
2590	SI4971	-8066.66	275
2591	SI4961	-8077.66	365
2592	SI4951	-8088.66	185
2593	SI4941	-8099.66	275
2594	SI4931	-8110.65	365
2595	SI4921	-8121.65	185
2596	SI4911	-8132.65	275
2597	SI4901	-8143.65	365
2598	SI4891	-8154.64	185
2599	SI4881	-8165.64	275
2600	SI4871	-8176.64	365

No.	Name	X	Y
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2604	SI4831	-8220.63	185
2605	SI4821	-8231.63	275
2606	SI4811	-8242.62	365
2607	SI4801	-8253.62	185
2608	SI4791	-8264.62	275
2609	SI4781	-8275.62	365
2610	SI4771	-8286.61	185
2611	SI4761	-8297.61	275
2612	SI4751	-8308.61	365
2613	SI4741	-8319.61	185
2614	SI4731	-8330.61	275
2615	SI4721	-8341.61	365
2616	SI4711	-8352.61	185
2617	SI4701	-8363.61	275
2618	SI4691	-8374.59	365
2619	SI4681	-8385.59	185
2620	SI4671	-8396.59	275
2621	SI4661	-8407.59	365
2622	SI4651	-8418.58	185
2623	SI4641	-8429.58	275
2624	SI4631	-8440.58	365
2625	SI4621	-8451.58	185
2626	SI4611	-8462.57	275
2627	SI4601	-8473.57	365
2628	SI4591	-8484.57	185
2629	SI4581	-8495.57	275
2630	SI4571	-8506.56	365
2631	SI4561	-8517.56	185
2632	SI4551	-8528.56	275
2633	SI4541	-8539.56	365
2634	SI4531	-8550.55	185
2635	SI4521	-8561.55	275
2636	SI4511	-8572.55	365
2637	SI4501	-8583.55	185
2638	SI4491	-8594.54	275
2639	SI4481	-8605.54	365
2640	SI4471	-8616.54	185
2641	SI4461	-8627.54	275
2642	SI4451	-8638.53	365
2643	SI4441	-8649.53	185
2644	SI4431	-8660.53	275
2645	SI4421	-8671.53	365
2646	SI4411	-8682.52	185
2647	SI4401	-8693.52	275
2648	SI4391	-8704.52	365
2649	SI4381	-8715.52	185
2650	SI4371	-8726.51	275
2651	SI4361	-8737.51	365
2652	SI4351	-8748.51	185
2653	SI4341	-8759.51	275
2654	SI4331	-8770.51	365
2655	SI4321	-8781.51	185
2656	SI4311	-8792.51	275
2657	SI4301	-8803.51	365
2658	SI4291	-8814.49	185
2659	SI4281	-8825.49	275
2660	SI4271	-8836.49	365
2661	SI4261	-8847.49	185
2662	SI4251	-8858.48	275
2663	SI4241	-8869.48	365
2664	SI4231	-8880.48	185
2665	SI4221	-8891.48	275
2666	SI4211	-8902.47	365
2667	SI4201	-8913.47	185
2668	SI4191	-8924.47	275
2669	SI4181	-8935.47	365
2670	SI4171	-8946.46	185
2671	SI4161	-8957.46	275
2672	SI4151	-8968.46	365
2673	SI4141	-8979	

No.	Name	X	Y
2801	SI2861	-10387.14	365
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2803	SI2841	-10409.13	275
2804	SI2831	-10420.13	365
2805	SI2821	-10431.13	185
2806	SI2811	-10442.12	275
2807	SI2801	-10453.12	365
2808	SI2791	-10464.12	185
2809	SI2781	-10475.12	275
2810	SI2771	-10486.11	365
2811	SI2761	-10497.11	185
2812	SI2751	-10508.11	275
2813	SI2741	-10519.11	365
2814	SI2731	-10530.11	185
2815	SI2721	-10541.1	275
2816	SI2711	-10552.1	365
2817	SI2701	-10563.1	185
2818	SI2691	-10574.09	275
2819	SI2681	-10585.09	365
2820	SI2671	-10596.09	185
2821	SI2661	-10607.09	275
2822	SI2651	-10618.08	365
2823	SI2641	-10629.08	185
2824	SI2631	-10640.08	275
2825	SI2621	-10651.08	365
2826	SI2611	-10662.07	185
2827	SI2601	-10673.07	275
2828	SI2591	-10684.07	365
2829	SI2581	-10695.07	185
2830	SI2571	-10706.06	275
2831	SI2561	-10717.06	365
2832	SI2551	-10728.06	185
2833	SI2541	-10739.06	275
2834	SI2531	-10750.05	365
2835	SI2521	-10761.05	185
2836	SI2511	-10772.05	275
2837	SI2501	-10783.05	365
2838	SI2491	-10794.04	185
2839	SI2481	-10805.04	275
2840	SI2471	-10816.04	365
2841	SI2461	-10827.04	185
2842	SI2451	-10838.03	275
2843	SI2441	-10849.03	365
2844	SI2431	-10860.03	185
2845	SI2421	-10871.03	275
2846	SI2411	-10882.02	365
2847	SI2401	-10893.02	185
2848	SI2391	-10904.02	275
2849	SI2381	-10915.02	365
2850	SI2371	-10926.01	185
2851	SI2361	-10937.01	275
2852	SI2351	-10948.01	365
2853	SI2341	-10959.01	185
2854	SI2331	-10970	275
2855	SI2321	-10981	365
2856	SI2311	-10992	185
2857	SI2301	-11003	275
2858	SI2291	-11013.99	365
2859	SI2281	-11024.99	185
2860	SI2271	-11035.99	275
2861	SI2261	-11046.99	365
2862	SI2251	-11057.98	185
2863	SI2241	-11068.98	275
2864	SI2231	-11079.98	365
2865	SI2221	-11090.98	185
2866	SI2211	-11101.97	275
2867	SI2201	-11112.97	365
2868	SI2191	-11123.97	185
2869	SI2181	-11134.97	275
2870	SI2171	-11145.96	365
2871	SI2161	-11156.96	185
2872	SI2151	-11167.96	275
2873	SI2141	-11178.96	365
2874	SI2131	-11189.95	185
2875	SI2121	-11200.95	275
2876	SI2111	-11211.95	365
2877	SI2101	-11222.95	185
2878	SI2091	-11233.94	275
2879	SI2081	-11244.94	365
2880	SI2071	-11255.94	185
2881	SI2061	-11266.94	275
2882	SI2051	-11277.93	365
2883	SI2041	-11288.93	185
2884	SI2031	-11299.93	275
2885	SI2021	-11310.93	365
2886	SI2011	-11321.92	185
2887	SI2001	-11332.92	275
2888	SI1991	-11343.92	365
2889	SI1981	-11354.92	185
2890	SI1971	-11365.91	275
2891	SI1961	-11376.91	365
2892	SI1951	-11387.91	185
2893	SI1941	-11398.91	275
2894	SI1931	-11409.91	365
2895	SI1921	-11420.91	185
2896	SI1911	-11431.9	275
2897	SI1901	-11442.9	365
2898	SI1891	-11453.89	185
2899	SI1881	-11464.89	275
2900	SI1871	-11475.89	365

No.	Name	X	Y
2901	SI1861	-11486.89	185
2902	SI1851	-11497.88	275
2903	SI1841	-11508.88	365
2904	SI1831	-11519.88	185
2905	SI1821	-11530.88	275
2906	SI1811	-11541.87	365
2907	SI1801	-11552.87	185
2908	SI1791	-11563.87	275
2909	SI1781	-11574.87	365
2910	SI1771	-11585.86	185
2911	SI1761	-11596.86	275
2912	SI1751	-11607.86	365
2913	SI1741	-11618.86	185
2914	SI1731	-11629.85	275
2915	SI1721	-11640.85	365
2916	SI1711	-11651.85	185
2917	SI1701	-11662.85	275
2918	SI1691	-11673.84	365
2919	SI1681	-11684.84	185
2920	SI1671	-11695.84	275
2921	SI1661	-11706.84	365
2922	SI1651	-11717.83	185
2923	SI1641	-11728.83	275
2924	SI1631	-11739.83	365
2925	SI1621	-11750.83	185
2926	SI1611	-11761.82	275
2927	SI1601	-11772.82	365
2928	SI1591	-11783.82	185
2929	SI1581	-11794.82	275
2930	SI1571	-11805.81	365
2931	SI1561	-11816.81	185
2932	SI1551	-11827.81	275
2933	SI1541	-11838.81	365
2934	SI1531	-11849.8	185
2935	SI1521	-11860.8	275
2936	SI1511	-11871.8	365
2937	SI1501	-11882.8	185
2938	SI1491	-11893.79	275
2939	SI1481	-11904.79	365
2940	SI1471	-11915.79	185
2941	SI1461	-11926.79	275
2942	SI1451	-11937.78	365
2943	SI1441	-11948.78	185
2944	SI1431	-11959.78	275
2945	SI1421	-11970.78	365
2946	SI1411	-11981.77	185
2947	SI1401	-11992.77	275
2948	SI1391	-12003.77	365
2949	SI1381	-12014.77	185
2950	SI1371	-12025.76	275
2951	SI1361	-12036.76	365
2952	SI1351	-12047.76	185
2953	SI1341	-12058.76	275
2954	SI1331	-12069.75	365
2955	SI1321	-12080.75	185
2956	SI1311	-12091.75	275
2957	SI1301	-12102.75	365
2958	SI1291	-12113.74	185
2959	SI1281	-12124.74	275
2960	SI1271	-12135.74	365
2961	SI1261	-12146.74	185
2962	SI1251	-12157.73	275
2963	SI1241	-12168.73	365
2964	SI1231	-12179.73	185
2965	SI1221	-12190.73	275
2966	SI1211	-12201.72	365
2967	SI1201	-12212.72	185
2968	SI1191	-12223.72	275
2969	SI1181	-12234.72	365
2970	SI1171	-12245.71	185
2971	SI1161	-12256.71	275
2972	SI1151	-12267.71	365
2973	SI1141	-12278.71	185
2974	SI1131	-12289.7	275
2975	SI1121	-12300.7	365
2976	SI1111	-12311.7	185
2977	SI1101	-12322.7	275
2978	SI1091	-12333.69	365
2979	SI1081	-12344.69	185
2980	SI1071	-12355.69	275
2981	SI1061	-12366.69	365
2982	SI1051	-12377.68	185
2983	SI1041	-12388.68	275
2984	SI1031	-12399.68	365
2985	SI1021	-12410.68	185
2986	SI1011	-12421.67	275
2987	SI1001	-12432.67	365
2988	SI991	-12443.67	185
2989	SI981	-12454.67	275
2990	SI971	-12465.66	365
2991	SI961	-12476.66	185
2992	SI951	-12487.66	275
2993	SI941	-12498.66	365
2994	SI931	-12509.65	185
2995	SI921	-12520.65	275
2996	SI911	-12531.65	365
2997	SI901	-12542.65	185
2998	SI891	-12553.64	275
2999	SI881	-12564.64	365
3000	SI871	-12575.64	185

No.	Name	X	Y
3001	SI861	-12586.64	275
3002	SI851	-12597.63	365
3003	SI841	-12608.63	185
3004	SI831	-12619.63	275
3005	SI821	-12630.63	365
3006	SI811	-12641.62	185
3007	SI801	-12652.62	275
3008	SI791	-12663.62	365
3009	SI781	-12674.62	185
3010	SI771	-12685.61	275
3011	SI761	-12696.61	365
3012	SI751	-12707.61	185
3013	SI741	-12718.61	275
3014	SI731	-12729.6	365
3015	SI721	-12740.6	185
3016	SI711	-12751.6	275
3017	SI701	-12762.6	365
3018	SI691	-12773.59	185
3019	SI681	-12784.59	275
3020	SI671	-12795.59	365
3021	SI661	-12806.59	185
3022	SI651	-12817.58	275
3023	SI641	-12828.58	365
3024	SI631	-12839.58	185
3025	SI621	-12850.58	275
3026	SI611	-12861.57	365
3027	SI601	-12872.57	185
3028	SI591	-12883.57	275
3029	SI581	-12894.57	365
3030	SI571	-12905.56	185
3031	SI561	-12916.56	275
3032	SI551	-12927.56	365
3033	SI541	-12938.56	185
3034	SI531	-12949.55	275
3035	SI521	-12960.55	365
3036	SI511	-12971.55	185
3037	SI501	-12982.55	275
3038	SI491	-12993.54	365
3039	SI481	-13004.54	185
3040	SI471	-13015.54	275
3041	SI461	-13026.54	365
3042	SI451	-13037.53	185
3043	SI441	-13048.53	275
3044	SI431	-13059.53	365
3045	SI421	-13070.53	185
3046	SI411	-13081.52	275
3047	SI401	-13092.52	365
3048	SI391	-13103.52	185
3049	SI381	-13114.52	275
3050	SI371	-13125.51	365
3051	SI361	-13136.51	185
3052	SI351	-13147.51	275
3053	SI341	-13158.51	365
3054	SI331	-13169.5	185
3055	SI321	-13180.5	275
3056	SI311	-13191.5	365
3057	SI301	-13202.5	185
3058	SI291	-13213.49	275
3059	SI281	-13224.49	365
3060	SI271	-13235.49	185
3061	SI261	-13246.49	275
3062	SI251	-13257.48	365
3063	SI241	-13268.48	185
3064	SI231	-13279.48	275
3065	SI221	-13290.48	365
3066	SI211	-13301.47	185
3067	SI201	-13312.47	275
3068	SI191	-13323.47	365
3069			

4. System Interface

4.1. DSI System Interface

4.1.1. General Description

The pad mapping of MIPI DSI interface is set by IM[2:0] pin, LANSEL pins and MIPI_LANE_SEL register(as below table).

Table 2: DSI Interface Lane Mode Selection

External Pad Set				Register	Configuration of MIPI Lane				
LANSEL	IM2	IM1	IM0	Page4_R00h MIPI_LANE_SEL	D0P/N Pin	D1P/N Pin	CLKP/N Pin	D2P/N Pin	D3P/N Pin
0	0	0	0	1	D3P/N	D2P/N	CLKP/N	D1P/N	D0P/N
0	0	0	1	1	D3N/P	D2N/P	CLKN/P	D1N/P	D0N/P
0	0	1	0	1	D0P/N	D1P/N	CLKP/N	D2P/N	D3P/N
0	0	1	1	1	D0N/P	D1N/P	CLKN/P	D2N/P	D3N/P
0	1	0	0	1	D3P/N	D0P/N	CLKP/N	D1P/N	D2P/N
0	1	0	1	1	D3N/P	D0N/P	CLKN/P	D1N/P	D2N/P
0	1	1	0	1	D2P/N	D1P/N	CLKP/N	D0P/N	D3P/N
0	1	1	1	1	D2N/P	D1N/P	CLKN/P	D0N/P	D3N/P
1	0	0	0	1	-	-	CLKP/N	D1P/N	D0P/N
1	0	0	1	1	-	-	CLKN/P	D1N/P	D0N/P
1	0	1	0	1	D0P/N	D1P/N	CLKP/N	-	-
1	0	1	1	1	D0N/P	D1N/P	CLKN/P	-	-
1	1	0	0	1	-	D0P/N	CLKP/N	D1P/N	-
1	1	0	1	1	-	D0N/P	CLKN/P	D1N/P	-
1	1	1	0	1	-	D1P/N	CLKP/N	D0P/N	-
1	1	1	1	1	-	D1N/P	CLKN/P	D0N/P	-
0	0	0	0	0	-	D2P/N	CLKP/N	D1P/N	D0P/N
0	0	0	1	0	-	D2N/P	CLKN/P	D1N/P	D0N/P
0	0	1	0	0	D0P/N	D1P/N	CLKP/N	D2P/N	-
0	0	1	1	0	D0N/P	D1N/P	CLKN/P	D2N/P	-
0	1	0	0	0	-	D0P/N	CLKP/N	D1P/N	D2P/N
0	1	0	1	0	-	D0N/P	CLKN/P	D1N/P	D2N/P
0	1	1	0	0	D2P/N	D1P/N	CLKP/N	D0P/N	-
0	1	1	1	0	D2N/P	D1N/P	CLKN/P	D0N/P	-
Others					Reserved				

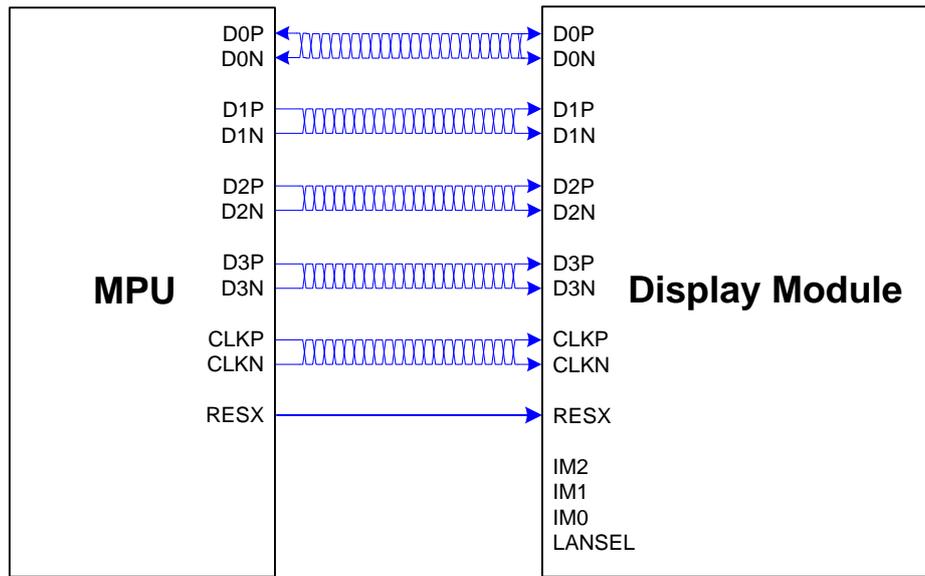


Figure 2: DSI System Interface Diagram

The communication is separated into two different levels between the MCU and the display module:

- ❖ Low level communication is done on the interface level.
- ❖ High level communication is done on the packet level.

4.1.2. Interface Level Communication

4.1.2.1. General

The display module uses data and clock lane differential pairs for DSI (DSI-2M). Both differential lane pairs can be driven to Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in the single ended mode, a differential receiver is disable (a termination resistor of the receiver is disable), and it can be driven into a low power mode.

High Speed mode means that differential pairs (the termination resistor of the receiver is enable) are not used in the single ended mode.

Different modes and protocols are used in each mode when transferring information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Table 3: High Speed and Low-Power Lane Pair State Codes

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low Power	
	DATA_P	DATA_N	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential – 0	Note 1	Note1
HS-1	High (HS)	Low (HS)	Differential – 1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS – Request	Mark - 0
LP-10	High (LP)	Low (LP)	Not Defined	LP - Request	Mark - 1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair will check the LP-00 state code when the Lane Pair is in the High Speed (HS) mode.
2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes the LP-11 state code, then the lane pair will return to LP-11 of the Control Mode.
3. $n = 0, 1, 2$ and 3 (D1P/N, D2 P/N and D3 P/N lanes only for HS-0 and HS-1)

4.1.2.2. DSI CLK Lanes

CLKP/N lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra-Low Power Mode (ULPM) and High Speed Clock Mode (HSCM). Clock lane are in the single ended mode (LP = Low Power) when entering or leaving Low Power Mode (LPM) or Ultra-Low Power Mode (ULPM). Clock lane is in the single ended mode (LP = Low Power) when entering in or leaving High Speed Clock Mode (HSCM). These entering and leaving protocols use Clock lane in the single ended mode to generate an entering or leaving sequence. The principal flow chart of the different Clock lane power modes is illustrated below.

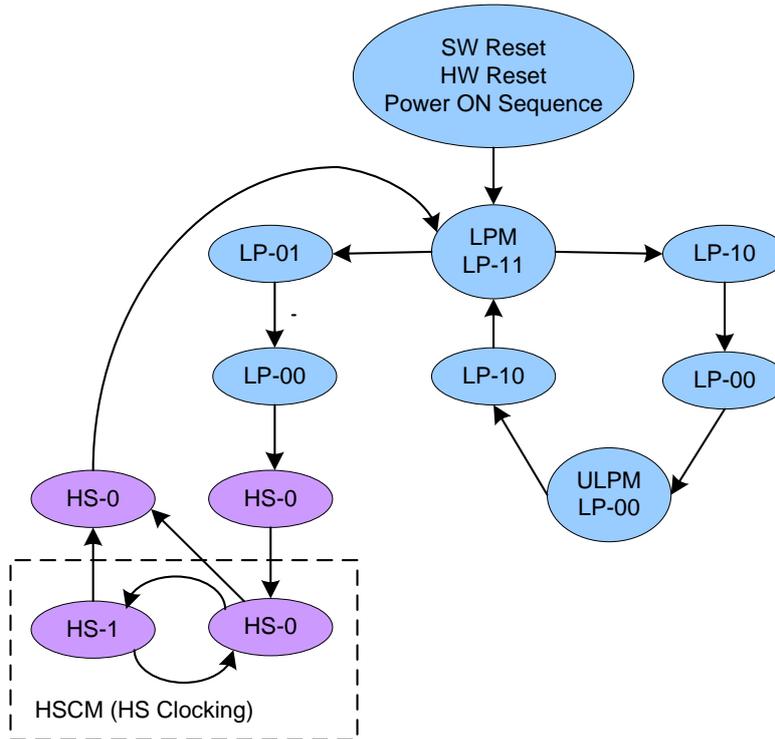


Figure 3: Clock lane Power Modes

4.1.2.2.1. Low Power Mode (LPM)

CLKP/N lanes can be driven to the Low Power Mode (LPM), when CLKP/N lanes enter LP-11 State Code, in three different ways:

- 1) After SW Reset, HW Reset or Power On Sequence => LP-11
- 2) After CLKP/N lanes leave Ultra-Low Power Mode (ULPM, LP-00 State Code) => LP-10 => LP-11 (LPM).

This sequence is illustrated below.

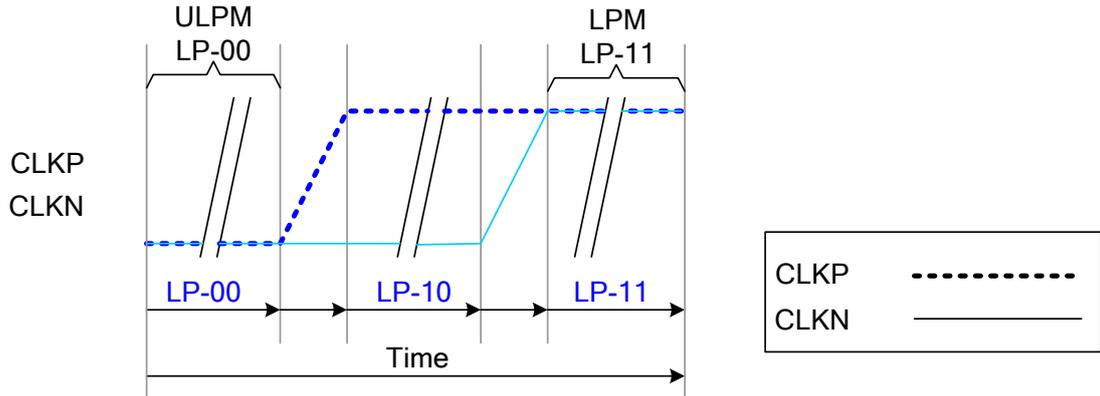


Figure 4: From ULPM to LPM

3) After CLKP/N lanes leave High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) => HS-0=> LP-11 (LPM).

This sequence is illustrated below.

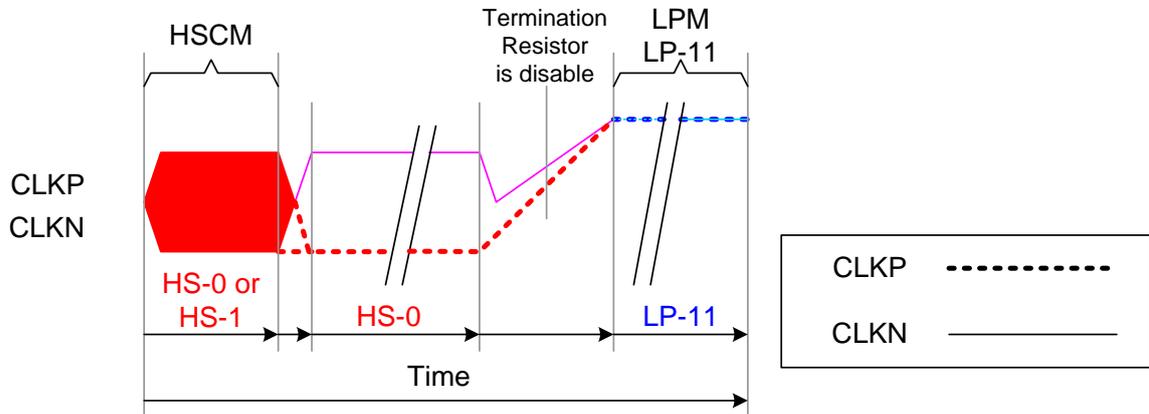


Figure 5: From High Speed Clock Mode (HSCM) to LPM

The changes of all the three modes are illustrated in the flow chart below.

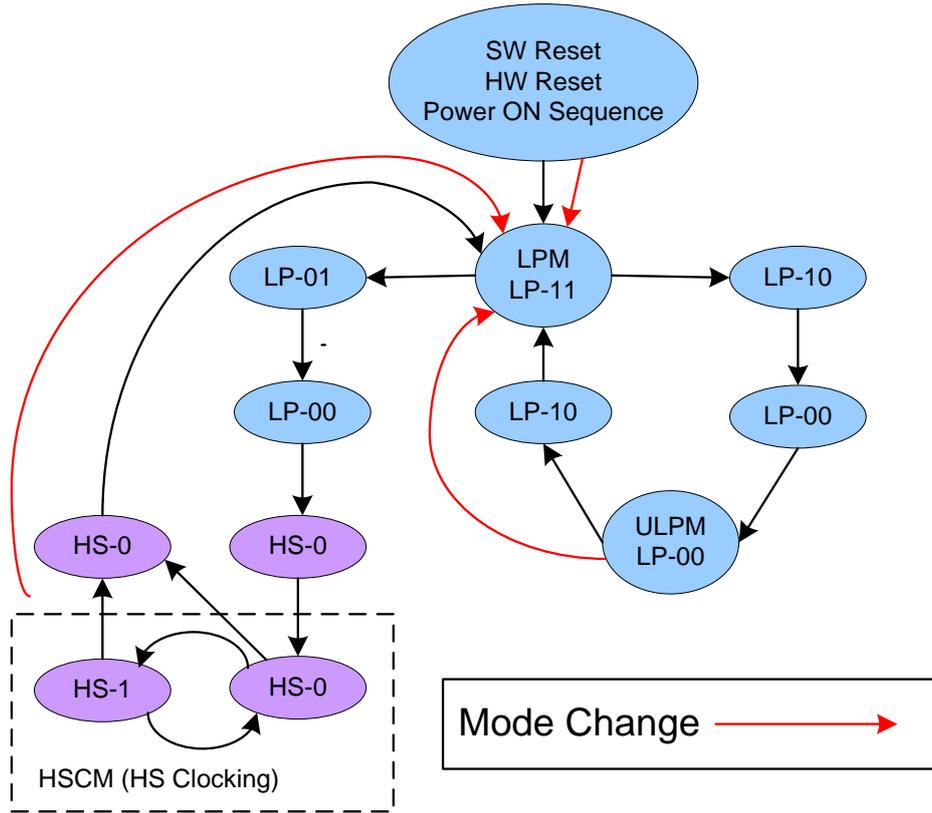


Figure 6: All Three Mode Changes to LPM

4.1.2.2.2. Ultra-Low Power Mode (ULPM)

CLKP/N lanes can be driven to the Ultra-Low power Mode (ULPM) when CLK lanes enter the LP-00 State Code. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-10 => LP-00 (ULPM). This sequence is illustrated below.

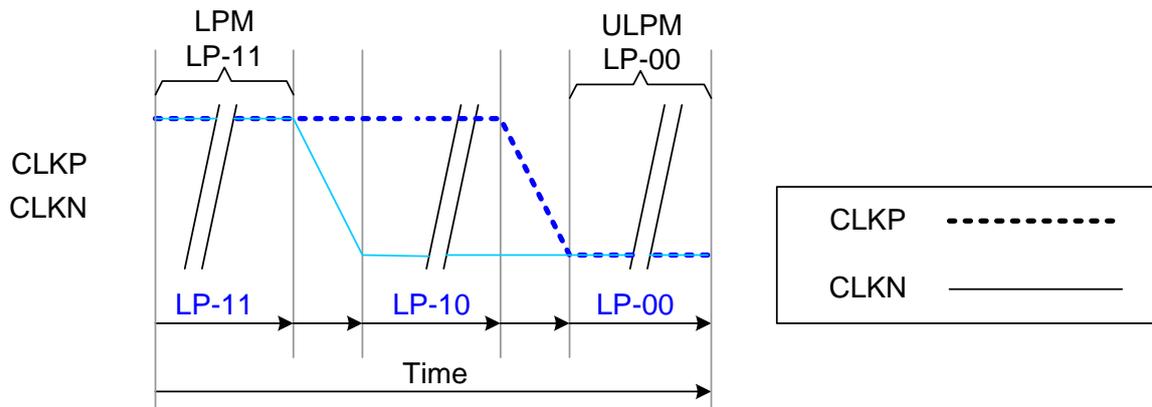


Figure 7: From LPM to ULPM

The mode change is also illustrated below.

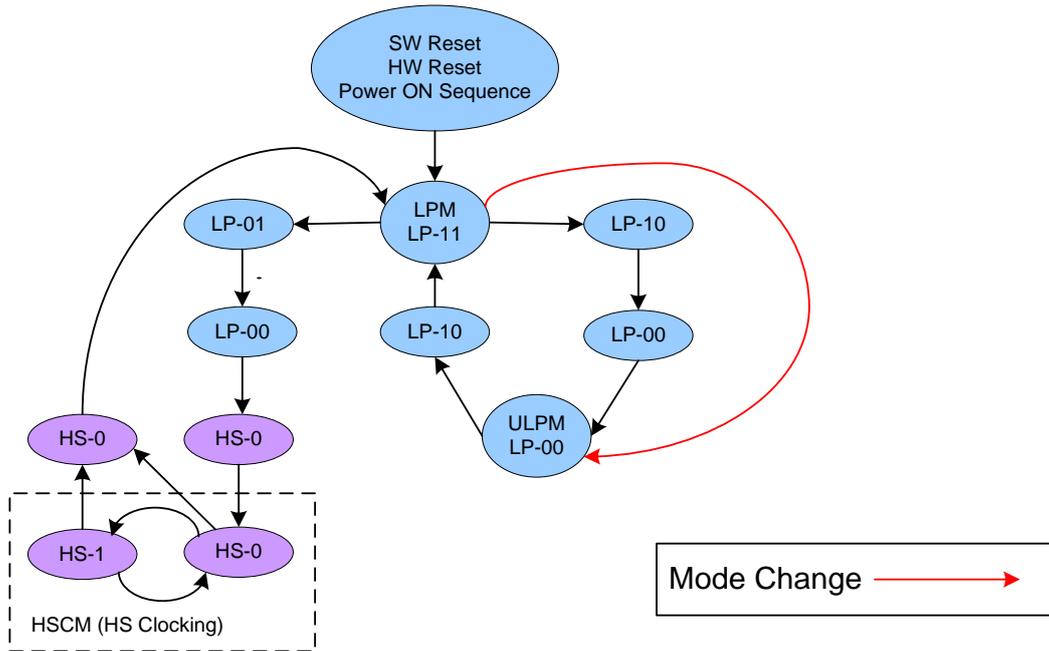


Figure 8: Mode Change from LPM to ULPM

4.1.2.2.3. High-Speed Clock Mode (HSCM)

CLKP/N lanes can be driven to the High Speed Clock Mode (HSCM) when CLK lanes start to function between HS-0 and HS-1 State Codes. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-01 => LP-00 => HS-0 => HS-0/1 (HSCM). This sequence is illustrated below.

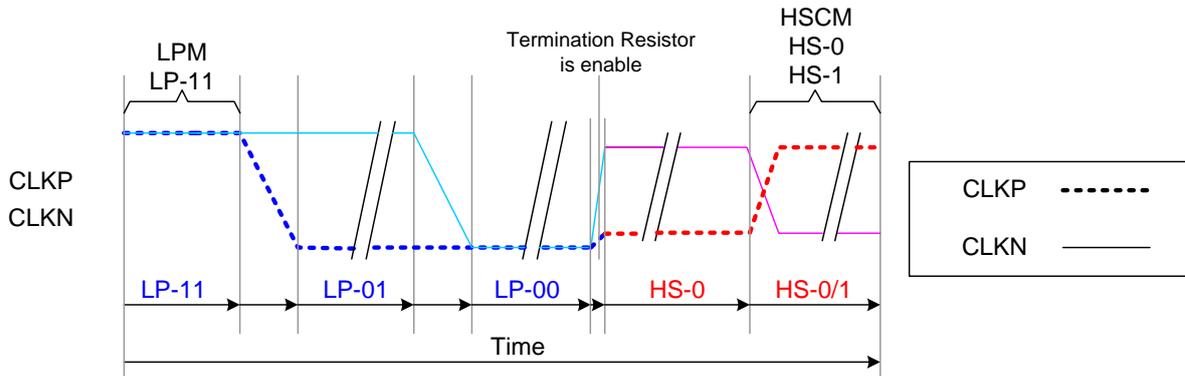


Figure 9: From LPM to HSCM

The mode change is also illustrated below.

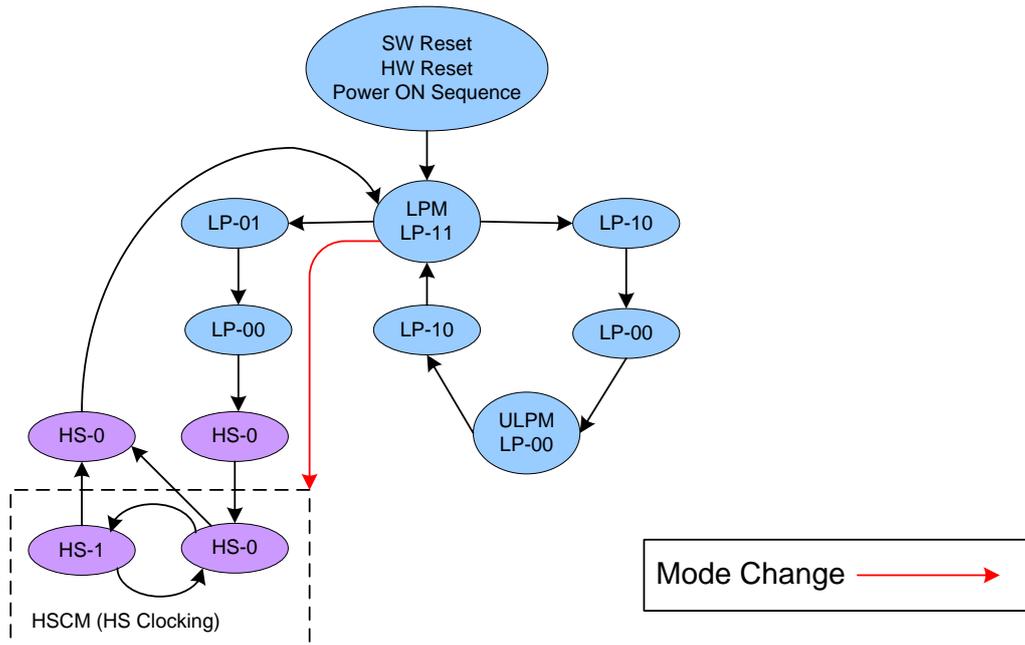


Figure 10: Mode Change from LPM to HSCM

The high speed clock (CLKP/N) starts before high speed data is sent via data lanes. The high speed clock continues clocking after the high speed data sending is stopped.

The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS-0
- End state is HS-0

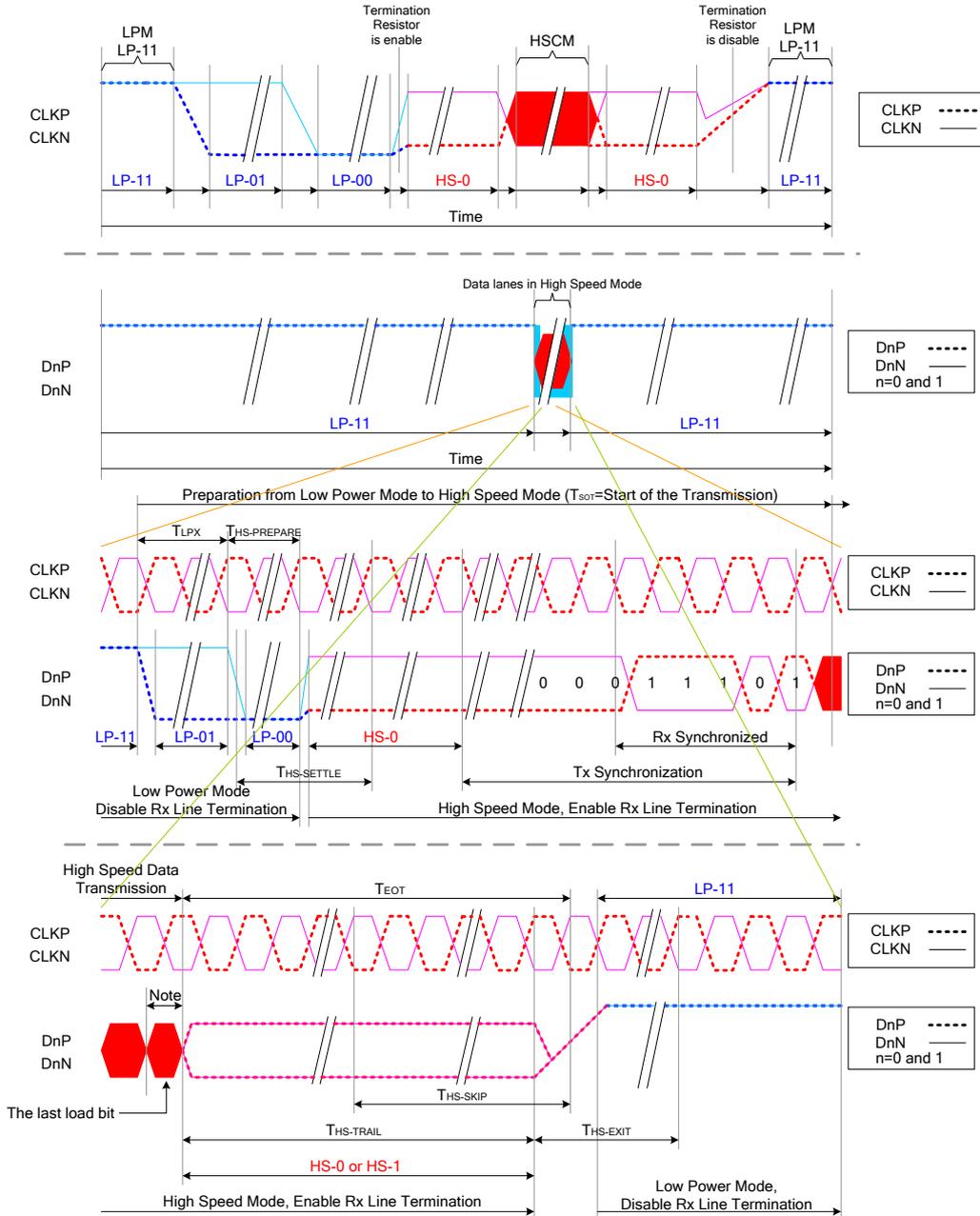


Figure 11: High Speed Clock Burst

Notes:

1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

4.1.2.3. DSI Data Lanes

4.1.2.3.1. General

D3P/N, D2P/N, D1P/N and D0P/N Data Lanes can be driven into different modes:

- Escape Mode (Only D0P/N data lane is used)
- High-Speed Data Transmission (all data lanes are used)
- Bus Turnaround Request (Only D0P/N data lane are used)

These modes and their entering codes are defined in the following table.

Table 4: Entering and Leaving Sequences

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode ¹	LP-11 → LP-10 → LP-00 → LP-01 → LP-00	LP-00 → LP-10 → LP-11 (Mark-1)
High-Speed Data Transmission ²	LP-11 → LP-01 → LP-00 → HS-0	(HS-0 or HS-1) → LP-11
Bus Turnaround Request ³	LP-11 → LP-10 → LP-00 → LP-10 → LP-00	Hi-Z

4.1.2.3.2. Escape Modes

D0P/N data lanes can be used in different Escape Modes when data lanes are in the Low Power (LP) mode. These Escape Modes are used to:

- ◆ Send “Low-Power Data Transmission” (LPDT) from the MCU to the display module,
- ◆ Drive data lanes to “Ultra-Low Power State” (ULPS),
- ◆ Indicate “Remote Application Reset” (RAR), which can reset the display module,
- ◆ Indicate “Acknowledge” (ACK), which is used to transmit a non-error event from the display module to the MCU.

The basic sequence of the Escape Mode is as follows:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Escape Command (EC), which is coded, when one of the data lanes changes from low-to-high-to-low then this changed data lane presents the value of the current data bit (D0P = 1, D0N= 0). When DSI-D0 changes from low-to-high-to-low, the receiver will latch a data bit, which value is logical 0. The receiver will use this low-to-high-to-low transition as its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 => LP-10 => LP-11
- End: LP-11

This basic construction is illustrated below:

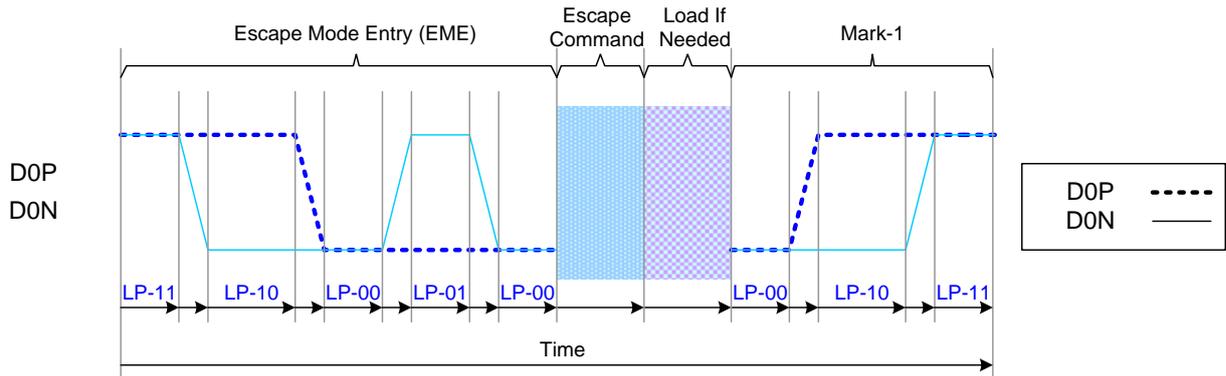


Figure 12 General Escape Mode Sequence

A total of eight Escape Commands (EC) are divided into two types: Mode and Trigger, as shown in Table 5: Escape Commands.

An example of the Mode type Escape Command is 'Ultra-Low Power Mode', where the MCU instructs the display module to enter its Ultra-Low Power Mode.

Escape commands are defined in the following table.

Table 5: Escape Commands

Escape command	Command Type Mode/Trigger	Entry command Pattern (First Bit → Last Bit Transmitted)	Dn	D0
Low-Power Data Transmission	Mode	1110 0001 b	-	X
Ultra-Low Power Mode	Mode	0001 1110 b	X	X
Undefined-1, ^{Note 1}	Mode	1001 1111 b	-	-
Undefined-2, ^{Note 1}	Mode	1101 1110 b	-	-
Remote Application Reset	Trigger	0110 0010 b	-	X
Acknowledge	Trigger	0010 0001 b	-	X
Unknown-5, ^{Note 1}	Trigger	1010 0000 b	-	-

Notes:

1. This Escape command support is not implemented on the display module.
2. n = 1
3. x = Supported
4. - = Not Supported

4.1.2.3.2.1. Low-Power Data Transmission (LPDT)

The MCU can send data to the display module in the Low-Power Data Transmission (LPDT) mode when data lanes enter the Escape Mode and Low-Power Data Transmission (LPDT) command is sent to the display module. The display module also uses the same sequence when it sends data to the MCU. The Low Power Data Transmission (LPDT) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Low-Power Data Transmission (LPDT) command in the Escape Mode: 1110 0001 (first to last bit)
- Load (Data):
 - ✧ One or more bytes (one byte = 8 bit)
 - ✧ Data lanes are in pause mode when data lanes are stopped (both lanes are low) between bytes
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

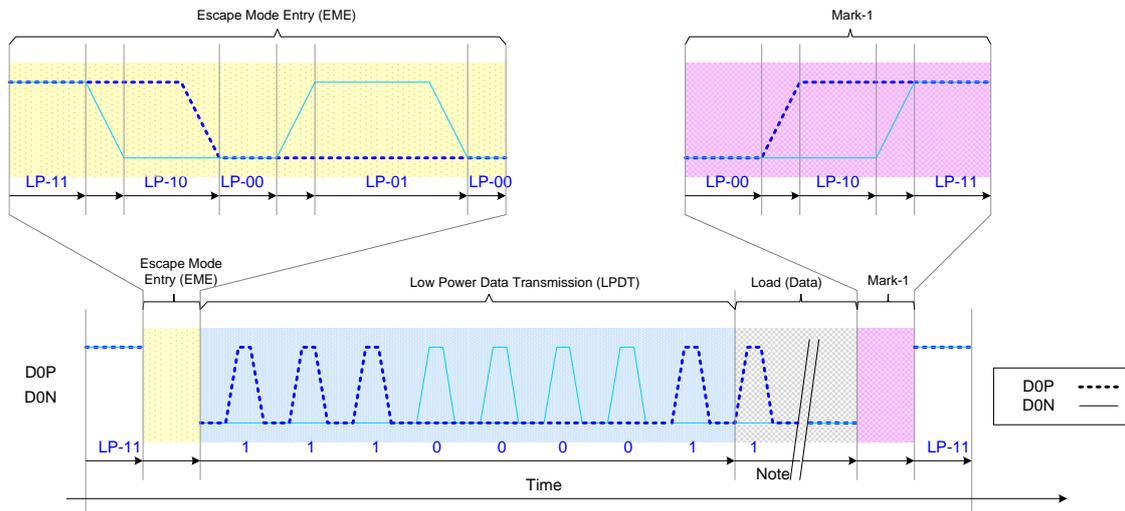


Figure 13: Low-Power Data Transmission (LPDT)

Note: Load (Data) presents that the first bit is the logical 1 in this example.

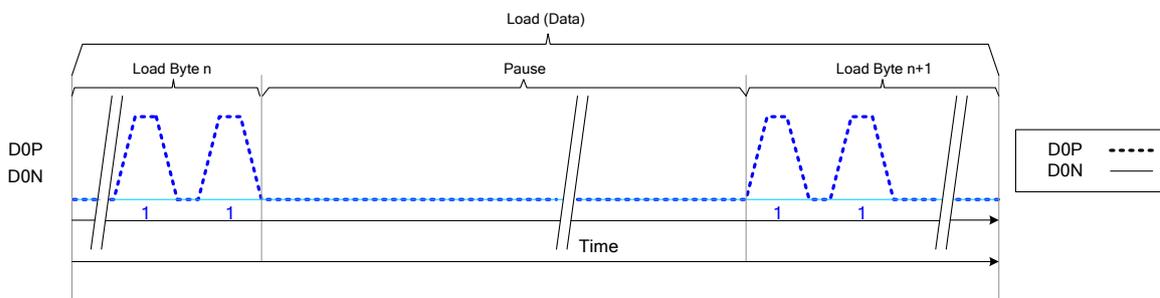


Figure 14: Pause (Example)

4.1.2.3.2.2. Ultra-Low Power State (ULPS)

The MCU can force data lanes get into the Ultra-Low Power State (ULPS) mode when data lanes enter the Escape Mode. The Ultra-Low Power State (ULPS) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Ultra-Low Power State (ULPS) command in the Escape Mode: 0001 1110 (first to last bit)
- Ultra-Low Power State (ULPS) when the MCU keeps data lanes low
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11 (Next command must wait 100us after data lanes leave ULPS)

This sequence is illustrated for reference purposes below:

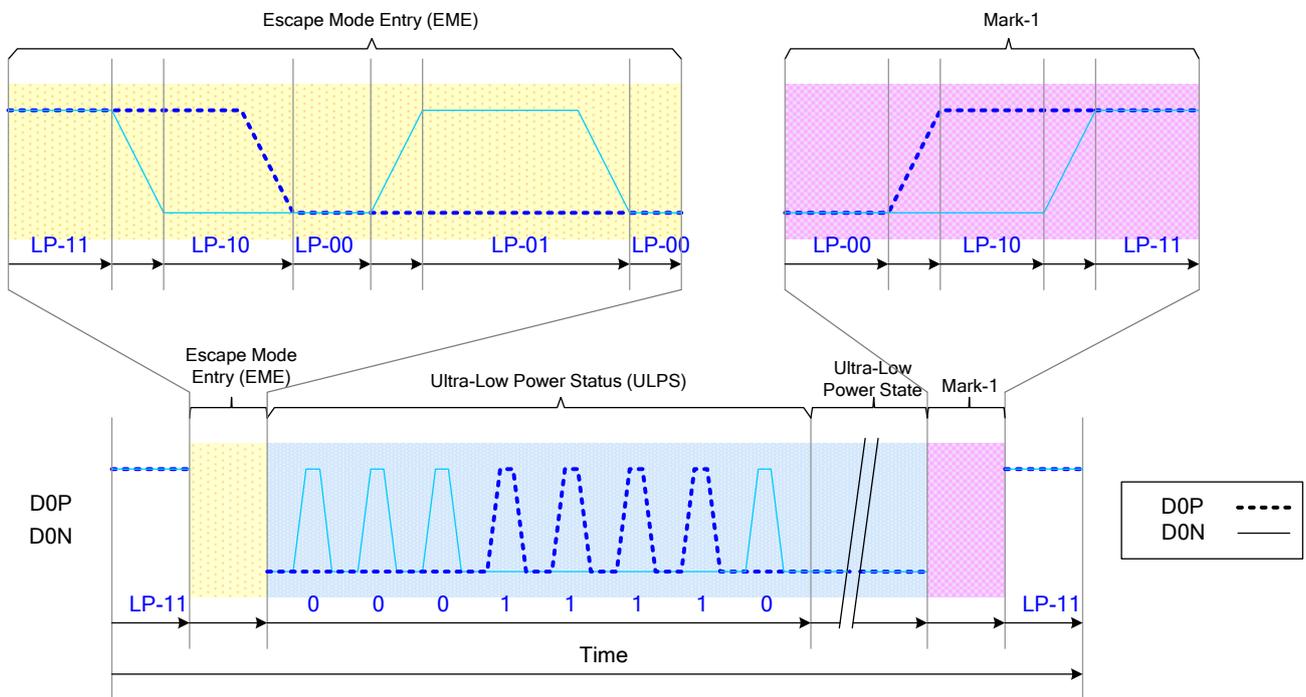


Figure 15: Ultra-Low Power State (ULPS)

4.1.2.3.2.3. Remote Application Reset (RAR)

The MCU can inform the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes enter the Escape Mode. The Remote Application Reset (RAR) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

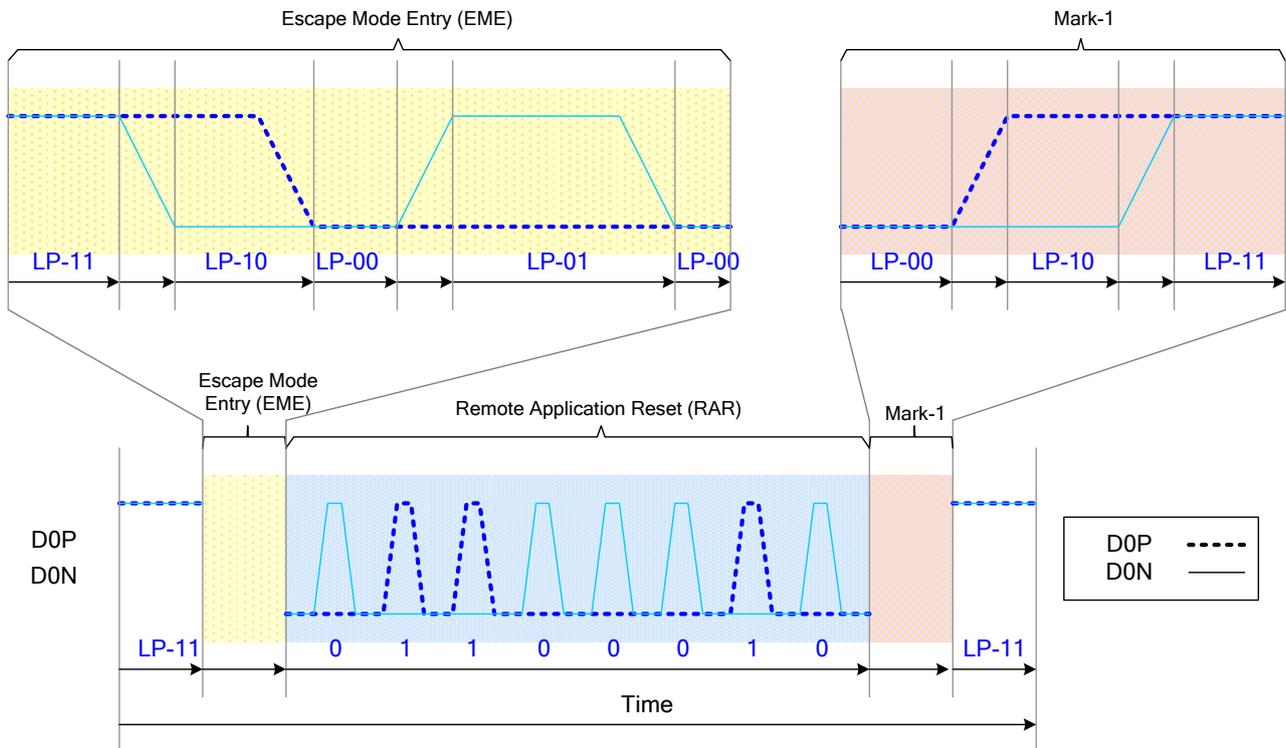


Figure 16: Remote Application Reset (RAR)

4.1.2.3.2.4. Acknowledge (ACK)

The display module can inform the MCU an error is not recognized by Acknowledge (ACK). The display module sends the Acknowledge (ACK) with the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Acknowledge (ACK) command in the Escape Mode: 0010 0001 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

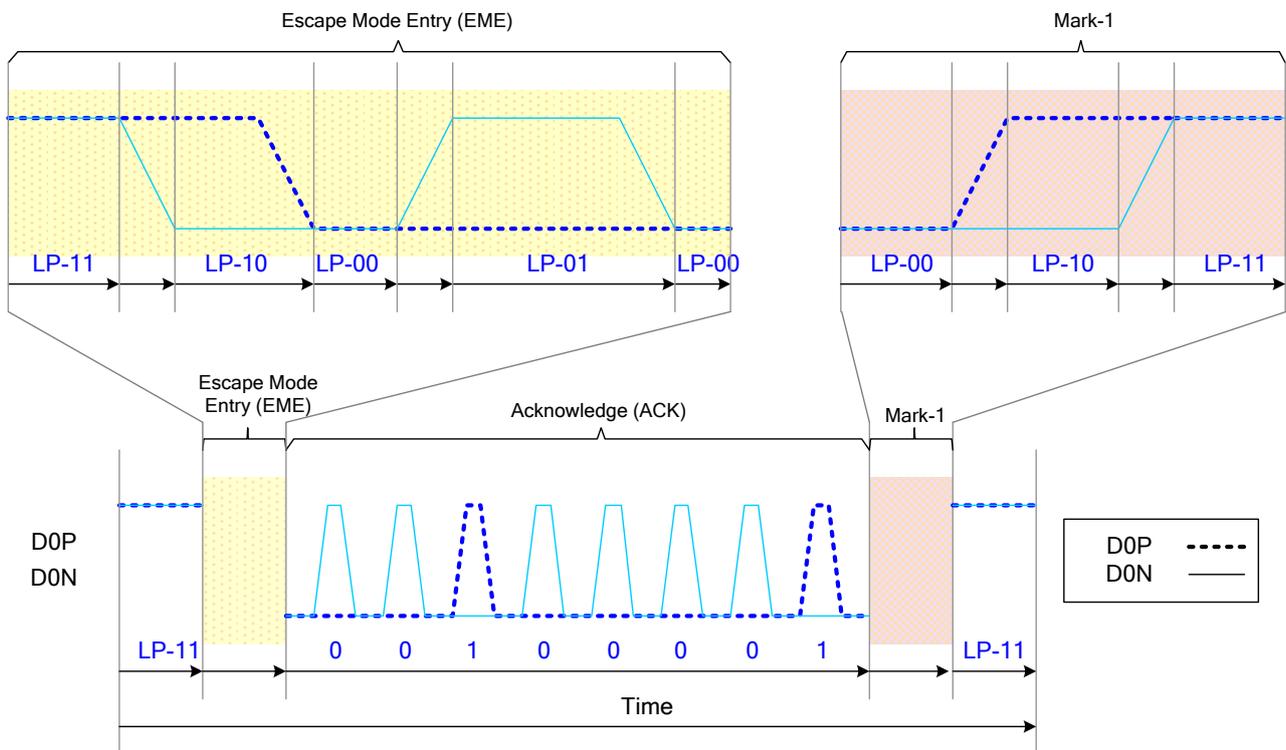


Figure 17: Acknowledge (ACK)

4.1.2.3.3. High-Speed Data Transmission (HSDT)

4.1.2.3.3.1. Entering High-Speed Data Transmission (TSOT of HSDT)

The display module enters High-Speed Data Transmission (HSDT) when Clock lane CLKP/N have already entered the High-Speed Clock Mode (HSCM) by the MCU. See more information in the section “4.1.2.2.3 High-Speed Clock Mode (HSCM)”.

Data lanes D3P/N, D2P/N, D1P/N and D0P/N of the display module enter the High-Speed Data Transmission (TSOT of HSDT) as follows:

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

The sequence of entering High-Speed Data Transmission (TSOT of HSDT) is illustrated below:

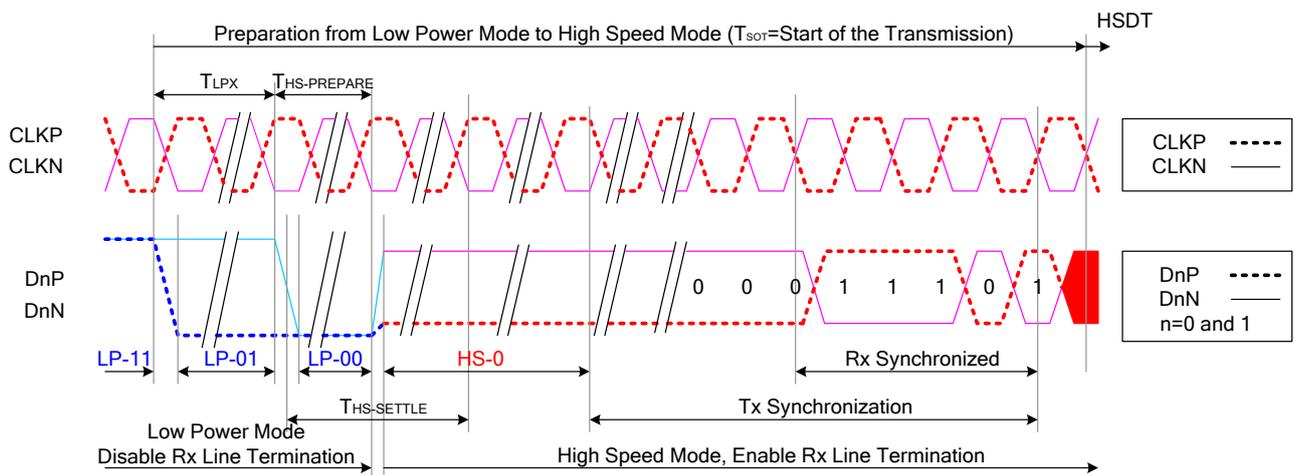


Figure 18: Entering High-Speed Data Transmission (TSOT of HSDT)

4.1.2.3.3.2. Leaving High-Speed Data Transmission (TEOT of HSDT)

The display module leaves the High-Speed Data Transmission (TEOT of HSDT) when Clock lane DSICLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU, and this HSCM is kept until data lanes D3P/N, D2P/N, D1P/N and D0P/N are in the LP-11 mode. See more information in the section “4.1.2.2.3 High-Speed Clock Mode (HSCM)”. Data lanes D3P/N, D2P/N, D1P/N and D0P/N of the display module leave the High-Speed Data Transmission (TEOT of HSDT) as follows:

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
 - ✧ MCU changes to HS-1, if the last load bit is HS-0
 - ✧ MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

The sequence of leaving High-Speed Data Transmission (TEOT of HSDT) is illustrated below:

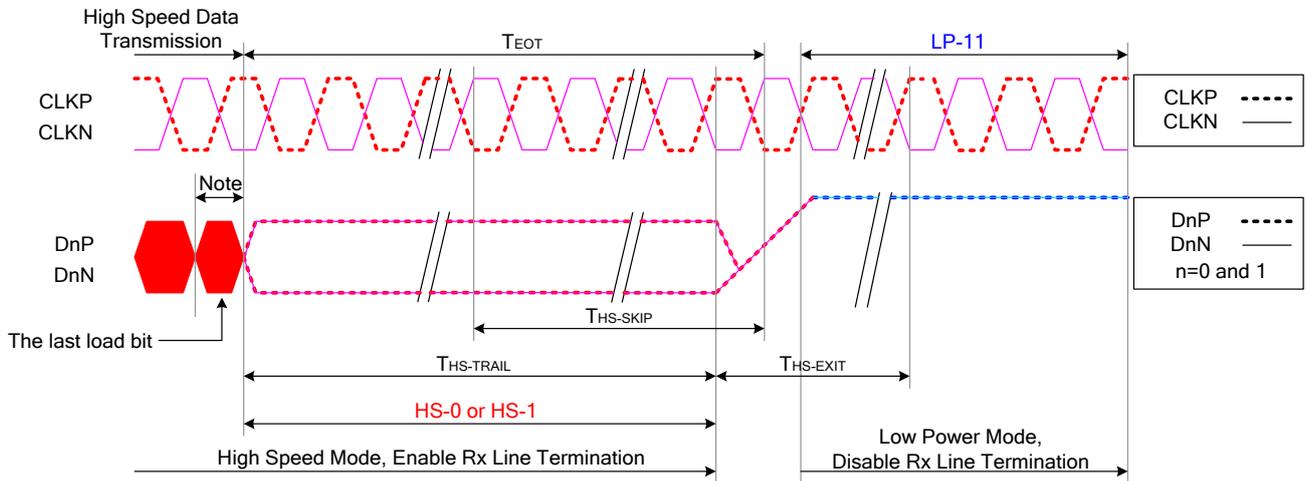


Figure 19: Leaving High-Speed Data Transmission (TEOT of HSDT)

Notes:

1. If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.
2. If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.

4.1.2.3.3.3. Burst of the High-Speed Data Transmission (HSDT)

The burst of the “High-Speed Data Transmission” (HSDT) can consist of one or several data packet(s). These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined in the section “4.1.3.1 Short Packet (SPa) and Long Packet (LPa) Structures”. These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

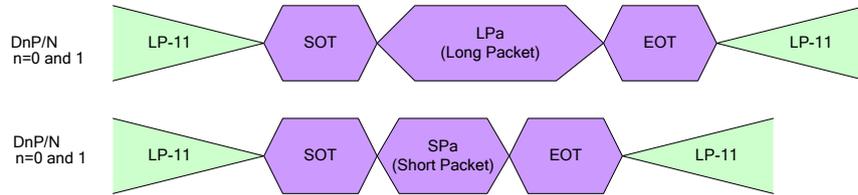


Figure 20: Single Packet in High-Speed Data Transmissions

The multiple packets in High-Speed Data Transmission are illustrated for reference purposes below:

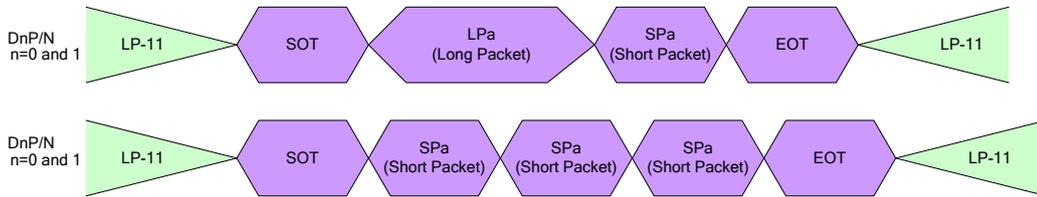


Figure 21: Multiple Packets in High-Speed Data Transmission – Examples

Table 6: Abbreviations

Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Both of Data lanes are ‘1’s (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

Byte orders of the sent packet in High-Speed Data Transmission (HSDT) are as follows.

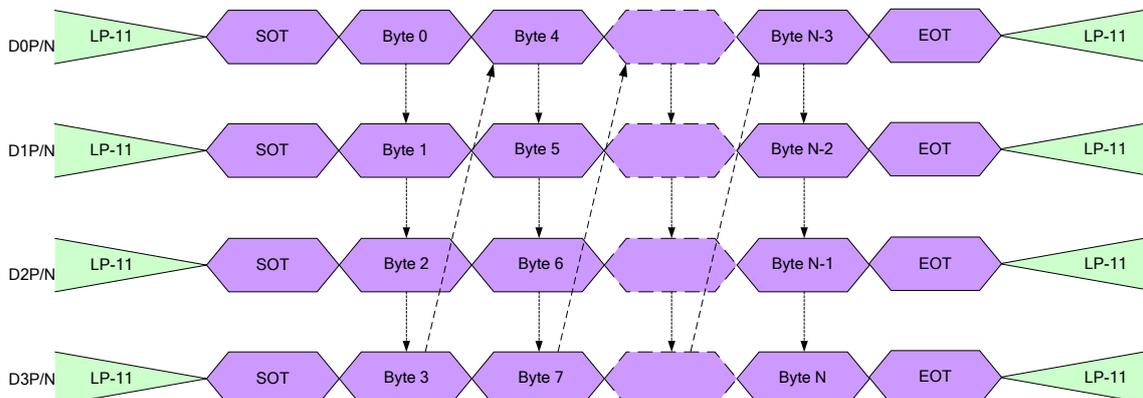


Figure 22: Number of Bytes, N, transmitted is an integer multiple of the number of lanes

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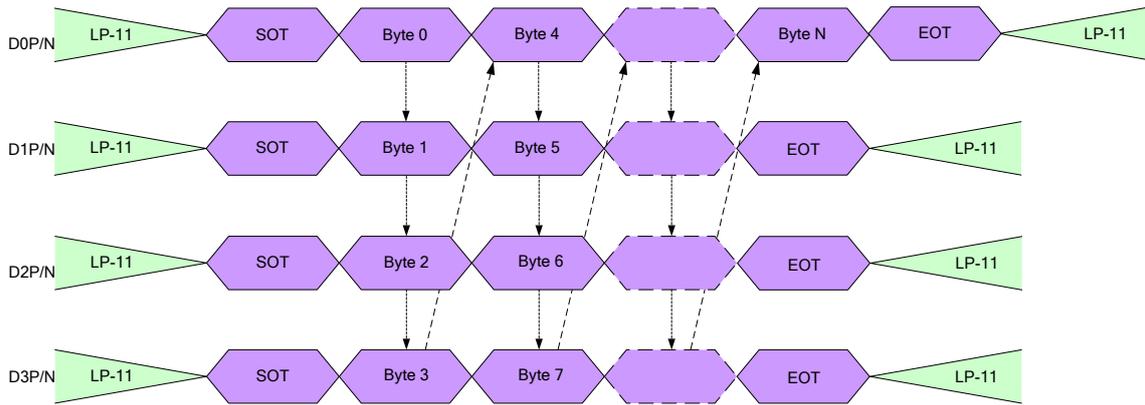


Figure 23: Number of Bytes, N, transmitted is NOT an integer multiple of the number of lanes (Example 1)

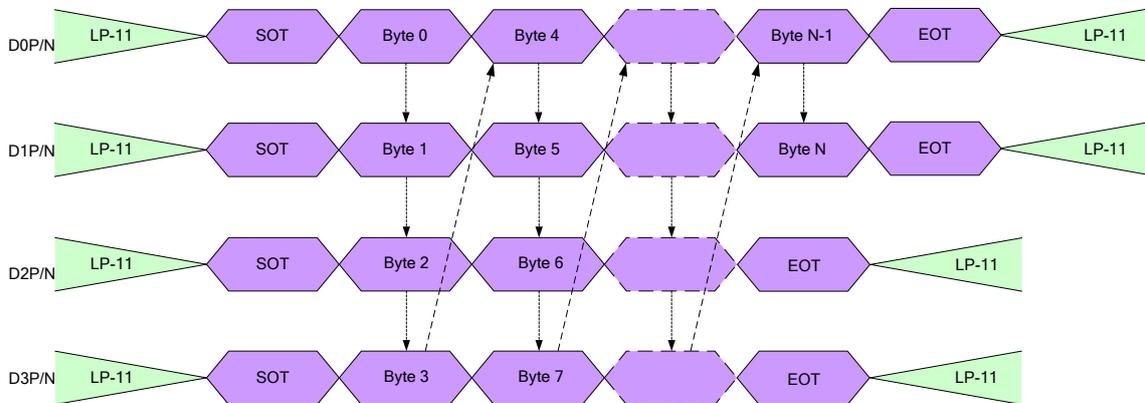


Figure 24: Number of Bytes, N, transmitted is NOT an integer multiple of the number of lanes (Example 2)

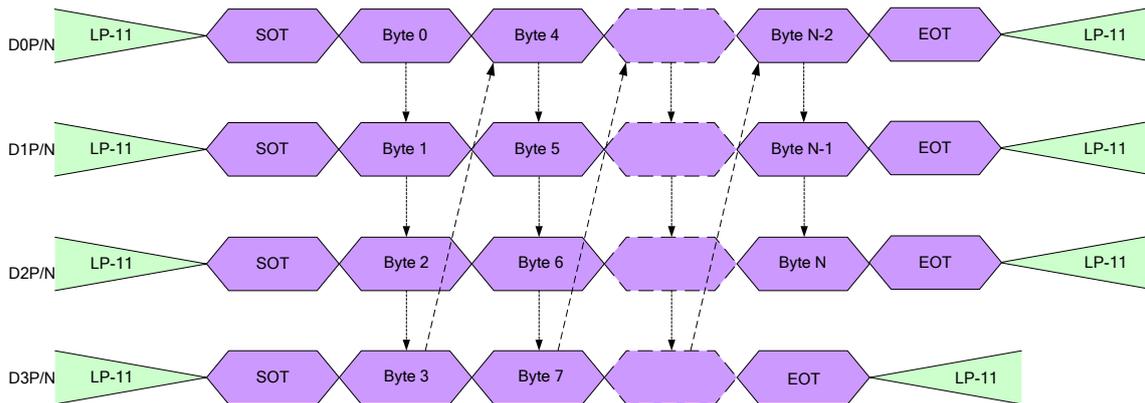


Figure 25: Number of Bytes, N, transmitted is NOT an integer multiple of the number of lanes (Example 3)

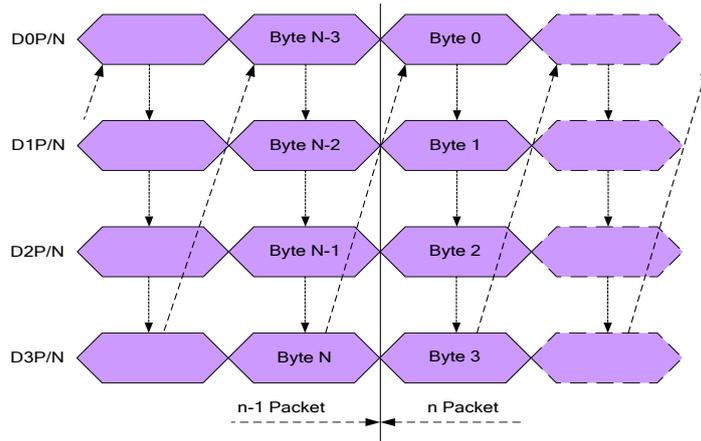


Figure 26: Continuous Multiple Packets in HSDT when Number of Bytes is Equal on Data Lanes at the End of the Packet

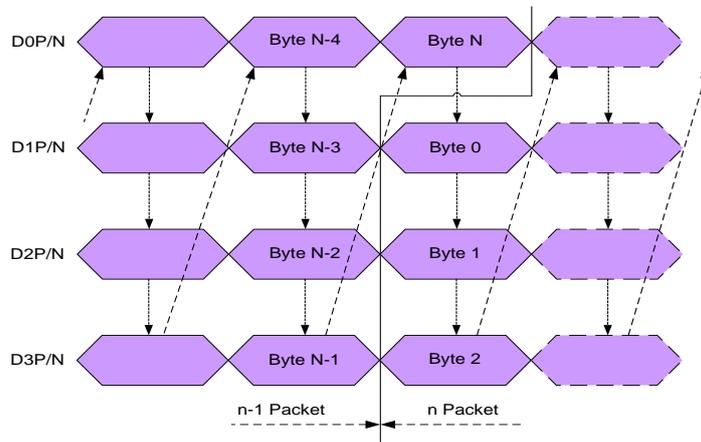


Figure 27: Continuous Multiple Packets in HSDT when Number of Bytes is not Equal on Data Lanes at the End of the Packet (Example 1)

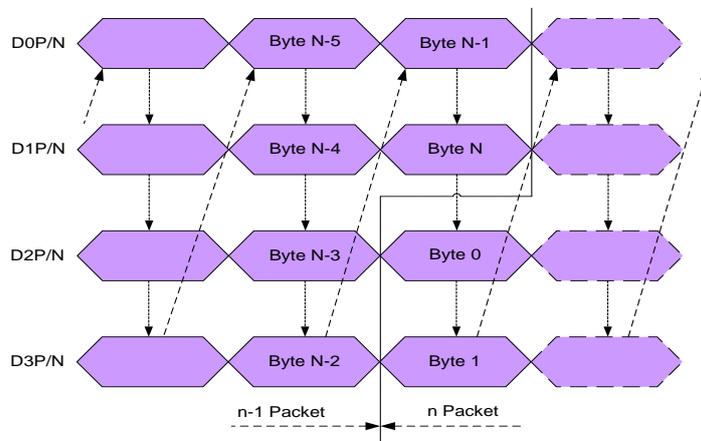


Figure 28: Continuous Multiple Packets in HSDT when Number of Bytes is not Equal on Data Lanes at the End of the Packet (Example 2)

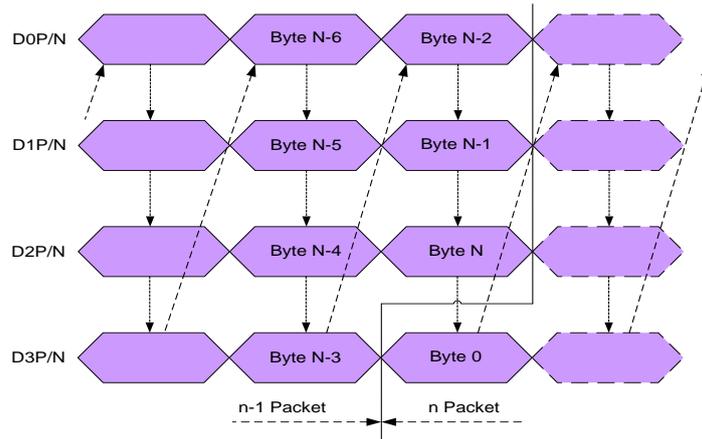


Figure 29: Continuous Multiple Packets in HSDT when Number of Bytes is not Equal on Data Lanes at the End of the Packet (Example 3)

4.1.2.3.4. Bus Turnaround (BTA)

The MCU or display module, which controls D0P/N Data Lanes, can start a bus turnaround procedure when it requires information from a receiver, which can be the MCU or display module.

The MCU and display module use the same sequence when this bus turnaround procedure is used. The sequence, when the MCU wants to do the bus turnaround procedure to the display module, is described for reference purposes as follows:

- Start (MCU): LP-11
- Turnaround Request (MCU): LP-11 => LP-10 => LP-00 => LP-10 => LP-00
- The MCU waits until the display module starts to control D0P/N data lanes and the MCU stops to control D0P/N data lanes (= High-Z)
- The display module changes to the stop mode: LP-00 => LP-10 => LP-11

The bus turnaround procedure (from the MCU to the display module) is illustrated below:

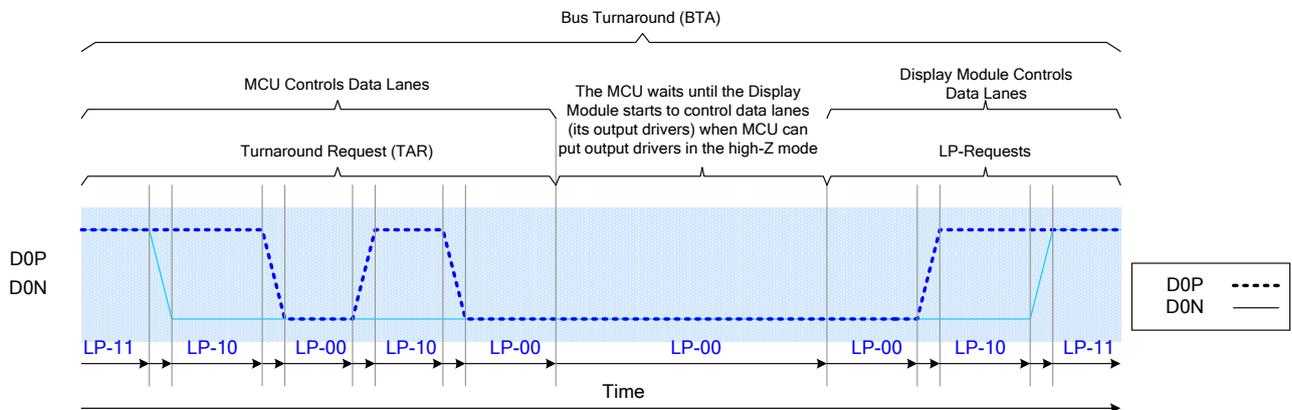


Figure 30: Bus Turnaround Procedure

MCU and display module terms can be switched in Figure 30 if the Bus Turnaround (BTA) is from the display module to the MCU.

4.1.3. Packet Level Communication

4.1.3.1. Short Packet (SPa) and Long Packet (LPa) Structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes. The lengths of the packets are:

- ❖ Short Packet (SPa): 4 bytes
- ❖ Long Packet (LPa): 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

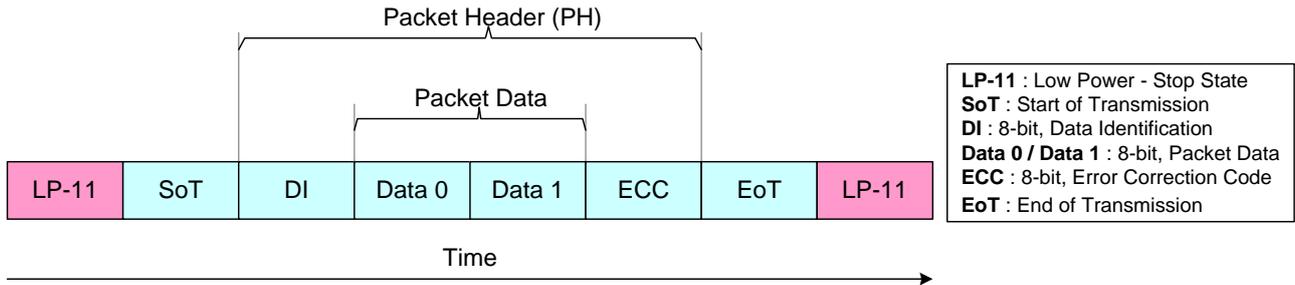


Figure 31: Short Packet (SPa) Structure

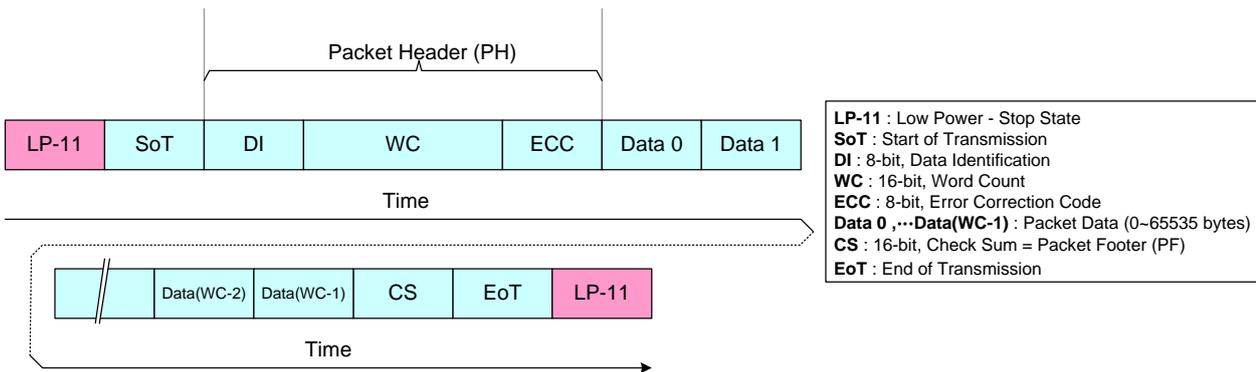


Figure 32: Long Packet (LPa) Structure

Notes:

1. Figure 31 and Figure 32 present a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).
2. The other possibility is that SoT, EoT and LP-11 are not needed between packets if packets are sent in multiple packet format, e.g.
 - LP-11 => SoT => SPa => LPa => SPa => SPa => EoT => LP-11
 - LP-11 => SoT => SPa => SPa => SPa => EoT => LP-11
 - LP-11 => SoT => LPa => LPa => LPa => EoT => LP-11

4.1.3.1.1. Bit Order of the Byte on Packets

The bit order of the byte, what is used in packets, is that the Least Significant Bit (LSB) of the byte is sent first, and the Most Significant Bit (MSB) is sent last. The order is illustrated for reference purposes below.

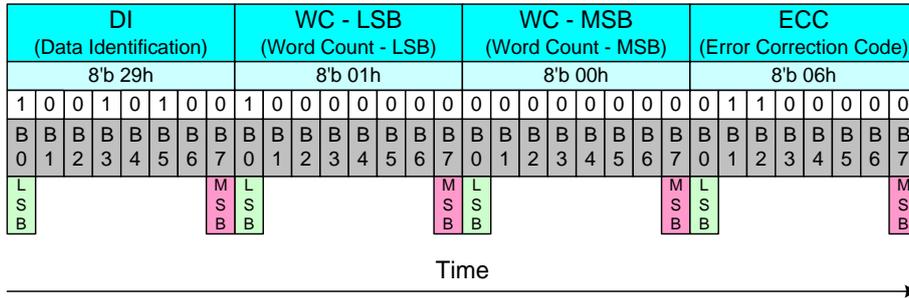


Figure 33: Bit Order of the Byte on Packets

4.1.3.1.2. Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used in packets, is that the Least Significant (LS) Byte of the information is sent first and the Most Significant (MS) Byte is sent last. For example, Word Count (WC) consists of 2 bytes (= 16 bits); while the LS byte is sent first and the MS byte is sent last. The order is illustrated for reference purposes below.

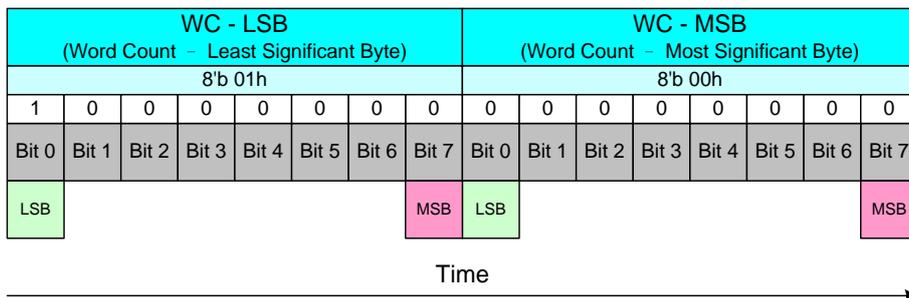


Figure 34: Byte Order of the Multiple Byte Information on Packets

4.1.3.1.3. Packet Header (PH)

The packet header always consists of 4 bytes. The content of these 4 bytes are different for Short Packet (SPa) and Long Packet (LPa).

Short Packet (SPa):

- 1st byte: Data Identification (DI) => Identify that this is a Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)

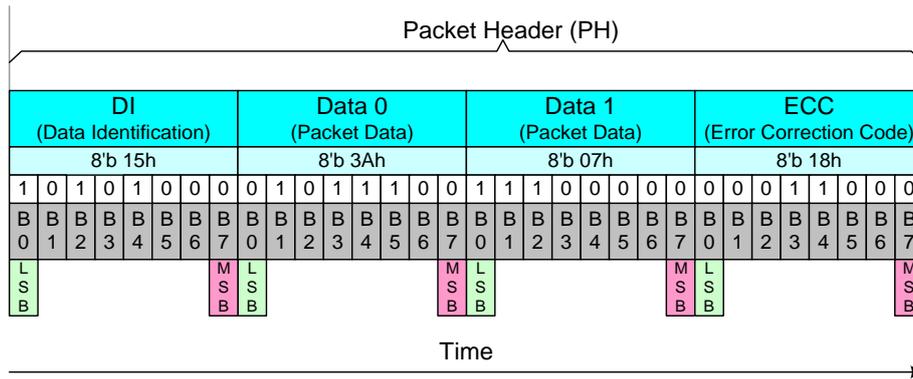


Figure 35: Packet Header (PH) in a Short Packet (SPa)

Long Packet (LPa):

- 1st byte: Data Identification (DI) => Identify that this is a Long Packet (LPa)
- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)

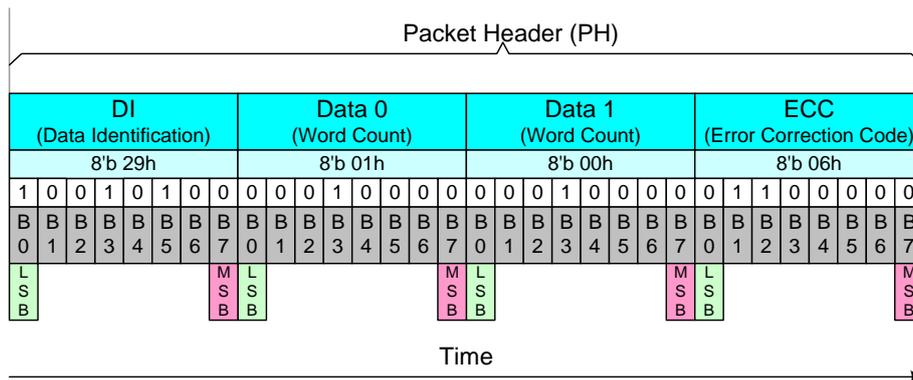


Figure 36: Packet Header (PH) in a Long Packet (LPa)

4.1.3.1.3.1. Data Identification (DI)

Data Identification (DI) is a part of the Packet Header (PH), and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI [7...6]
- Data Type (DT), 6 bits, DI [5...0]

The Data Identification (DI) structure is illustrated, see the figure below.

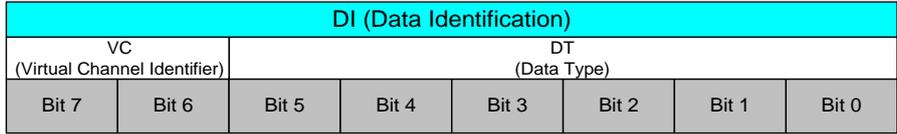


Figure 37: Data Identification (DI) Structure

Data Identification (DI) in the Packet Header (PH) is illustrated for reference purposes below.

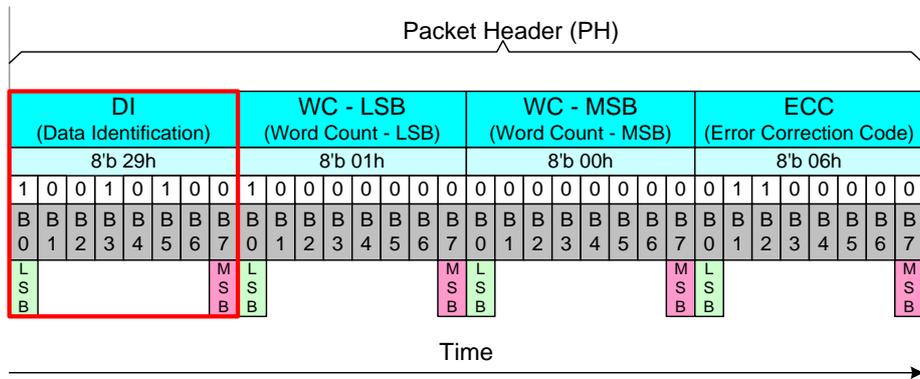


Figure 38: Data Identification (DI) on the Packet Header (PH)

4.1.3.1.3.1.1. Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI [7...6]) structure, and it is used to address where a packet is to be sent from the MCU. Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

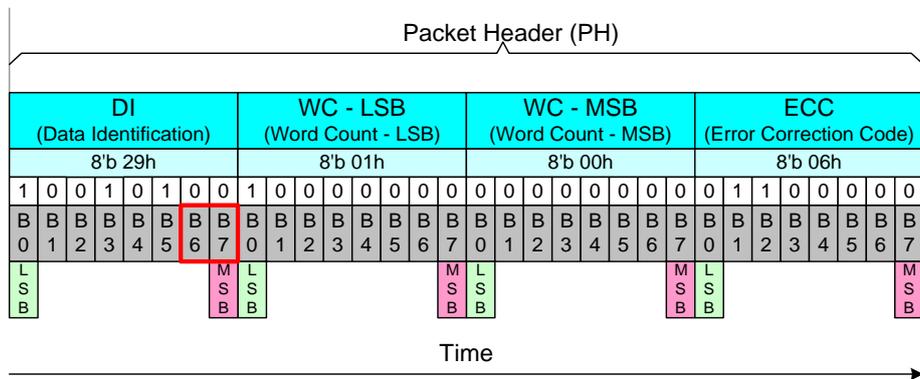


Figure 39: Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can assign 4 different channels for 4 different display modules. Devices will use the same virtual channel as which the MCU uses to send packets to them, e.g.

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Table 7: Data Type (DT) from the MCU to the Display Module

From the MCU to the Display Module								
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex	Description	Short/Long Packet
0	0	0	0	0	1	01	Sync Event, V Sync Start	SPa (Short Packet)
0	1	0	0	0	1	11	Sync Event, V Sync End	SPa (Short Packet)
1	0	0	0	0	1	21	Sync Event, H Sync Start	SPa (Short Packet)
1	1	0	0	0	1	31	Sync Event, H Sync End	SPa (Short Packet)
0	0	1	0	0	0	08	End of Transmission Packet (EoTP) ^{Note1}	SPa (Short Packet)
0	0	0	0	1	0	02	Color Mode Off Command	SPa (Short Packet)
0	1	0	0	1	0	12	Color Mode On Command	SPa (Short Packet)
1	0	0	0	1	0	22	Shut Down Peripheral Command	SPa (Short Packet)
1	1	0	0	1	0	32	Turn On Peripheral Command	SPa (Short Packet)
0	0	0	0	1	1	03	Generic Short WRITE, no parameters	SPa (Short Packet)
0	1	0	0	1	1	13	Generic Short WRITE, 1 parameters	SPa (Short Packet)
1	0	0	0	1	1	23	Generic Short WRITE, 2 parameters	SPa (Short Packet)
0	0	0	1	0	0	04	Generic Short READ, no parameters	SPa (Short Packet)
0	1	0	1	0	0	14	Generic Short READ, 1 parameters	SPa (Short Packet)
1	0	0	1	0	0	24	Generic Short READ, 2 parameters	SPa (Short Packet)
0	0	0	1	0	1	05	DCS Write, No Parameter	SPa (Short Packet)
0	1	0	1	0	1	15	DCS Write, 1 Parameter	SPa (Short Packet)
0	0	0	1	1	0	06	DCS Read, No Parameter	SPa (Short Packet)
1	1	0	1	1	1	37	Set Maximum Return Packet Size	SPa (Short Packet)
0	0	1	0	0	1	09	Null Packet, No Data, ^{Note2}	LPa (Long Packet)
0	1	1	0	0	1	19	Blanking Packet, no data	LPa (Long Packet)
1	0	1	0	0	1	29	Generic Long Write	LPa (Long Packet)
1	1	1	0	0	1	39	DCS Write Long	LPa (Long Packet)
0	0	1	1	1	0	0E	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	LPa (Long Packet)
0	1	1	1	1	0	1E	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	LPa (Long Packet)
1	0	1	1	1	0	2E	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	LPa (Long Packet)
1	1	1	1	1	0	3E	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	LPa (Long Packet)
x	x	0	0	0	0	x0	DO NOT USE	
x	x	1	1	1	1	xF	All unspecified codes are reserved	

Notes:

1. This can be used when the MCU wants to make sure that it is the end of the transmission in High Speed Data Transferring (HSDDT) mode.
2. This can be used when data lanes are to be kept in High Speed Data Transferring (HSDDT) Mode.

Table 8: Data Type (DT) from the Display Module to the MCU

From the Display Module to the MCU							Description	Short/Long Packet
Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex		
0	0	0	0	1	0	02	Acknowledge with Error Report	SPa (Short Packet)
0	0	1	0	0	0	08	End of Transmission Packet (EoTP)	SPa (Short Packet)
0	1	0	0	0	1	11	Generic Short READ Response, 1 byte returned	SPa (Short Packet)
0	1	0	0	1	0	12	Generic Short READ Response, 2 byte returned	SPa (Short Packet)
0	1	1	0	1	0	1A	Generic Long READ Response	LPa (Long Packet)
0	1	1	1	0	0	1C	DCS Read Long Response	LPa (Long Packet)
1	0	0	0	0	1	21	DCS Read Short Response, 1 byte returned	SPa (Short Packet)
1	0	0	0	1	0	22	DCS Read Short Response, 2 byte returned	SPa (Short Packet)

The receiver will ignore other Data Types (DT) if they are not defined in Table 7 and Table 8.

4.1.3.1.3.2. Packet Data (PD) in a Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is placed after Data Type (DT) of the Data Identification (DI) and indicates a Short Packet (SPa) is to be sent. Packet Data (PD) of a Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1. The sending order of the Packet Data (PD) is that Data 0 is sent first and the Data 1 is sent last. Bits of Data 1 are set to 0 if the information length is 1 byte. Packet Data (PD) of a Short Packet (SPa), when the length of the information is 1 or 2 bytes and Virtual Channel (VC) is 0, are illustrated for reference purposes below.

Packet Data (PD) information:

- Data 0: 26hex (Display Command Set (DCS) with 1 Parameter => DI (Data Type (DT)) = 15hex)
- Data 1: 01hex (DCS's parameter)

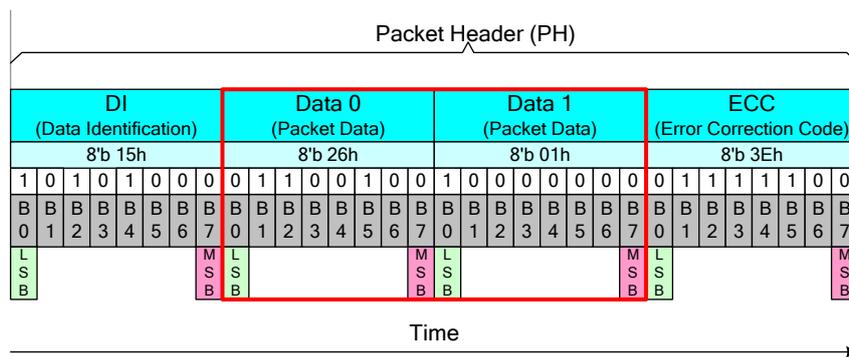


Figure 42: Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

- Data 0: 10hex (DCS without parameter => DI (Data Type (DT)) = 05hex)
- Data 1: 00hex (Null)

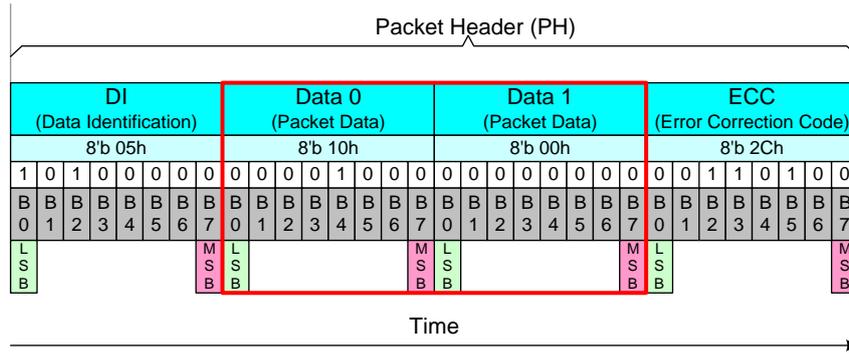


Figure 43: Packet Data (PD) for Short Packet (SPa), 1 Byte Information

4.1.3.1.3.3. Word Count (WC) in a Long Packet (LPa)

Word Count (WC) of the Long Packet (LPa) is placed after Data Type (DT) of the Data Identification (DI) and indicates that a Long Packet (LPa) is to be sent. Word Count (WC) indicates the amount of data bytes of the Packet Data (PD) that is to be sent after the Packet Header (PH). The location of the Word Count (WC) in a Long Packet is the same as which of the Packet Data (PD) in a Short Packet (SPa), as shown in Figure 45. Word Count (WC) of the Long Packet (LPa) consists of 2 bytes. The sending order of these 2 bytes of the Word Count (WC) is that the Least Significant (LS) Byte is sent first, and the Most Significant (MS) Byte is sent last. Word Count (WC) of a Long Packet (LPa) is illustrated for reference purposes below.

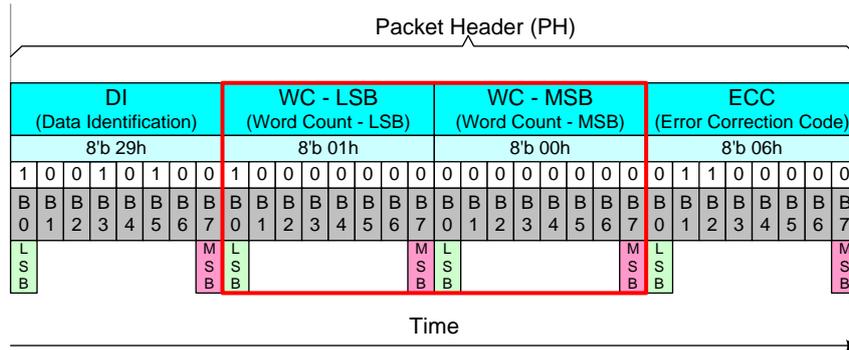


Figure 44: Word Count (WC) in a Long Packet (LPa)

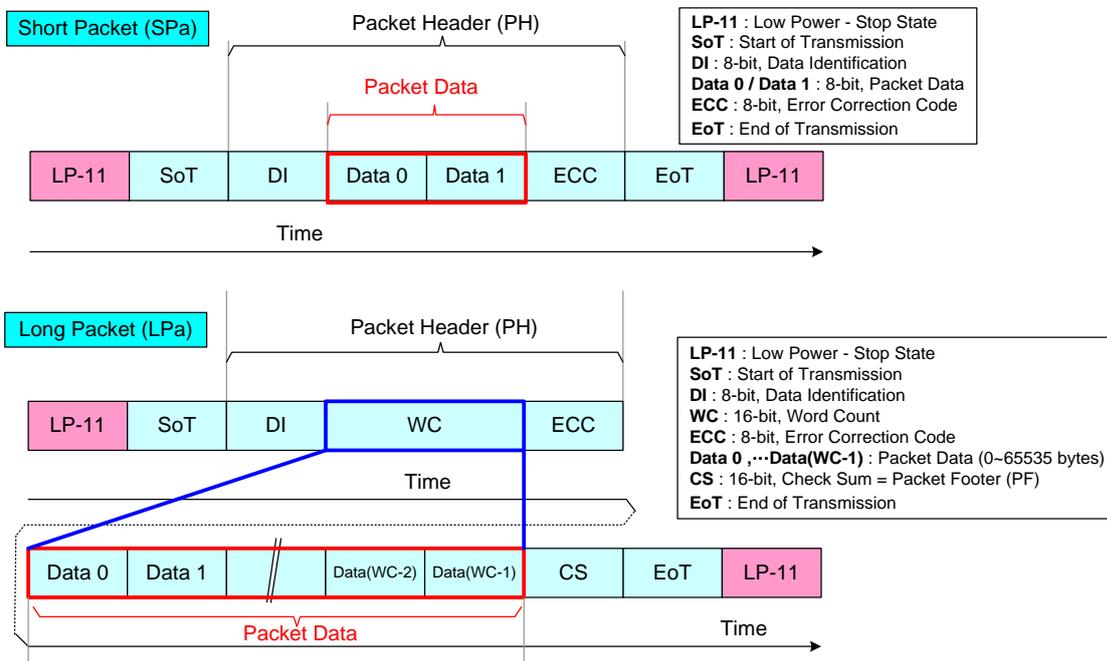


Figure 45: Packet Data in Short and Long Packets

4.1.3.1.3.4. Error Correction Code (ECC)

The Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors. The ECC protects the following fields:

- ❖ Short Packet (SPa): Data Identification (DI) byte (8 bits: D [0...7]), Packet Data (PD) bytes (16 bits: D [8...23]) and ECC (8 bits: P [0...7])
- ❖ Long Packet (LPa): Data Identification (DI) byte (8 bits: D [0...7]), Word Count (WC) bytes (16 bits: D [8...23]) and ECC (8 bits: P [0...7])

D [23...0] and P [7...0] are illustrated for reference purposes below.

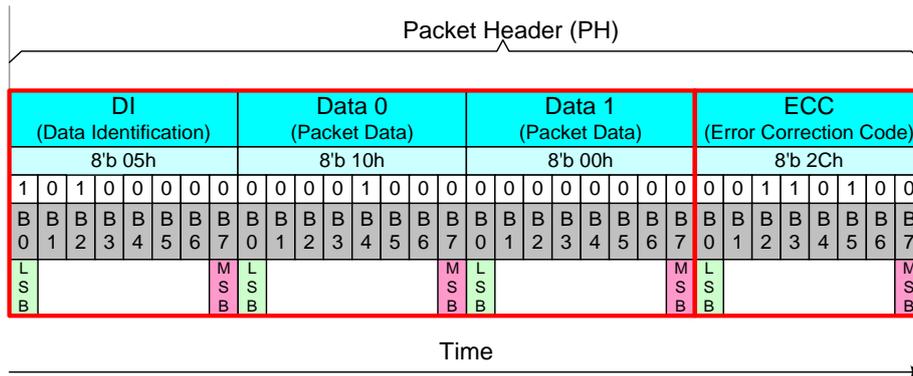


Figure 46: D [23...0] and P [7...0] in a Short Packet (SPa)

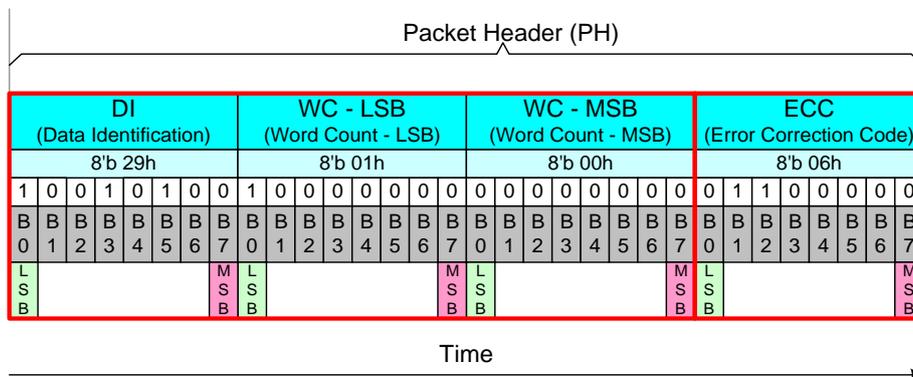


Figure 47: D [23...0] and P [7...0] in a Long Packet (LPa)

Error Correction Code (ECC) can recognize one or several error(s) and can only correct one-bit error. Bits (P [7...0]) of the Error Correction Code (ECC) are defined, where the symbol '^' presents the XOR function (Pn is 1 if there is odd number of 1, and Pn is 0 if there is even number of 1), as follows.

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

- $P1 = D0 \oplus D1 \oplus D3 \oplus D4 \oplus D6 \oplus D8 \oplus D10 \oplus D12 \oplus D14 \oplus D17 \oplus D20 \oplus D21 \oplus D22 \oplus D23$
- $P0 = D0 \oplus D1 \oplus D2 \oplus D4 \oplus D5 \oplus D7 \oplus D10 \oplus D11 \oplus D13 \oplus D16 \oplus D20 \oplus D21 \oplus D22 \oplus D23$

P7 and P6 are set to 0 because Error Correction Code (ECC) is based on 64 bit value (D [63...0]), but this implementation is based on 24 bit value (D [23...0]). Therefore, only 6 bits are needed (P [5...0]) for Error Correction Code (ECC).

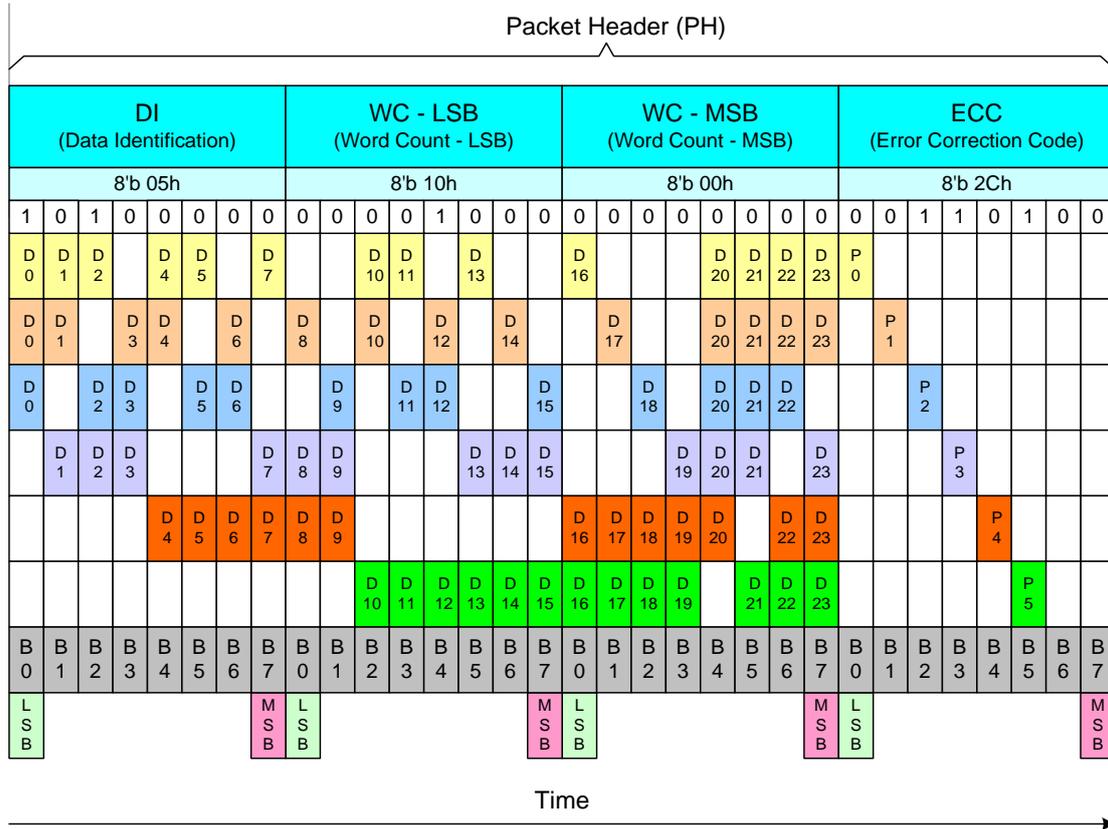


Figure 48: XOR Function on a Short Packet (SPa)

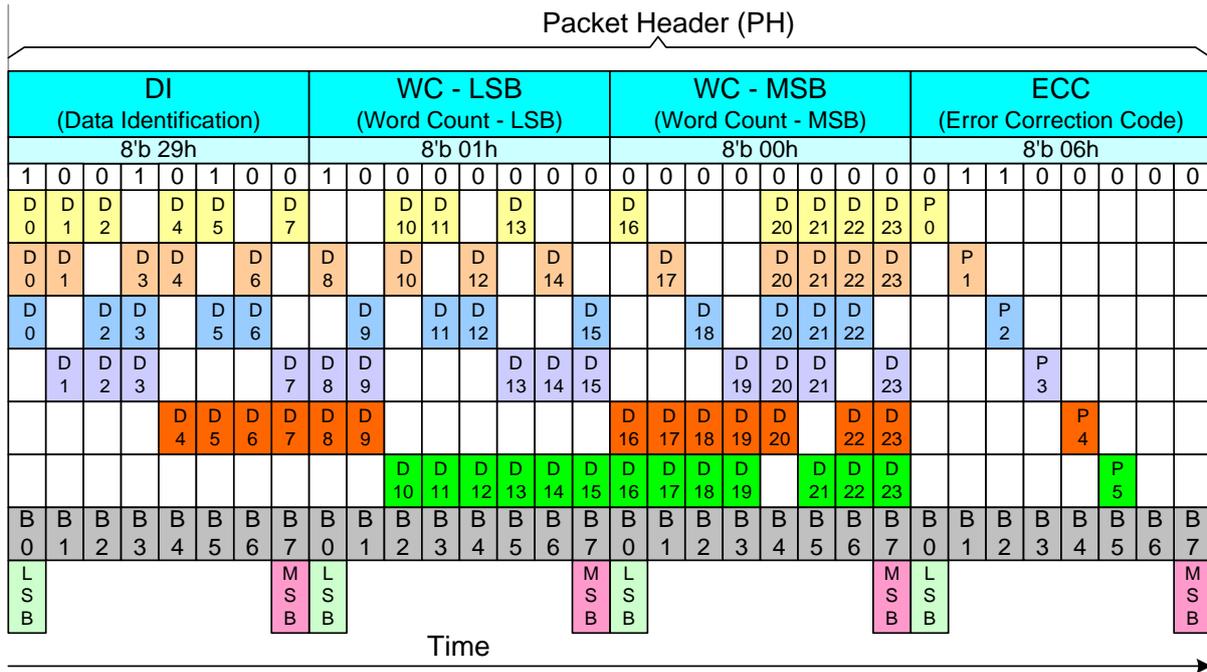


Figure 49: XOR Function on a Long Packet (LPa)

The transmitter (= the MCU or the Display Module) will send data bits D [23...0] and Error Correction Code (ECC) P [7...0]. The receiver (= the Display module or the MCU) will calculate the Internal Error Correction Code (IECC) and compare the received Error Correction Code (ECC) and the Internal Error Correction Code (IECC). This comparison is done when each power bit of ECC and IECC have performed the XOR function. The result of this function is PO [7...0]. This functionality, where the transmitter is the MCU and the receiver is the display module, is illustrated for reference purposes below.

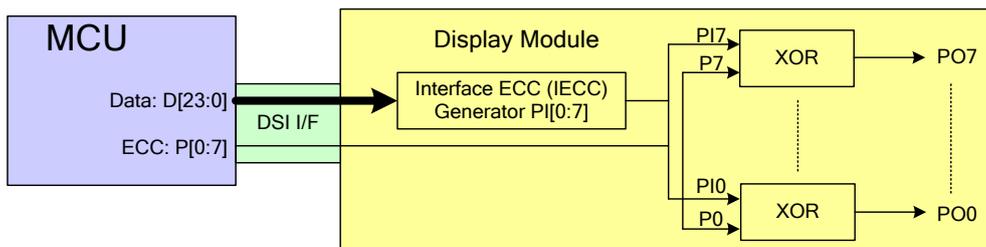


Figure 50: Internal Error Correction Code (IECC) on the Display Module (= the Receiver)

The sent data bits (D [23...0]) and ECC (P [7...0]) are correctly received if the value of the PO [7...0] is 00h. The sent data bits (D [23...0]) and ECC (P [7...0]) are not correctly received if the value of the PO [7...0] is not 00h.

ECC P[7...0]	1	1	0	0	0	0	0	0	03h
IECC PI[7...0]	1	1	0	0	0	0	0	0	03h
XOR(ECC, IECC) => PO[7...0]	0	0	0	0	0	0	0	0	= 00h => No Error
	L							M	
	S							S	
	B							B	

Figure 51: Internal XOR Calculation between ECC and IECC Values – No Error

ECC P[7...0]	1	1	0	0	0	0	0	0	03h
IECC PI[7...0]	1	1	1	1	0	0	0	0	0Fh
XOR(ECC, IECC) => PO[7...0]	0	0	1	1	0	0	0	0	= 0Ch => Error
	L							M	
	S							S	
	B							B	

Figure 52: Internal XOR Calculation between ECC and IECC Values - Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) function is not used for data values D [23...0] on the transmitter side. The number of the errors (one or more) can be defined when the value of the PO [7...0] is compared to the values in the following table.

Table 9: One Bit Error Value of the Error Correction Code (ECC)

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D [0]	0	0	0	0	0	1	1	1	07h
D [1]	0	0	0	0	1	0	1	1	0Bh
D [2]	0	0	0	0	1	1	0	1	0Dh
D [3]	0	0	0	0	1	1	1	0	0Eh
D [4]	0	0	0	1	0	0	1	1	13h
D [5]	0	0	0	1	0	1	0	1	15h
D [6]	0	0	0	1	0	1	1	0	16h
D [7]	0	0	0	1	1	0	0	1	19h
D [8]	0	0	0	1	1	0	1	0	1Ah
D [9]	0	0	0	1	1	1	0	0	1Ch
D [10]	0	0	1	0	0	0	1	1	23h
D [11]	0	0	1	0	0	1	0	1	25h
D [12]	0	0	1	0	0	1	1	0	26h
D [13]	0	0	1	0	1	0	0	1	29h
D [14]	0	0	1	0	1	0	1	0	2Ah
D [15]	0	0	1	0	1	1	0	0	2Ch
D [16]	0	0	1	1	0	0	0	1	31h
D [17]	0	0	1	1	0	0	1	0	32h
D [18]	0	0	1	1	0	1	0	0	34h
D [19]	0	0	1	1	1	0	0	0	38h
D [20]	0	0	0	1	1	1	1	1	1Fh
D [21]	0	0	1	0	1	1	1	1	2Fh
D [22]	0	0	1	1	0	1	1	1	37h
D [23]	0	0	1	1	1	0	1	1	3Bh

An error is detected if the value of the PO [7...0] is in Table 9, and the receiver can correct this one bit error

because this found value also defines the location of the corrupt bit, e.g.

- ❖ PO [7...0] = 0Eh
- ❖ The bit of the data (D [23...0]), that is not correct, is D [3]

More than one error is detected if the value of the PO [7...0] is not in Table 9, for example, PO [7...0] = 0Ch.

4.1.3.1.4. Packet Data (PD) in a Long Packet (LPa)

Packet Data (PD) of a Long Packet (LPa) is placed after the Packet Header (PH) of a Long Packet (LPa). The amount of the data bytes is defined in the section “4.1.3.1.3.3 Word Count (WC) in a Long Packet (LPa)”.

4.1.3.1.5. Packet Footer (PF) in a Long Packet (LPa)

Packet Footer (PF) of a Long Packet (LPa) is placed after the Packet Data (PD) of a Long Packet (LPa). The Packet Footer (PF) is a checksum value that is calculated from the Packet Data of the Long Packet (LPa). The checksum uses a 16-bit Cyclic Redundancy Check (CRC) value which is generated by a polynomial $X^{16}+X^{12}+X^5+X^0$, as illustrated below.

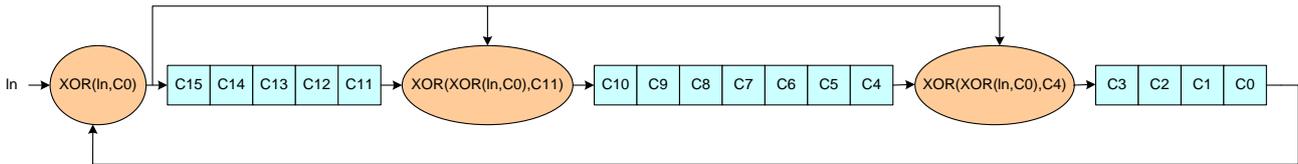


Figure 53: 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit which is inputted into the 16-bit Cyclic Redundancy Check (CRC). An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of a Long Packet (LPa) is 01h, is illustrated (step-by-step) below.

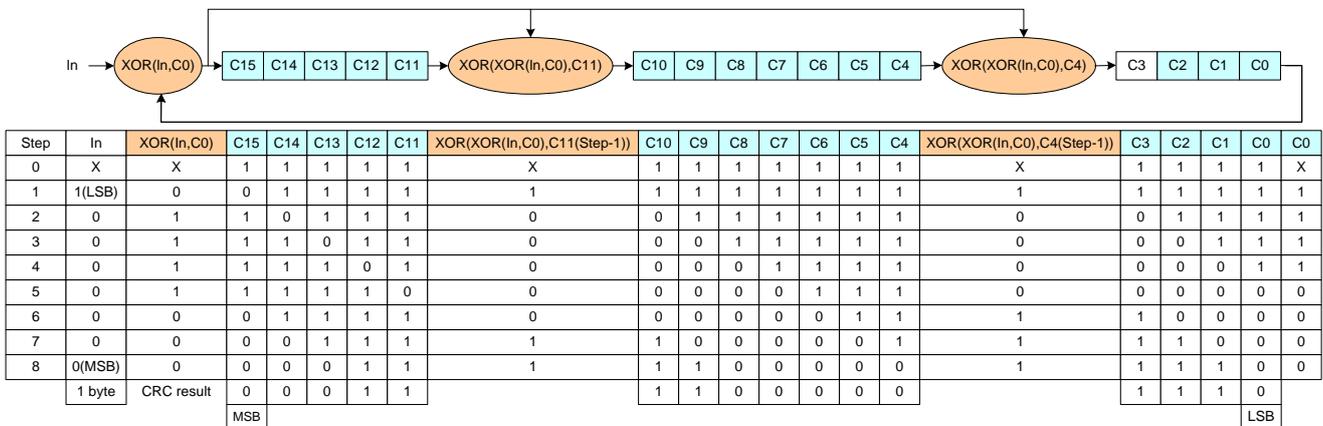


Figure 54: CRC Calculation – Packet Data (PD) is 01h

The value of the Packet Footer (PF) is 1E0Eh in this example (Command 01h has been sent), and is illustrated

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below.

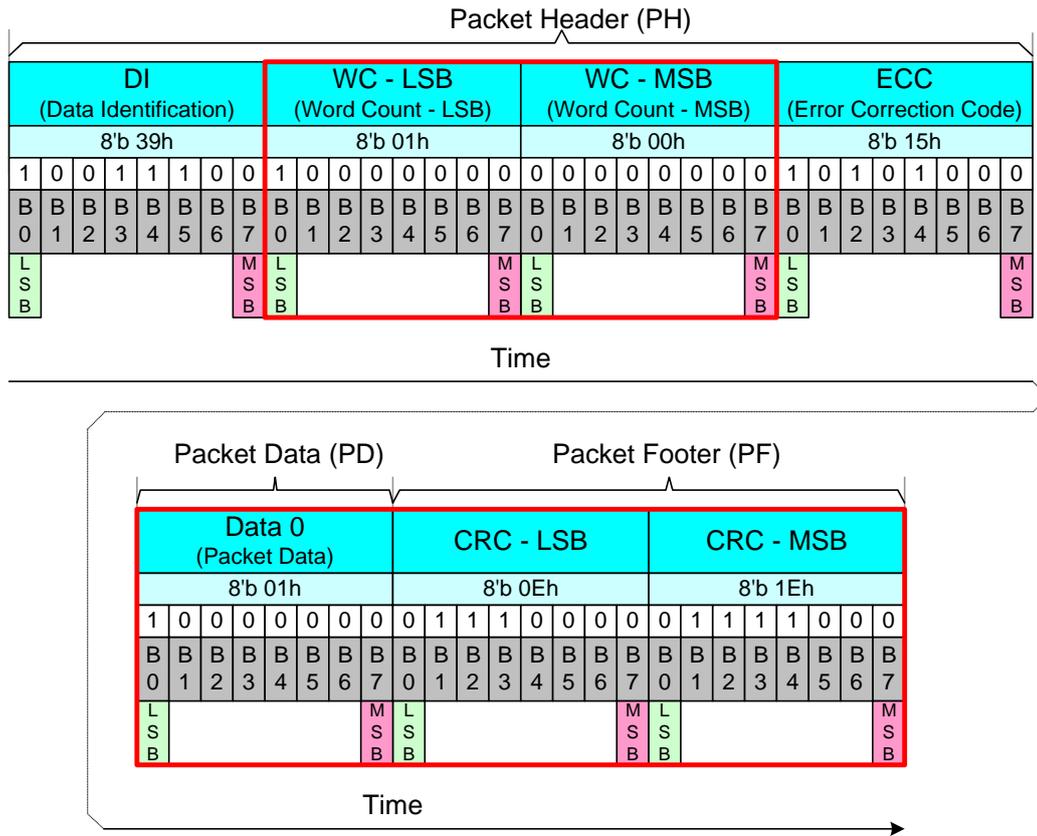


Figure 55: Packet Footer (PF) Example

The receiver calculates its checksum value from the received Packet Data (PD). The receiver compares its checksum and the Packet Footer (PF) that the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the checksum of the receiver and Packet Footer (PF) are equal. The received Packet Data (PD) and Packet Footer (PF) are not correct if the checksum of the receiver and Packet Footer (PF) are not equal.

4.1.3.2. Packet Transmissions

4.1.3.2.1. Packet from the MCU to the Display Module

4.1.3.2.1.1. Display Command Set (DCS)

Display Command Set (DCS), defined in the section “5.3Page 0 Command Description”, is used from the MCU to the display module. This Display Command Set (DCS) is always defined in the Data 0 of the Packet Data (PD), and is included in Short Packet (SPa) and Long packet (LPa), as illustrated below.

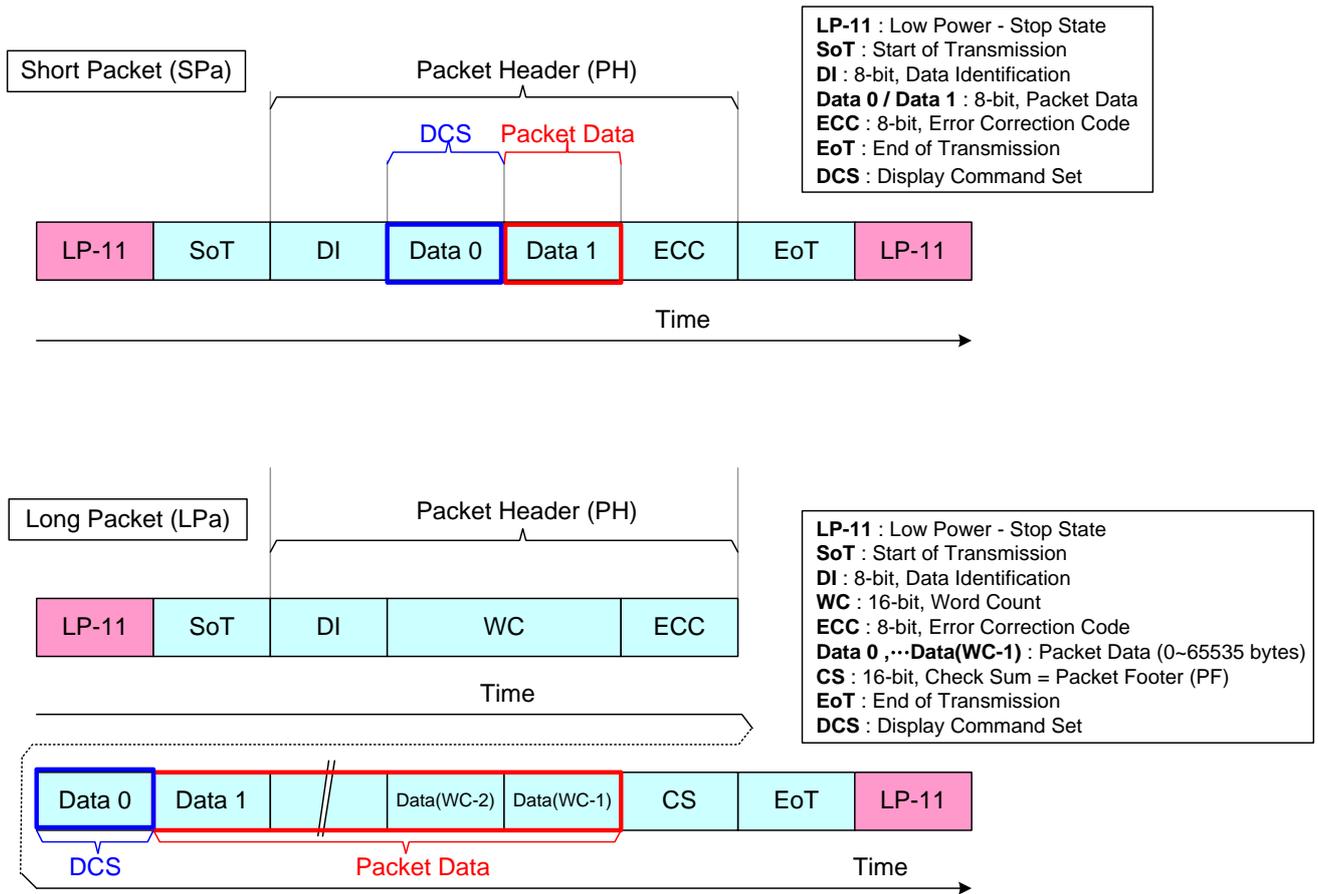


Figure 56: Display Command Set (DCS) in Short Packet (SPa) and Long Packet (LPa)

4.1.3.2.1.2. Display Command Set (DCS) Write, No Parameter (DCSWN-S)

“Display Command Set (DCS) Write, No Parameter”, which is defined in Data Type (DT, 00 0101b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in a table below.

Table 10: Display Command Set (DCS) Write, No Parameters (DCSWN-S)

Command
NOP (00h)
Software Reset (01h)
Sleep In(10h)
Sleep Out (11h)
Normal Display Mode On (13h)
All Pixel Off (22h)
All Pixel On (23h)
Display Off (28h)
Display ON (29h)
Tearing Effect Line OFF (34h)
Idle Mode Off (38h)
Idle Mode On (39h)
Stop Transition (59h)

A Short Packet (SPa) is defined as:

- Data Identification (DI)
 - ✧ Virtual Channel (VC, DI [7...6]): 00b
 - ✧ Data Type (DT, DI [5...0]): 00 0101b
- Packet Data (PD)
 - ✧ Data 0: “Sleep In (10h)”, Display Command Set (DCS)
 - ✧ Data 1: Always 00hex
- Error Correction Code (ECC)

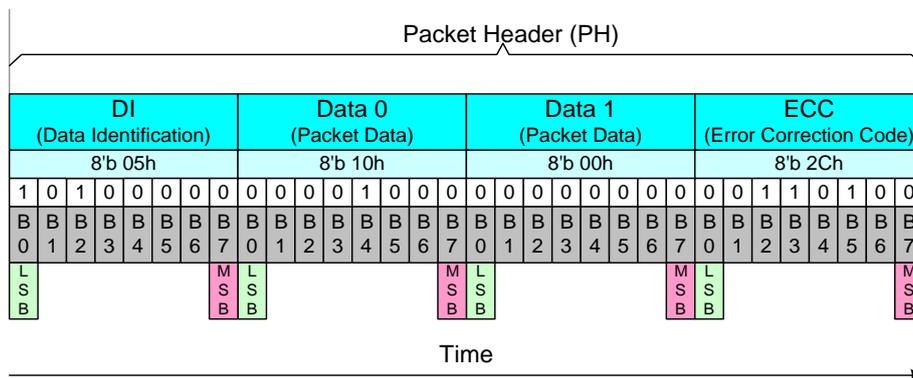


Figure 57: Display Command Set (DCS) Write, No Parameter (DCSWN-S) - Example

4.1.3.2.1.3. Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

“Display Command Set (DCS) Write, 1 Parameter” (DCSW1-S), which is defined in Data Type (DT, 01 0101b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in the table below.

Table 11: Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)

Command
Gamma Curve Set (26h)
Tearing Effect Line ON(35h)
Memory Access Control (36h)
Interface Pixel Format (3Ah)
Write Display Brightness (51h)
Write CTRL Display (53h)
Write Power Save (55h)

Note: One Subpixel has been written

A Short Packet (SPa) is defined as:

- Data Identification (DI)
 - ✧ Virtual Channel (VC, DI [7...6]): 00b
 - ✧ Data Type (DT, DI [5...0]): 01 0101b
- Packet Data (PD)
 - ✧ Data 0: “Gamma Set (26h)”, Display Command Set (DCS)
 - ✧ Data 1: 01hex, Parameter of the DCS
- Error Correction Code (ECC)

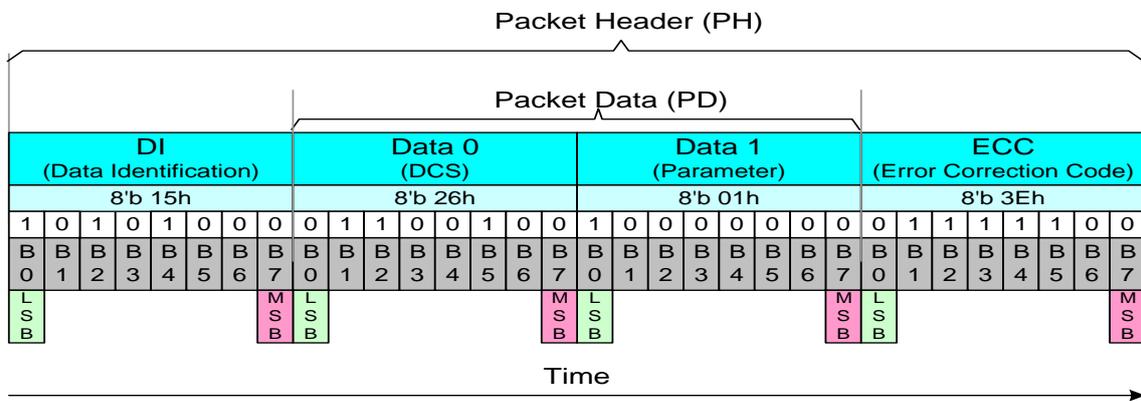


Figure 58: Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) – Example

4.1.3.2.1.4. Display Command Set (DCS) Write Long (DCSW-L)

“Display Command Set (DCS) Write Long” (DCSW-L), which is defined in Data Type (DT, 11 1001b), is always used in a Long Packet (LPa) from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters) are defined in a table below.

Table 12: Display Command Set (DCS) Write Long (DCSW-L)

Command
NOP (00h), ^{Note 1}
Software Reset (01h), ^{Note 1}
Sleep In(10h), ^{Note 1}
Sleep Out (11h), ^{Note 1}
Normal Display Mode On (13h), ^{Note 1}
All Pixel Off (22h), ^{Note 1}
All Pixel On (23h), ^{Note 1}
Gamma Curve Set (26h), ^{Note 2}
Display Off (28h), ^{Note 1}
Display ON (29h), ^{Note 1}
Tearing Effect Line OFF (34h), ^{Note 1}
Tearing Effect Line ON (35h), ^{Note 2}
Memory Access Control (36h), ^{Note 2}
Idle Mode Off (38h), ^{Note 1}
Idle Mode On (39h), ^{Note 1}
Interface Pixel Format (3Ah), ^{Note 2}
Set Tear Scan Line(44h),
Write Display Brightness (51h), ^{Note 2}
Write CTRL Display (53h), ^{Note 2}
Write Power Save(55h), ^{Note 2}
Stop Transition (59h), ^{Note 1}
Write CABC Minimum Brightness (5Eh), ^{Note 2}
Set Transition Time(68h)

Notes:

1. Short Packet (SPa) can also be used; See the section “4.1.3.2.1.2 Display Command Set (DCS) Write, No Parameter (DCSWN-S)”.
2. Short Packet (SPa) can also be used; See the section “4.1.3.2.1.3 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)”.

A Long Packet (LPa) with one command (No Parameter) is defined as:

- Data Identification (DI)
 - ✧ Virtual Channel (VC, DI [7...6]): 00b
 - ✧ Data Type (DT, DI [5...0]): 11 1001b
- Word Count (WC)
 - ✧ Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: “Sleep In (10h)”, Display Command Set (DCS)
- Packet Footer (PF)

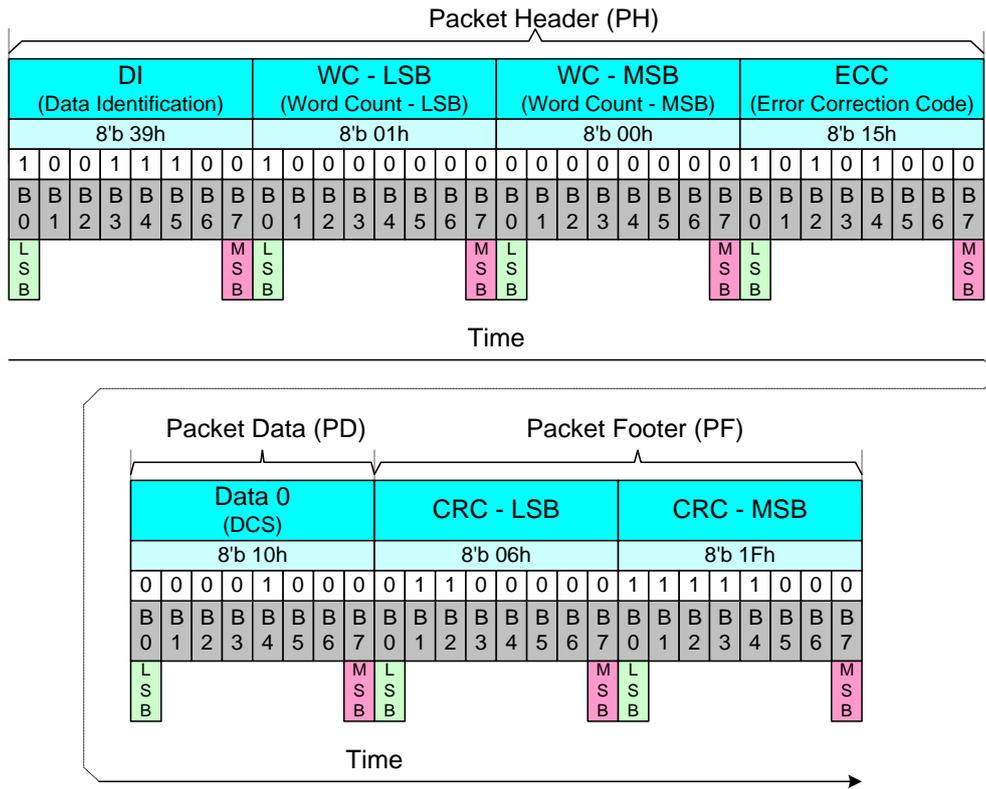


Figure 59: Display Command Set (DCS) Write Long (DCSW-L) with DCS Only - Example

A Long Packet (LPa) with one Write (1 parameter) is defined as:

- Data Identification (DI)
 - ✧ Virtual Channel (VC, DI [7...6]): 00b
 - ✧ Data Type (DT, DI [5...0]): 11 1001b
- Word Count (WC)
 - ✧ Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
 - ✧ Data 0: "Gamma Set (26h)", Display Command Set (DCS)
 - ✧ Data 1: 01hex, Parameter of the DCS
- Packet Footer (PF)

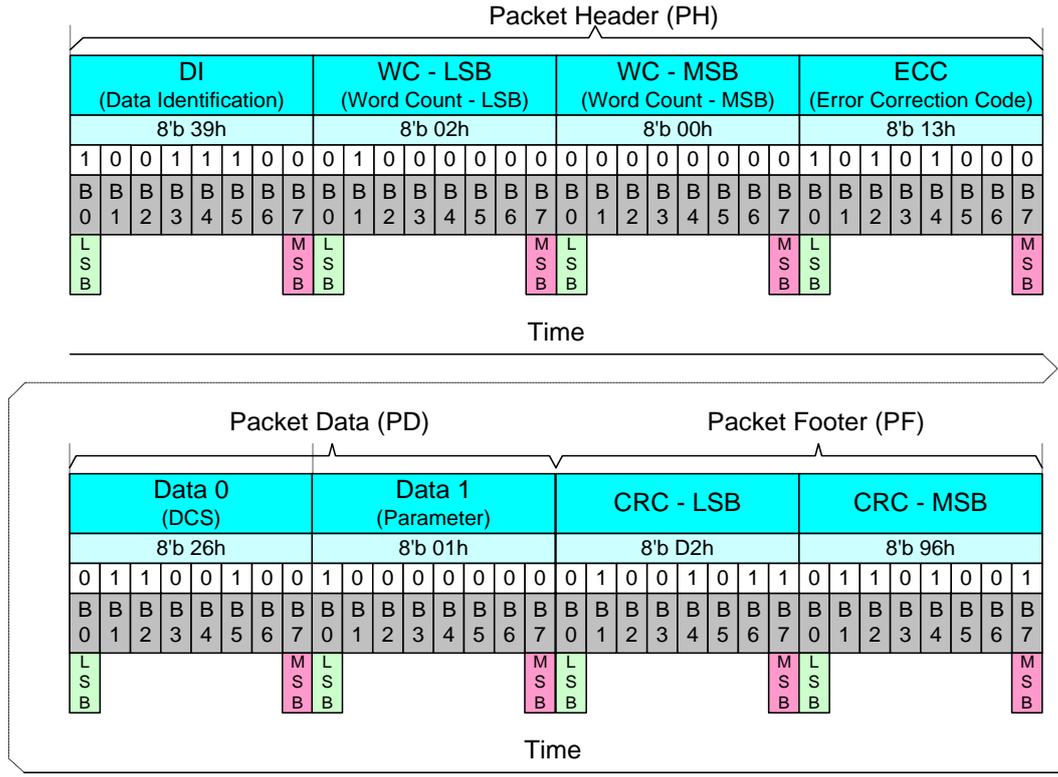


Figure 60: Display Command Set (DCS) Write Long with DCS and 1 Parameter - Example

A Long Packet (LPa) with one Write (4 parameters) is defined as:

- Data Identification (DI)
 - ✧ Virtual Channel (VC, DI [7...6]): 00b
 - ✧ Data Type (DT, DI [5...0]): 11 1001b
- Word Count (WC)
 - ✧ Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
 - ✧ Data 0: "Column Address Set (2Ah)" (For example only), Display Command Set (DCS)
 - ✧ Data 1: 00hex, 1st Parameter of the DCS, Start Column SC [15...8]
 - ✧ Data 2: 12hex, 2nd Parameter of the DCS, Start Column SC [7...0]
 - ✧ Data 3: 01hex, 3rd Parameter of the DCS, End Column EC [15...8]
 - ✧ Data 4: EFhex, 4th Parameter of the DCS, End Column EC [7...0]
- Packet Footer (PF)

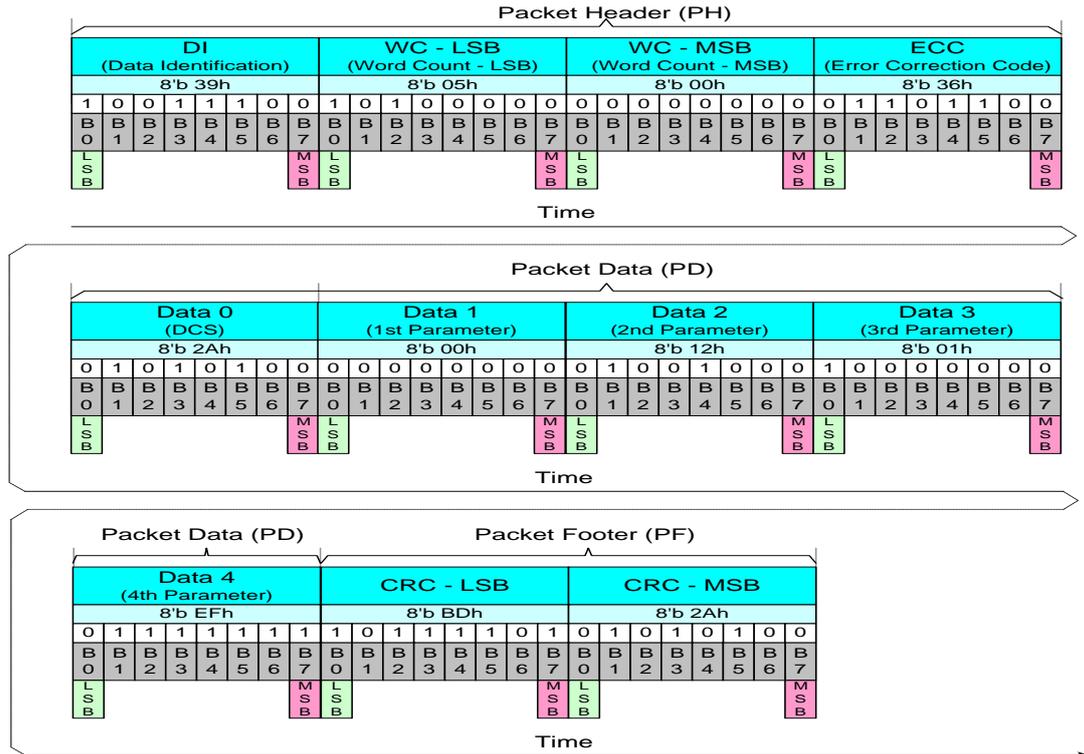


Figure 61: Display Command Set (DCS) Write Long with DCS and 4 Parameters - Example

4.1.3.2.1.5. Display Command Set (DCS) Read, No Parameter (DCSRN-S)

“Display Command Set (DCS) Read, No Parameter” (DCSRN-S), which is defined in Data Type (DT, 00 0110b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in the table below.

Table 13: Display Command Set (DCS) Read, No Parameter (DCSRN-S)

Command
Read Number of the Errors on DSI (05h)
Read Display Power Mode (0Ah)
Read Display MADCTL (0Bh)
Read Display Pixel Format (0Ch)
Read Display Image Mode (0Dh)
Read Display Signal Mode (0Eh)
Read Display Self-Diagnostic Result (0Fh)
Get Tear Scan Line(45h)
Read Display Brightness Value (52h)
Read CTRL Value Display (54h)
Read Power Save (56h)
Read CABC Minimum Brightness (5Fh)
Get Transition Time(69h)
Read DDB Start (A1h)
Read DDB Continue (A8h)
Read First Checksum(AAh)
Read Continue Checksum (AFh)
Read ID1 (DAh)
Read ID2 (DBh)
Read ID3 (DCh)

The MCU has to define to the display module the maximum size of the returned packet. The command, which is used for this purpose, is “Set Maximum Return Packet Size” (SMRPS-S), which Data Type (DT) is 11 0111b and is used in a Short Packet (SPa) before the MCU can send “Display Command Set (DCS) Read, No Parameter” to the display module. This sequence is illustrated for reference purposes below.

Step 1:

The MCU sends “Set Maximum Return Packet Size” (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module.

- Data Identification (DI)
 - ✧ Virtual Channel (VC, DI [7...6]): 00b
 - ✧ Data Type (DT, DI [5...0]): 11 0111b
- Maximum Return Packet Size (MRPS)
 - ✧ Data 0: 01hex
 - ✧ Data 1: 00hex
- Error Correction Code (ECC)

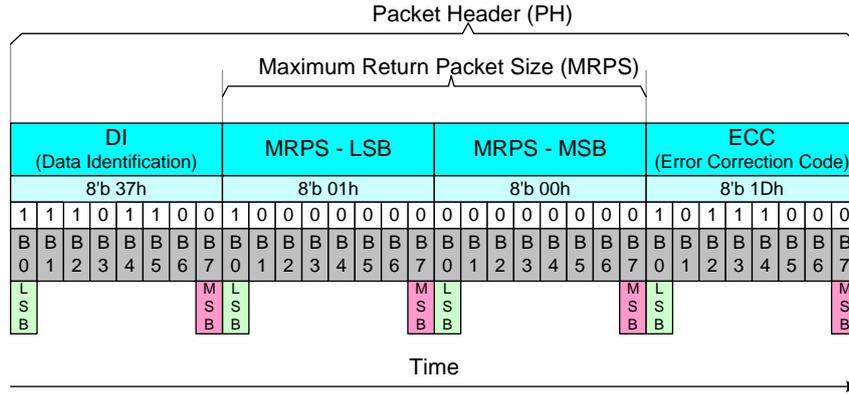


Figure 62: Set Maximum Return Packet Size (SMRPS-S) - Example

Step 2:

The MCU wants to receive the value of the “Read ID1 (DAh)” from the display module when the MCU sends “Display Command Set (DCS) Read, No Parameter” to the display module.

- Data Identification (DI)
 - ✧ Virtual Channel (VC, DI [7...6]): 00b
 - ✧ Data Type (DT, DI [5...0]): 00 0110b
- Packet Data (PD)
 - ✧ Data 0: “Read ID1 (DAh)”, Display Command Set (DCS)
 - ✧ Data 1: Always 00hex
- Error Correction Code (ECC)

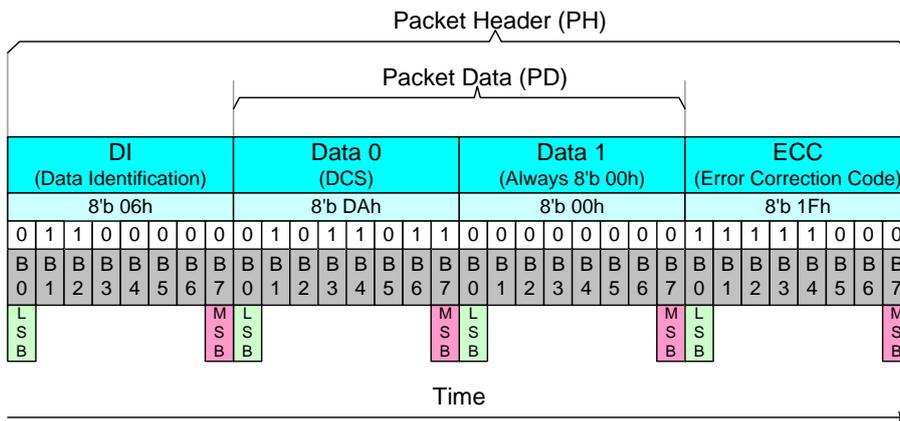


Figure 63: Display Command Set (DCS) Read, No Parameter (DCSRN-S) - Example

Step 3:

The display module can send 2 different information to the MCU after Bus Turnaround (BTA):

1. An acknowledge with Error Report (AwER), which is used in a Short Packet (SPa), if there is an error when receiving a command. See the section “4.1.3.2.2.2 Acknowledge with Error Report (AwER)”.

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2. Information of the received command, which can be a Short Packet (SPa) or a Long Packet (LPa).

4.1.3.2.1.6. Null Packet, No Data (NP-L)

“Null Packet, No Data” (NP-L), which is defined in Data Type (DT, 001001b), is always used in a Long Packet (LPa) from the MCU to the display module. The purpose of this command is to keep data lanes in the high speed mode (HSMT) if necessary. The display module can ignore the Packet Data (PD) that the MCU sends.

A Long Packet (LPa) with 5 random data bytes of the Packet Data (PD) is defined as:

- Data Identification (DI)
 - ✧ Virtual Channel (VC, DI [7...6]): 00b
 - ✧ Data Type (DT, DI [5...0]): 00 1001b
- Word Count (WC)
 - ✧ Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
 - ✧ Data 0: 89hex (Random data)
 - ✧ Data 1: 23hex (Random data)
 - ✧ Data 2: 12hex (Random data)
 - ✧ Data 3: A2hex (Random data)
 - ✧ Data 4: E2hex (Random data)
- Packet Footer (PF)

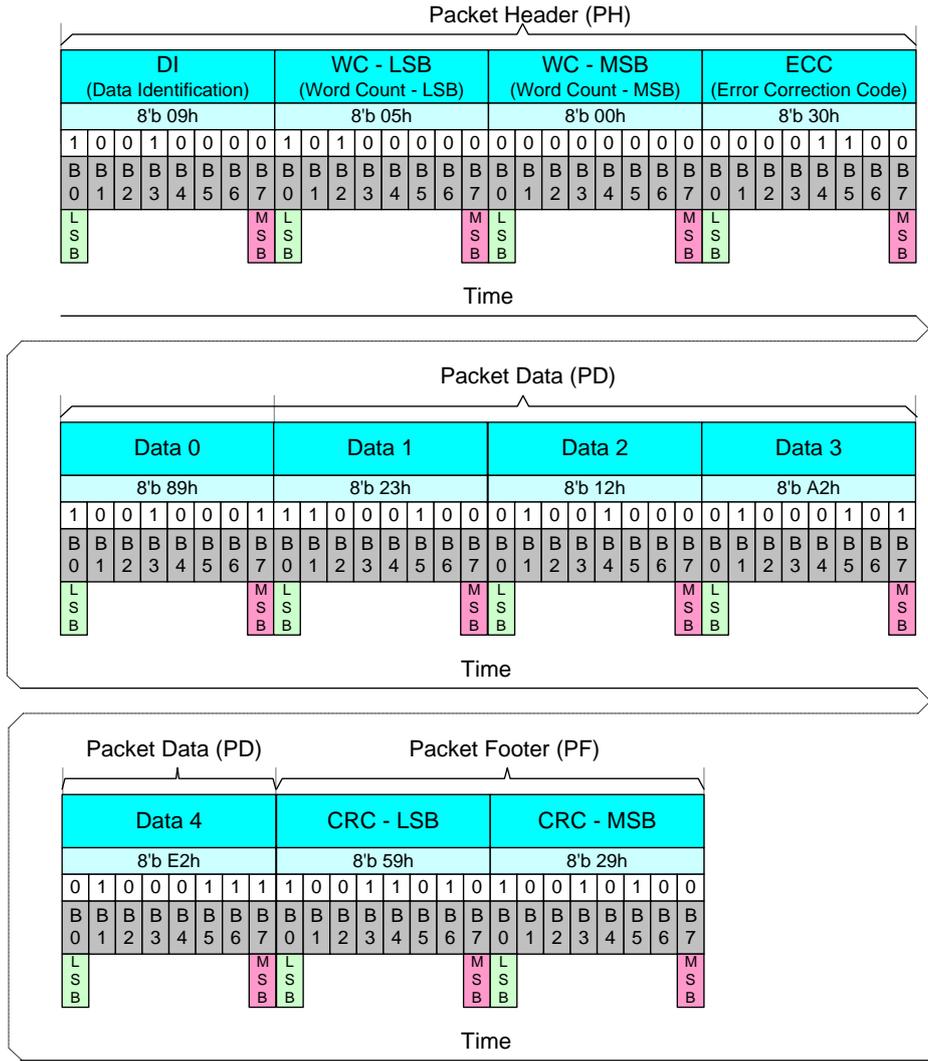


Figure 64: Null Packet, No Data (NP-L) - Example

4.1.3.2.1.7. End of Transmission Packet (EoTP)

“End of Transmission Packet” (EoTP), which is an interface level function and defined in Data Type (DT, 00 1000b), is always used in a Short Packet (SPa) from the MCU to the display module. The purpose of this command is to terminate the high Speed Data Transmission (HSDT) mode properly when EoTP is added after the last payload packet before “End of Transmission” (EoT).

The MCU can decide if it wants to use the “End of Transmission Packet” (EoTP) or not. The display shall have the capability to support both. That is, if the MCU applies the EoTP, it shall report the “DSI Protocol Violation Error” when the EoTP is not detected in the High-Speed (HS). The display module error reporting shall be enabled/disabled statistically, according to the module application.

The display module does or does not receive “End of Transmission Packet” (EoTP) from the MCU during the Low Power Data Transmission (LPDT) mode before “Mark-1” (= leaving the Escape mode) which ends the Low Power Data Transmission (LPDT) mode. The display module is not allowed to send “End of Transmission Packet” (EoTP) to the MCU during the Low Power Data Transmission (LPDT) mode. The summary of the receiving and transmitting EoTP is listed below.

Table 14: Receiving and Transmitting EoTP during LPDT

Direction	Display Module (DM) in High Speed Data Transmission (HSDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MCU => Display Module	Support With and Without EoTP	Support With and Without EoTP
Display Module => MCU	HS Mode is not available (EoTP is not available)	EoTP cannot be sent by the Display Module (DM)

A Short Packet (SPa) using a fixed format is as follows:

- Data Identification (DI)
 - ✧ Virtual Channel (VC, DI [7...6]): 00b
 - ✧ Data Type (DT, DI [5...0]): 00 1000b
- Packet Data (PD)
 - ✧ Data 0: 0Fhex
 - ✧ Data 1: 0Fhex
- Error Correction Code (ECC)
 - ✧ ECC: 01hex

4.1.3.2.2. Packet from the Display Module to the MCU

4.1.3.2.2.1. Used Packet types

The display module always uses Short Packets (SPa) or Longs Packet (LPa) when returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS) (See the section “4.1.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)”) or an Acknowledge with Error Report (See the section “4.1.3.2.2.2 Acknowledge with Error Report (AwER)”).

The used packet type is defined on Data Type (DT). See the section “4.1.3.1.3.1.2 Data Type (DT)”. If the maximum size of the Packet Data (PD) could be sent in one packet, the display module should not send returned bytes in several packets. Both cases are illustrated for reference purposes below.

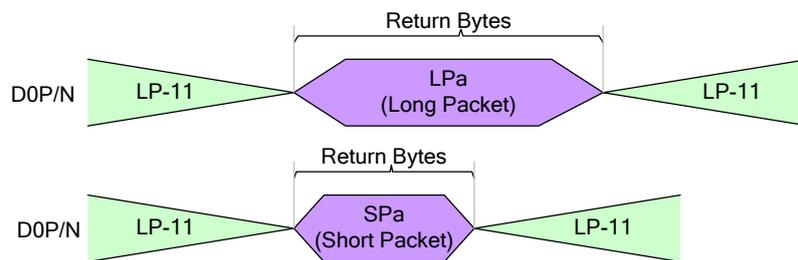


Figure 67: Return Bytes in Single Packet

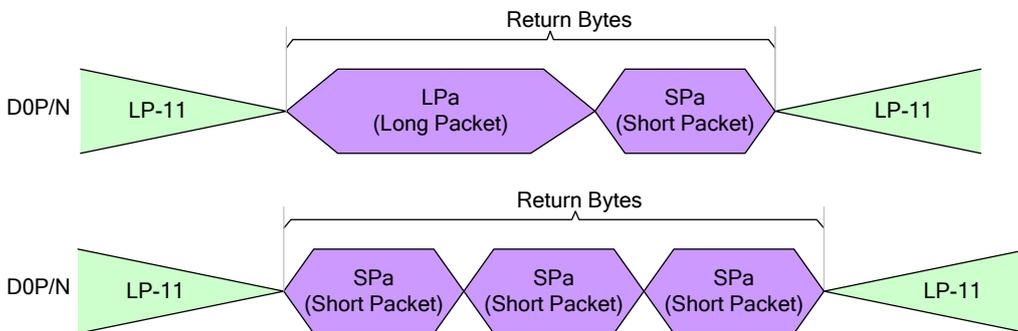


Figure 68: Return Bytes in Several Packets – Not Allowed

EXCEPTION:

The display module will return 2 packets (1st packet: Data, 2nd Packet: Acknowledge with Error Report) to the MCU when the display module receives a read command (See section “4.1.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)”), which is detected and corrected a single bit error by the EEC (See bit 8 in Table 15). These returned packets are illustrated for reference purposes below.

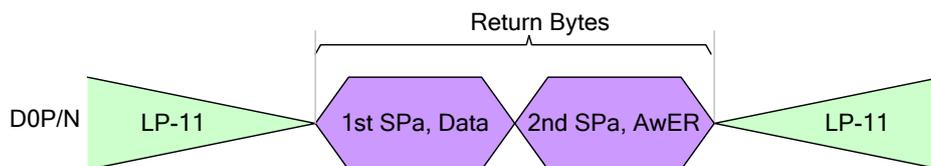


Figure 69: Exception when Returned Bytes in Several Packets

AwER = Acknowledge with Error Report

4.1.3.2.2.2. Acknowledge with Error Report (AwER)

“Acknowledge with Error Report” (AwER), which is defined in Data Type (DT, 00 0010b), is always used in a Short Packet (SPa) from the display module to the MCU. The Packet Data (PD) can include bits, which define the current error, when the corresponding bit is set to 1, as defined in the following table.

Table 15: Error Report (AwER) Bit Definitions

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long Packet only)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to 0 internally
15	DSI Protocol Violation

These errors are included in all packages that have been received from the MCU to the display module before the Bus Turnaround (BTA). The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of a Short Packet (SPa) is defined as:

- Data Identification (DI)
 - ✧ Virtual Channel (VC, DI [7...6]): 00b
 - ✧ Data Type (DT, DI [5...0]): 00 0010b
- Packet Data (PD)
 - ✧ Bit 8: ECC Error, single-bit (detected and corrected)
 - ✧ AwER: 0100h
- Error Correction Code (ECC)

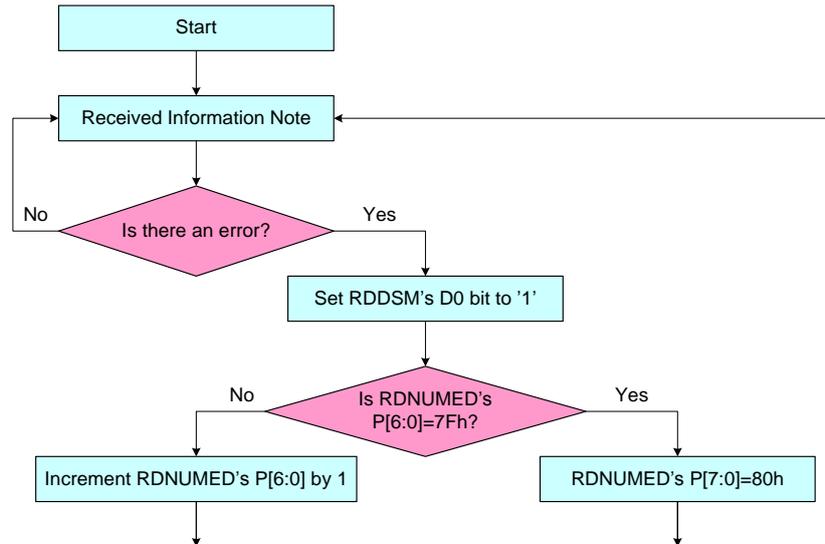


Figure 72: Flow Chart for Errors on DSI

Notes:

1. This information can be Interface or Packet Level Communication, but it is always from the MCU to the display module.
2. CRC or ECC error

4.1.3.2.2.3. DCS Read Long Response (DCSRR-L)

“DCS Read Long Response” (DCSRR-L), which is defined in Data Type (DT, 011100b), is always used in a Long Packet (LPa) from the display module to the MCU. “DCS Read Long Response” (DCSRR-L) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), is defined as:

- Data Identification (DI)
 - ✧ Virtual Channel (VC, DI [7...6]): 00b
 - ✧ Data Type (DT, DI [5...0]): 01 1100b
- Word Count (WC)
 - ✧ Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
 - ✧ Data 0: 89hex
 - ✧ Data 1: 23hex
 - ✧ Data 2: 12hex
 - ✧ Data 3: A2hex
 - ✧ Data 4: E2hex
- Packet Footer (PF)

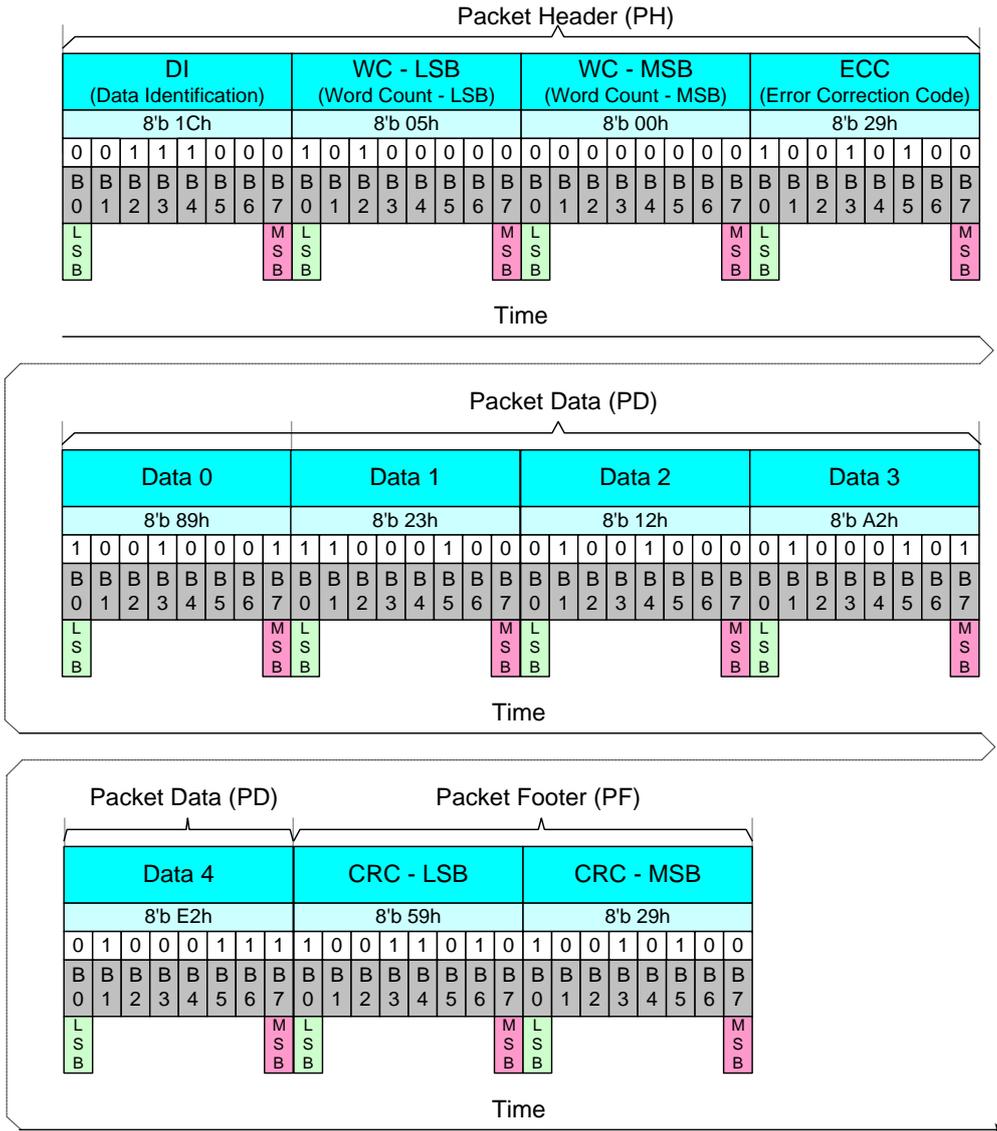


Figure 73: DCS Read Long Response (DCSRR-L) - Example

4.1.3.2.2.4. DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

“DCS Read Short Response, 1 Byte Returned” (DCSRR1-S), which is defined in Data Type (DT, 10 0001b), is always used in a Short Packet (SPa) from the display module to the MCU. “DCS Read Short Response, 1 Byte Returned (DCSRR1-S) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Short Packet (SPa) is defined as:

- Data Identification (DI)
 - ✧ Virtual Channel (VC, DI [7...6]): 00b
 - ✧ Data Type (DT, DI [5...0]): 10 0001b
- Packet Data (PD)
 - ✧ Data 0: 45hex
 - ✧ Data 1: 00hex (Always)
- Error Correction Code (ECC)

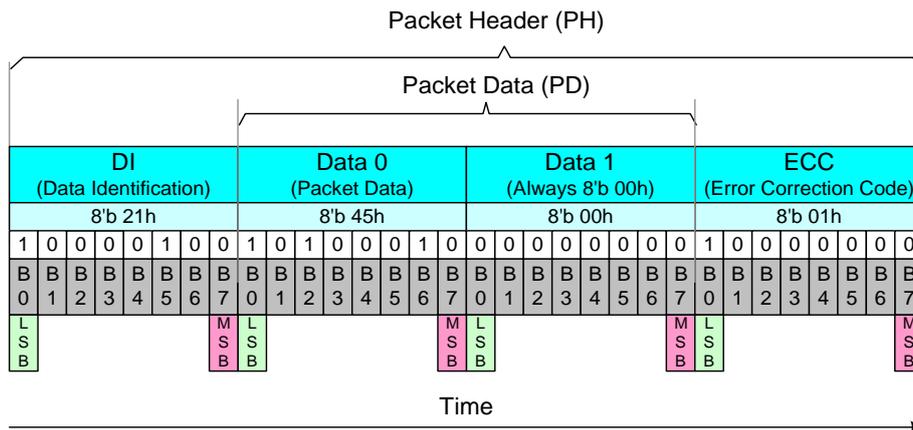


Figure 74: DCS Read Short Response, 1 Byte Returned (DCSRR1-S) - Example

4.1.3.2.2.5. DCS Read Short Response, 2 Bytes Returned (DCSRR2-S)

“DCS Read Short Response, 2 Bytes Returned” (DCSRR2-S), which is defined in Data Type (DT, 10 0010b), is always used in a Short Packet (SPa) from the display module to the MCU. “DCS Read Short Response, 2 Bytes Returned” (DCSRR2-S) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Short Packet (SPa) is defined as:

- Data Identification (DI)
 - ✧ Virtual Channel (VC, DI [7...6]): 00b
 - ✧ Data Type (DT, DI [5...0]): 10 0010b
- Packet Data (PD)
 - ✧ Data 0: 45hex
 - ✧ Data 1: 32hex
- Error Correction Code (ECC)

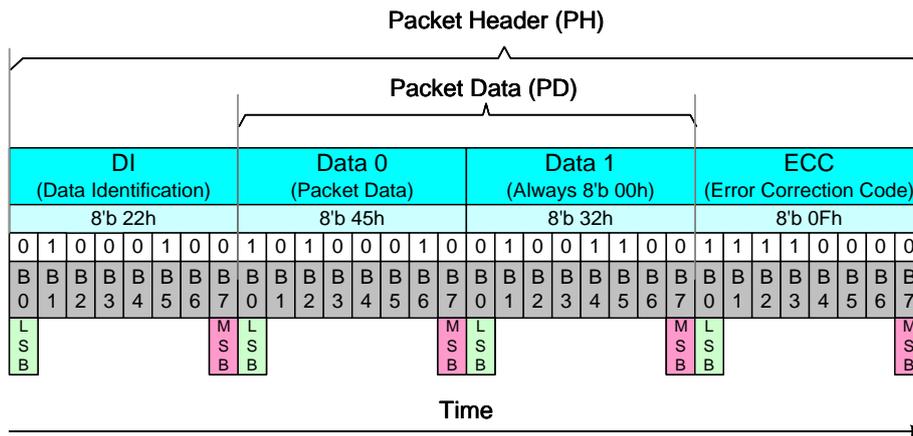


Figure 75: DCS Read Short Response, 2 Bytes Returned (DCSRR2-S) - Example

4.1.3.3. Communication Sequences

4.1.3.3.1. General

The communication sequences can be done on interface or packet levels between the MCU and the display module. See sections “4.1.2 Interface Level Communication” and “4.1.3 Packet Level Communication”. This communication sequence description is for DSI data lanes (D3P/N, D2P/N, D1P/N and D0P/N), and it is assumed that the needed low level communication is done on DSI Clock lane (CLKP/N) automatically. See the section “4.1.2.2 DSI CLK Lanes”. Functions of the interface level communication are described in the following table.

Table 16: Interface Level Communication

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop State
	LPDT	Low Power Data Transmission
	ULPS	Ultra-Low Power State
	RAR	Remote Application Reset
	ACK	Acknowledge (No Error)
	BTA	Bus Turnaround
High Speed	HSDT	High speed Data Transmission

Functions of the packet level communication are described in the following table.

Table 17: Packet Level Communication for MCU-sourced Packets

Interface Mode	Abbreviation	Packet Size	Interface Action Description
MCU	VSS	Short Packet	Sync Event, V Sync Start
	VSE	Short Packet	Sync Event, V Sync End
	HSS	Short Packet	Sync Event, H Sync Start
	HSE	Short Packet	Sync Event, H Sync End
	EoTP	Short Packet	End of Transmission Packet (EoTP) ^{Note1}
	CMOFF	Short Packet	Color Mode Off Command
	CMON	Short Packet	Color Mode On Command
	SDNP	Short Packet	Shut Down Peripheral Command
	TONP	Short Packet	Turn On Peripheral Command
	GENWN-S	Short Packet	Generic Short WRITE, no parameters
	GENW1-S	Short Packet	Generic Short WRITE, 1 parameters
	GENW2-S	Short Packet	Generic Short WRITE, 2 parameters
	GENRN-S	Short Packet	Generic Short READ, no parameters
	GENR1-S	Short Packet	Generic Short READ, 1 parameters
	GENR2-S	Short Packet	Generic Short READ, 2 parameters
	DCSWN-S	Short Packet	DCS Write, No Parameter
	DCSW1-S	Short Packet	DCS Write, 1 Parameter
	DCSRN-S	Short Packet	DCS Read, No Parameter
	SMRPS-S	Short Packet	Set Maximum Return Packet Size
	NP-L	Long Packet	Null Packet, No Data, ^{Note2}
	BLK-L	Long Packet	Blanking Packet, no data
	GENW-L	Long Packet	Generic Long Write
	DCSW-L	Long Packet	DCS Write Long
	PKPS16	Long Packet	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format
	PKPS18	Long Packet	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format
	LPKPS18	Long Packet	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format
	PKPS24	Long Packet	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format

Table 18: Packet Level Communication for Peripheral-sourced packets

Interface Mode	Abbreviation	Packet Size	Interface Action Description
Display Module (ILI9881C-04)	AwER	Short Packet	Acknowledge with Error Report
	EoTP	Short Packet	End of Transmission Packet
	GENRR1-S	Short Packet	Generic Short READ Response, 1 byte returned
	GENRR2-S	Short Packet	Generic Short READ Response, 2 byte returned
	GENRR-L	Long Packet	Generic Long READ Response
	DCSRR-L	Long Packet	DCS Read Long Response
	DCSRR1-S	Short Packet	DCS Read Short Response, 1 byte returned
	DCSRR2-S	Short Packet	DCS Read Short Response, 2 byte returned

4.1.3.3.2. Sequences

4.1.3.3.2.1. DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is defined in the section “4.1.3.2.1.3 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” and example sequences on how this packet is used are described in following tables.

Table 19: DCS Write, 1 Parameter Sequence – Example 1

DCS Write, 1 Parameter Sequence – Example 1						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 20: DCS Write, 1 Parameter Sequence – Example 2

DCS Write, 1 Parameter Sequence – Example 2						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 21: DCS Write, 1 Parameter Sequence – Example 3

DCS Write, 1 Parameter Sequence – Example 3						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW1-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	↔	BTA	--	Interface Control Change from MCU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	↔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	↔	BTA	--	
16	--	LP-11	→	--	--	End

4.1.3.3.2.2. DCS Write, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” is defined in the section “4.1.3.2.1.2 Display Command Set (DCS) Write, No Parameter (DCSWN-S)” and example sequences on how this packet is used are described in following tables.

Table 22: DCS Write, No Parameter Sequence – Example 1

DCS Write, No Parameter Sequence – Example 1						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 23: DCS Write, No Parameter Sequence – Example 2

DCS Write, No Parameter Sequence – Example 2						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 24: DCS Write, No Parameter Sequence – Example 3

DCS Write, 1 Parameter Sequence – Example 3						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSWN-S	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	↔	BTA	--	Interface Control Change from MCU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	↔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	↔	BTA	--	
16	--	LP-11	→	--	--	End

4.1.3.3.2.3. DCS Write Long Sequence

A Long Packet (LPa) of “Display Command Set (DCS) Write Long (DCSW-L)” is defined in the section “4.1.3.2.1.4 Display Command Set (DCS) Write Long (DCSW-L)” and example sequences on how this packet is used are described in following tables.

Table 25: DCS Write Long Sequence – Example 1

DCS Write Long Sequence – Example 1						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	LPDT	→	--	--	
3	--	LP-11	→	--	--	End

Table 26: DCS Write Long Sequence – Example 2

DCS Write Long Sequence – Example 2						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	End

Table 27: DCS Write Long Sequence – Example 3

DCS Write Long Sequence – Example 3						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	DCSW-L	HSDT	→	--	--	
3	EoTP	HSDT	→	--	--	End of Transmission Packet
4	--	LP-11	→	--	--	
5	--	BTA	↔	BTA	--	Interface Control Change from MCU to the display module
6	--	--	←	LP-11	--	If No Error → Go to Line 8 If Error Occurs → Go to Line 13
7						
8	--	--	←	ACK	--	No Error
9	--	--	←	LP-11	--	
10	--	BTA	↔	BTA	--	Interface Control Change from the display module to MCU
11	--	LP-11	→	--	--	End
12						
13	--	--	←	LPDT	AwER	Error Report
14	--	--	←	LP-11	--	
15	--	BTA	↔	BTA	--	
16	--	LP-11	→	--	--	End

4.1.3.3.2.4. DCS Read, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” is defined in the section “4.1.3.2.1.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)” and example sequences on how this packet is used are described in following tables.

Table 28: DCS Read, No Parameter Sequence – Example 1

DCS Read, No Parameter Sequence – Example 1						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	→	--	--	Start
2	SMRPS-S	HSDT	→	--	--	Defined how many data byte is wanted to read : 1 byte
3	DCSRN-S	HSDT	→	--	--	Wanted to get a response ID1 (DAh)
4	EoTP	HSDT	→	--	--	End of Transmission Packet
5	--	LP-11	→	--	--	
6	--	BTA	↔	BTA	--	Interface Control Change from MCU to the display module
7	--	--	←	LP-11	--	If No Error → Go to Line 9 If Error Occurs → Go to Line 14 If Error is Corrected by ECC → Go to Line 19
8						
9	--	--	←	LPDT	DCSRR1-S	Response 1 byte return
10	--	--	←	LP-11	--	
11	--	BTA	↔	BTA	--	Interface Control Change from the display module to MCU
12	--	LP-11	→	--	--	End
13						
14	--	--	←	LPDT	AwER	Error Report
15	--	--	←	LP-11	--	
16	--	BTA	↔	BTA	--	Interface Control Change from the display module to MCU
17	--	LP-11	→	--	--	End
18						
19	--	--	←	LPDT	DCSRR1-S	Response 1 byte return
20	--	--	←	LPDT	AwER	Error Report (Error is corrected by ECC)
21			←	LP-11	--	
22	--	BTA	↔	BTA	--	Interface Control Change from the display module to MCU
23	--	LP-11	→	--	--	End

Table 29: DCS Read, No Parameter Sequence – Example 2

DCS Read, No Parameter Sequence – Example 2						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	➔	--	--	Start
2	SMRPS-S	HSDT	➔	--	--	Defined how many data byte is wanted to read : 200 bytes
3	DCSRN-S	HSDT	➔	--	--	Wanted to get a response
4	EoTP	HSDT	➔	--	--	End of Transmission Packet
5	--	LP-11	➔	--	--	
6	--	BTA	↔	BTA	--	Interface Control Change from MCU to the display module
7	--	--	←	LP-11	--	If No Error ➔ Go to Line 9 If Error Occurs ➔ Go to Line 14 If Error is Corrected by ECC ➔ Go to Line 19
8						
9	--	--	←	LPDT	DCSRR-L	Response 200 byte return
10	--	--	←	LP-11	--	
11	--	BTA	↔	BTA	--	Interface Control Change from the display module to MCU
12	--	LP-11	➔	--	--	End
13						
14	--	--	←	LPDT	AwER	Error Report
15	--	--	←	LP-11	--	
16	--	BTA	↔	BTA	--	Interface Control Change from the display module to MCU
17	--	LP-11	➔	--	--	End
18						
19	--	--	←	LPDT	DCSRR-S	Response 200 byte return
20	--	--	←	LPDT	AwER	Error Report (Error is corrected by ECC)
21	--	--	←	LP-11	--	
22	--	BTA	↔	BTA	--	Interface Control Change from the display module to MCU
23	--	LP-11	➔	--	--	End

4.1.3.3.2.5. Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined in the section “4.1.3.2.1.6 Null Packet, No Data (NP-L)”, and an example sequence on how this packet is used is described in the following table.

Table 30: Null Packet, No Data Sequence - Example

Null Packet, No Data Sequence – Example						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	➔	--	--	Start
2	NP-L	HSDT	➔	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	➔	--	--	End of Transmission Packet
4	--	LP-11	➔	--	--	End

4.1.3.3.2.6. End of Transmission Packet

A Short Packet (SPa) of “End of Transmission (EoTP)” is defined in the section “4.1.3.2.1.7 End of Transmission Packet (EoTP)”, and an example sequence on how this packet is used is described in the following table.

Table 31: End of Transmission Packet – Example

End of Transmission Packet – Example						
Line	MCU		Information Direction	Display Module (ILI9881C-04)		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	--	LP-11	➔	--	--	Start
2	NP-L	HSDT	➔	--	--	Only High Speed Data Transmission is used
3	EoTP	HSDT	➔	--	--	End of Transmission Packet
4	--	LP-11	➔	--	--	End

4.2. Display Data Format

4.2.1. DSI Transmission Data Format

4.2.1.1. 16-bit per Pixel, Long Packet, Data Type 00 1110 (0Eh)

Packed Pixel Stream 16-Bit Format is a Long Packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is red (5 bits), green (6 bits), and blue (5 bits), in that order. Note that the Green component is split across two bytes. Within a color component, the LSB is sent first, the MSB last. With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.

Normally, the ILI9881C-04 has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifacts.

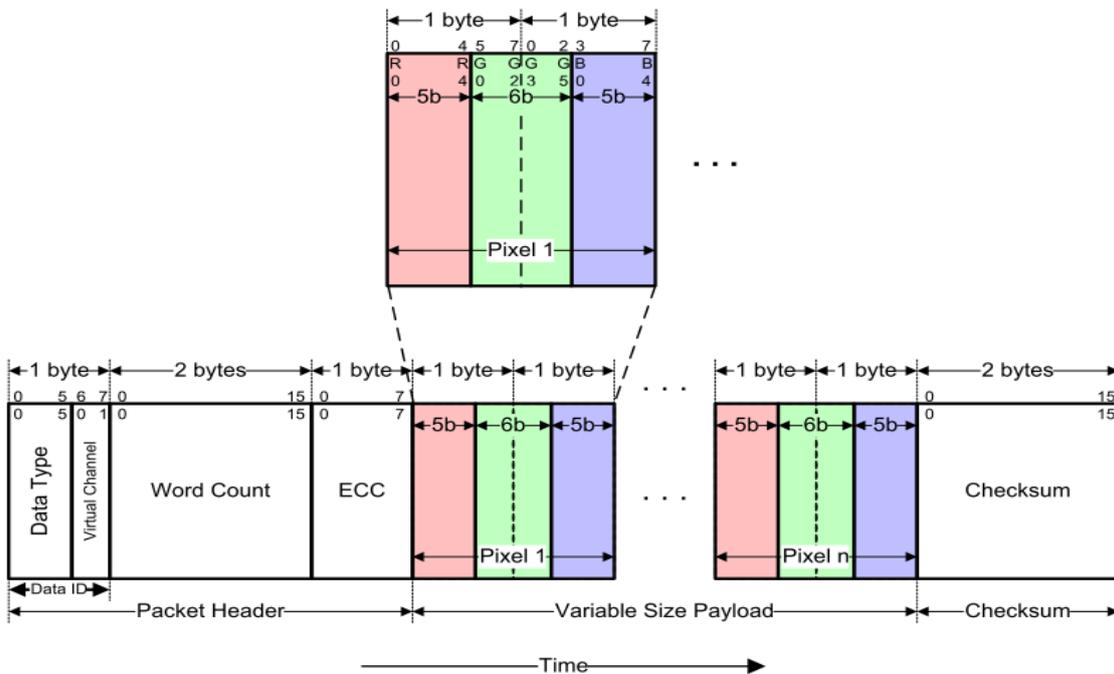


Figure 76: 16-bit per Pixel, Data Type 00 1110 (0Eh)

4.2.1.2. 18-bit per Pixel, Long Packet, Data Type = 01 1110 (1Eh)

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes, and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last.

Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional filled pixels at the end of the display line to make the transmitted width a

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multiple of four pixels. The receiving peripheral shall not display the filled pixels when refreshing the display device. For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission. With this format, the total line width (displayed and non-displayed pixels) should be a multiple of four pixels (nine bytes).

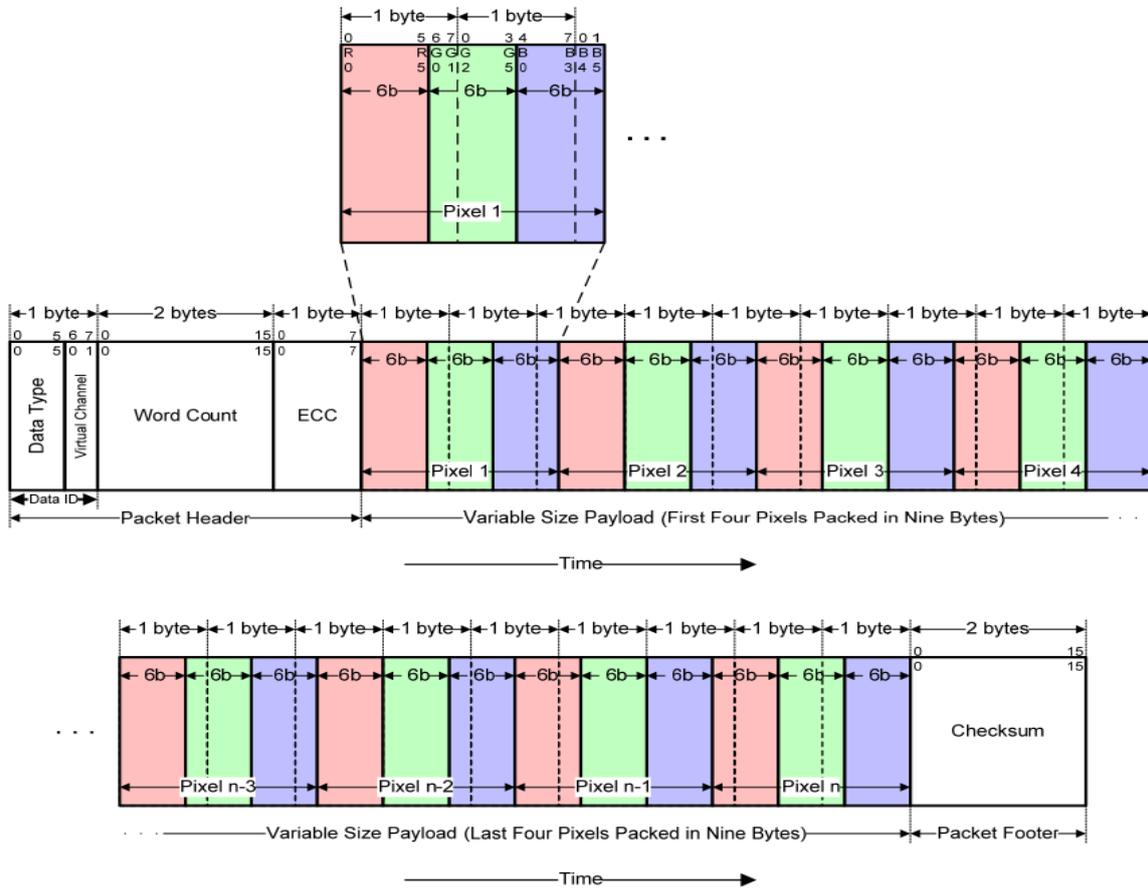


Figure 77: 18-bit per Pixel, Data Type = 01 1110 (1Eh)

4.2.1.3. 18-bit per Pixel, Long Packet, Data Type = 10 1110 (2Eh)

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed and non-displayed pixels) should be a multiple of three bytes.

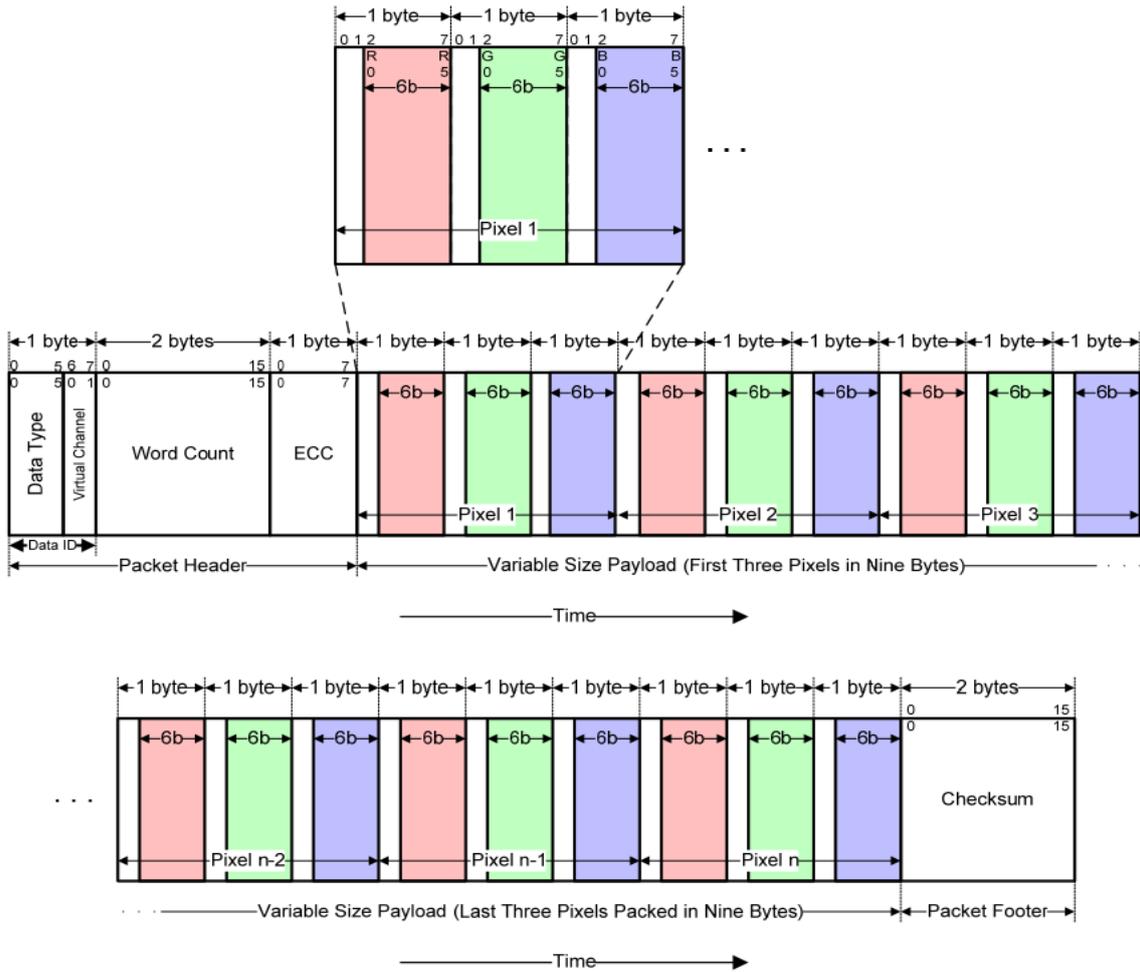


Figure 78: 18-bit per Pixel, Data Type = 10 1110 (2Eh)

4.2.1.4. 24-bit per Pixel, Long Packet, Data Type = 11 1110 (3Eh)

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last.

With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed and non-displayed pixels) should be a multiple of three bytes.

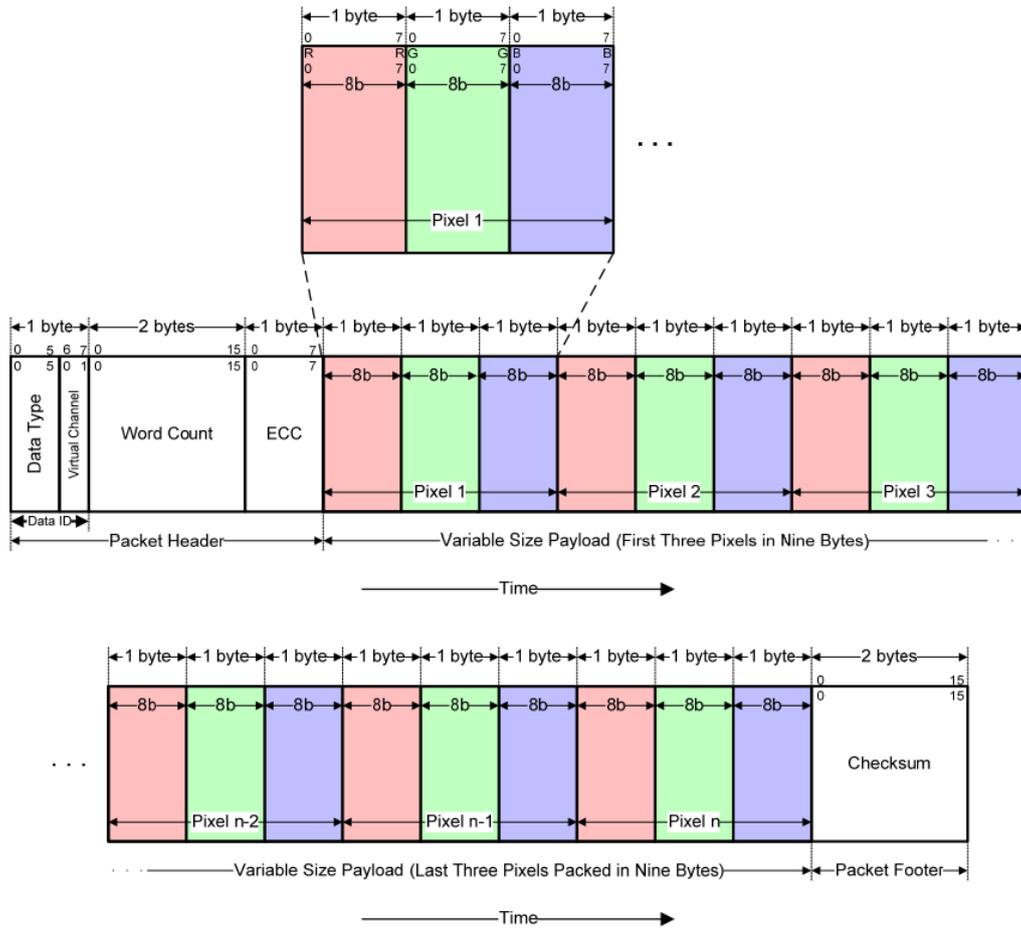


Figure 79: 24-bit per Pixel, Data Type = 11 1110 (3Eh)

4.2.2. 16/18-bit Color Data Mapping to 24-bit Pixel Data Operation

Table 32 below lists settings for 24-bit data mapping. Set the EPF[1:0] bits function, which defines three types of data formats for 24-bit data (pixel data r, g, b) mapping.

Table 32: 16/18-bit Color Data Mapping to 24-bit Pixel Data Operation

EPF[1:0]	Expand 16-bit color data (R,G,B) to 24-bit subpixel data (r, g, b)	Expand 18-bit color data (R,G,B) to 24-bit subpixel data (r, g, b)
00	0 is written to the LSB. 8 bits subpixel, data r [7:0] = {16-bit color data R [4:0], 3'h0} 8 bits subpixel, data g [7:0] = {16-bit color data G [5:0], 2'h0} 8 bits subpixel, data b [7:0] = {16-bit color data B [4:0], 3'h0} (Note3): that the data are converted as follows. 16-bit color data R [4:0] = 5'h1F, G [5:0] = 6'h3F, B [4:0] = 5'h1F → 24-bit pixel data r, g, b [7:0] = 24'hFFFFFF	0 is written to the LSB. 8 bits subpixel, data r [7:0] = {18-bit color data R [5:0], 2'h0} 8 bits subpixel, data g [7:0] = {18-bit color data G [5:0], 2'h0} 8 bits subpixel, data b [7:0] = {18-bit color data B [5:0], 2'h0} (Note1): that the data are converted as follows. 18-bit color data R [5:0] = 6'h3F, G [5:0] = 6'h3F, B [5:0] = 6'h3F → 24-bit pixel data r, g, b [7:0] = 24'hFFFFFF
01	1 is written to the LSB. 8 bits subpixel, data r [7:0] = {16-bit color data R [4:0], 3'h7} 8 bits subpixel, data g [7:0] = {16-bit color data G [5:0], 2'h3} 8 bits subpixel, data b [7:0] = {16-bit color data B [4:0], 3'h7} (Note4): that the data are converted as follows. 16-bit color data R [4:0] = 5'h0, G [5:0] = 6'h0, B [4:0] = 5'h0 →24-bit pixel data r, g, b [7:0] = 24'h000000	1 is written to the LSB. 8 bits subpixel, data r [7:0] = {18-bit color data R [5:0], 2'h3} 8 bits subpixel, data g [7:0] = {18-bit color data G [5:0], 2'h3} 8 bits subpixel, data b [7:0] = {18-bit color data B [5:0], 2'h3} (Note2): that the data are converted as follows. 18-bit color data R [5:0] = 6'h0, G [5:0] = 6'h0, B [5:0] = 6'h0 →24-bit pixel data r, g, b [7:0] = 24'h000000
10	The MSB value is written to the LSB. 8 bits subpixel, data r [7:0] = {16-bit color data R [4:0], R [4:2]} 8 bits subpixel, data g [7:0] = {16-bit color data G [5:0], G [5:4]} 8 bits subpixel, data b [7:0] = {16-bit color data B [4:0], B [4:2]}	The MSB value is written to the LSB. 8 bits subpixel, data r [7:0] = {18-bit color data R [5:0], R [5:4]} 8 bits subpixel, data g [7:0] = {18-bit color data G [5:0], G [5:4]} 8 bits subpixel, data b [7:0] = {18-bit color data B [5:0], B [5:4]}
11	Same as setting "EPF [1:0] = 10"	Same as setting "EPF [1:0] = 10"

	Display image data (24 bits)																							
	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
24-bit	R[7]	R[6]	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[7]	G[6]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]
18-bit EPF[1:0]=00 (Note 1)	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	0	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	0	0	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	0	0
18-bit EPF[1:0]=01 (Note 2)	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	1	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	1	1	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	1	1
18-bit EPF[1:0]=10	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	R[5]	R[4]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	G[5]	G[4]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]	B[5]	B[4]
16-bit EPF[1:0]=00 (Note 3)	R[4]	R[3]	R[2]	R[1]	R[0]	0	0	0	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	0	0	B[4]	B[3]	B[2]	B[1]	B[0]	0	0	0
16-bit EPF[1:0]=01 (Note 4)	R[4]	R[3]	R[2]	R[1]	R[0]	1	1	1	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	1	1	B[4]	B[3]	B[2]	B[1]	B[0]	1	1	1
16-bit EPF[1:0]=10	R[4]	R[3]	R[2]	R[1]	R[0]	R[4]	R[3]	R[2]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	G[5]	G[4]	B[4]	B[3]	B[2]	B[1]	B[0]	B[4]	B[3]	B[2]

Example 1: 16-bit data mapping to 24-bit, EPF[1:0] = 10

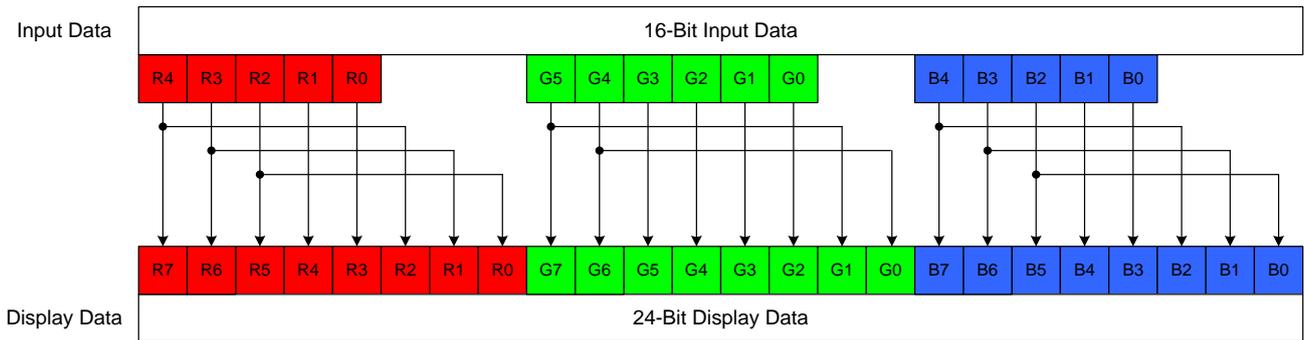


Figure 80: EPF[1:0] = 10, 16-bit Data Mapping to 24-bit

Example 2: 18-bit data mapping to 24-bit, EPF[1:0] = 10

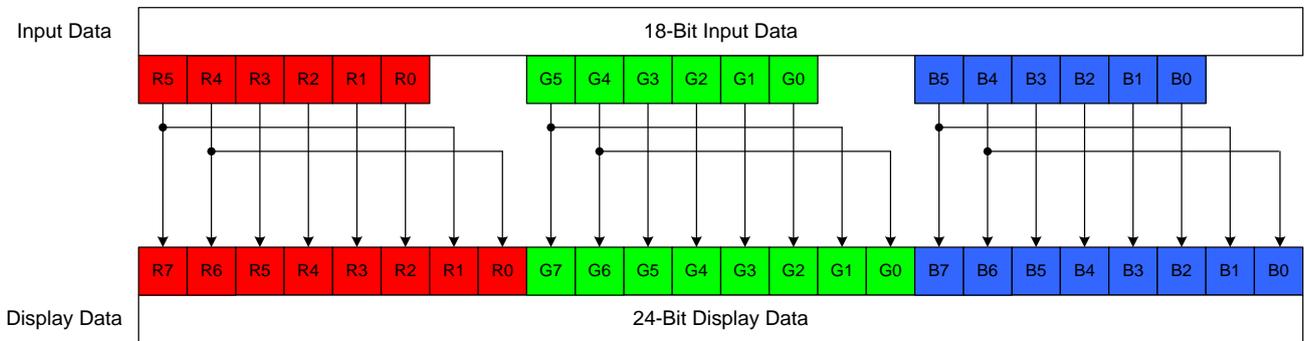


Figure 81: EPF[1:0] = 10, 18-bit Data Mapping to 24-bit

5. Command

5.1. Command Flow

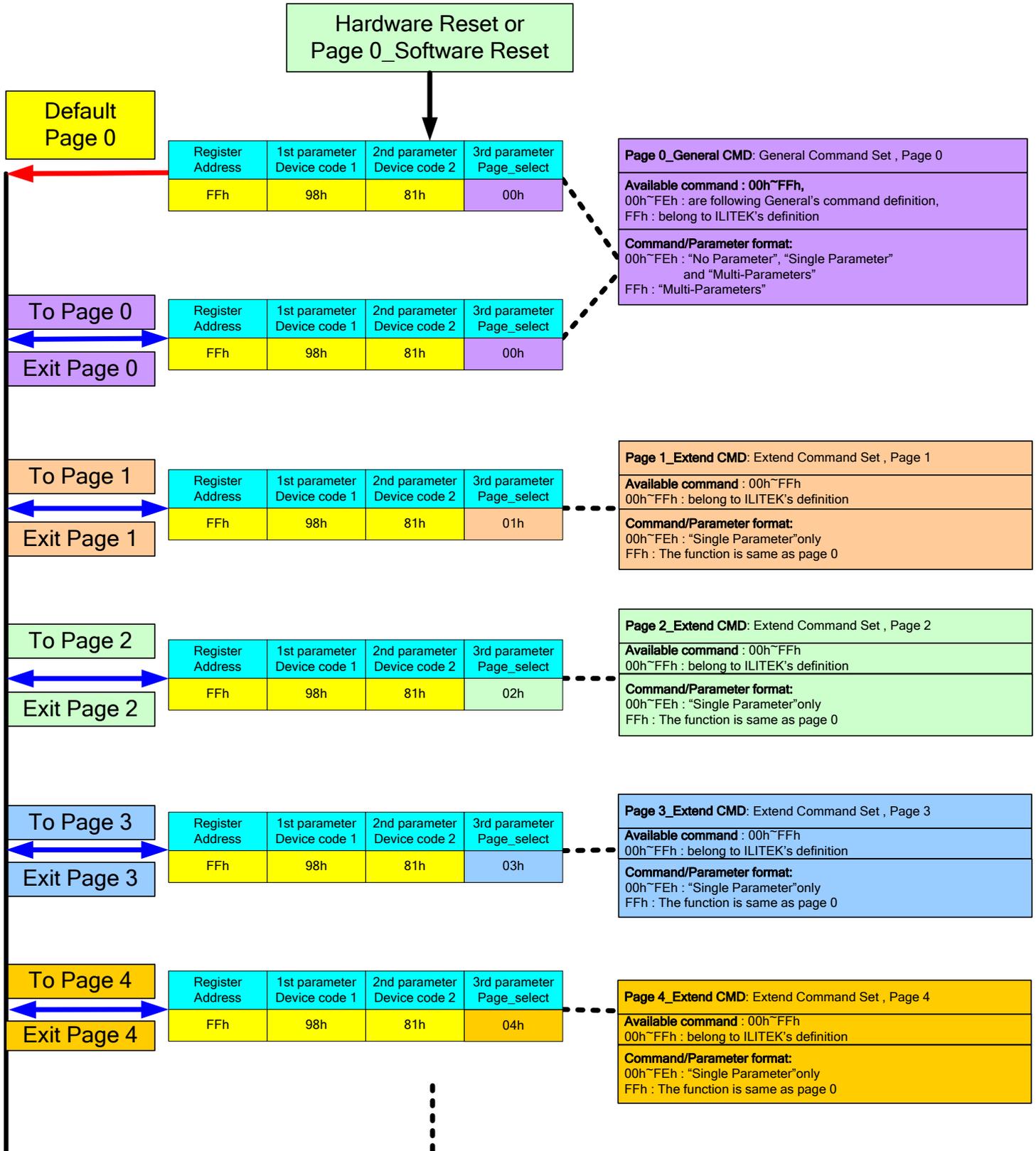


Figure 82: Command Flow

5.2. Command List

5.2.1. Page 0 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P0	00h	-	W	NOP	No Argument								-	-
P0	01h	-	W	Software Reset	No Argument								-	-
P0	05h	1st	R	Read Number of the Errors on DSI	P[7:0]								00h	-
P0	09h	1st	R	Read Display Status	D31	0	0	0	0	D26	0	D24	00h	-
		2nd	R		D23	0	0	0	D19	0	D17	D16	01h	-
		3rd	R		0	0	0	D12	D11	D10	D9	D8	00h	-
		4th	R		D7	D6	D5	0	0	0	0	D0	00h	-
P0	0Ah	1st	R	Read Display Power Mode	D7	D6	0	D4	D3	D2	0	0	08h	-
P0	0Bh	1st	R	Read Display MADCTL	0	0	0	0	D3	0	D1	D0	00h	-
P0	0Ch	1st	R	Read Pixel Format	0	0	0	0	0	D2	D1	D0	07h	-
P0	0Dh	1st	R	Read Display Mode	0	0	0	D4	D3	D2	D1	D0	00h	-
P0	0Eh	1st	R	Read Display signal Mode	D7	D6	0	0	0	0	0	D0	00h	-
P0	0Fh	1st	R	Read Display Self-Diagnostic Result	D7	D6	0	0	0	0	0	D0	00h	-
P0	10h	-	W	Sleep In	No Argument								-	-
P0	11h	-	W	Sleep Out	No Argument								-	-
P0	13h	-	W	Normal Display Mode On	No Argument								-	-
P0	22h	-	W	All Pixel Off	No Argument								-	-
P0	23h	-	W	All Pixel On	No Argument								-	-
P0	26h	1st	W	Gamma Curve Set	0	0	0	0	GC[3:0]			01h	-	
P0	28h	-	W	Display Off	No Argument								-	-
P0	29h	-	W	Display ON	No Argument								-	-
P0	34h	-	W	TE OFF	No Argument								-	-
P0	35h	1st	W	TE ON	0	0	0	0	0	0	0	M	00h	-
P0	36h	1st	W	Memory Access	0	0	0	0	BGR	0	SS	GS	00h	-
P0	38h	-	W	Idle Mode Off	No Argument								-	-
P0	39h	-	W	Idle Mode On	No Argument								-	-
P0	3Ah	1st	W	Interface Pixel Format	0	0	0	0	0	DBI[2:0]			07h	-
P0	44h	1st	W	Set tear scan line	0	0	0	0	0	TE_LINE[10:8]			00h	-
		TE_LINE[7:0]								00h	-			
P0	45h	1st	R	Get tear scan line	0	0	0	0	0	TE_LINE[10:8]			00h	-
		TE_LINE[7:0]								00h	-			
P0	51h	1st	W	Write Display Brightness	0	0	0	0	DBV[11:8]			00h	-	
		DBV[7:0]								00h	-			
P0	52h	1st	R	Read Display Brightness Value	0	0	0	0	DBV[11:8]			00h	-	
		DBV[7:0]								00h	-			
P0	53h	1st	W	Write CTRL Display	0	0	BCTRL	0	DD	BL	0	0	00h	-
P0	54h	1st	R	Read CTRL Display	0	0	BCTRL	0	DD	BL	0	0	00h	-
P0	55h	1st	W	Write Power Save	PWRSAVE[7:0]								00h	-
P0	56h	1st	R	Read Power Save	PWRSAVE[7:0]								00h	-
P0	59h	-	W	Stop Transition	No Argument								-	-
P0	5Eh	1st	W	Write CABG Minimum Brightness	0	0	0	0	CMB[11:8]			00h	-	
		CMB[7:0]								00h	-			
P0	5Fh	1st	R	Read CABG Minimum Brightness	0	0	0	0	CMB[11:8]			00h	-	
		CMB[7:0]								00h	-			
P0	68h	1st	W	Set Transition Time	TT_STP[7:0]								00h	-
		ST_TIM[7:0]								00h	-			
P0	69h	1st	R	Get Transition Time	TT_STP[7:0]								00h	-
		ST_TIM[7:0]								00h	-			

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P0	A1h	1st	R	Read the DDB from the provided location	SID[7:0]								00h	1
		2nd			SID[15:8]								00h	1
		3rd			MRID[7:0]								00h	1
		4th			MRID[15:8]								00h	1
		5th			SID2[7:0]								00h	1
		6th			SID2[15:8]								00h	1
		7th			1	1	1	1	1	1	1	1	1	FFh
P0	A8h	1st	R	Continue reading the DDB from the last read location	D1[7:0]								00h	-
		2nd			D2[7:0]								00h	-
		:			:								00h	-
		nth			Dn[7:0]								00h	-
P0	AAh	1st	R	Read First Checksum	FCS[7:0]								00h	-
P0	AFh	1st	R	Read Continue Checksum	CCS[7:0]								00h	-
P0	DAh	1st	R	Read ID1	ID1[7:0]								00h	3
P0	DBh	1st	R	Read ID2	ID2[6:0]								00h	3
P0	DCh	1st	R	Read ID3	ID3[7:0]								00h	3
P0	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	1	81h	-	
		3rd	W		PAGE[7:0]								00h	-

Notes:

1. Undefined commands are treated as NOP (00h) command.
2. Commands 10h, 13h, 22h, 23h, 26h, 28h, 29h, 36h, 38h, 39h, 51h, 53h, 55h, 5Eh and 68h are updated during V-SYNC when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Commands 05h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh, 45h, 52h, 54h, 56h, 5Fh, 69h, A1h, A8h of these commands is updated immediately both in Sleep In mode and Sleep Out mode.

5.2.2. Page 1 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P1	00h	1st	R	Read ID4	ID4[23:16]							98h	-	
P1	01h	1st	R		ID4[15:8]							81h	-	
P1	02h	1st	R		ID4[7:0]							5Ch	-	
P1	22h	1st	W/R	Set Panel Operation Mode and Data Complement Setting	0	0	EPF[1:0]	BGR_PA NEL	REV_PA NEL	SS_PANE L	GS_PAN EL	30h	1	
P1	25h	1st	W/R	Blanking Porch Control	VFP[7:0]							14h	-	
P1	26h	1st	W/R		VBP[7:0]							14h	-	
P1	29h	1st	W/R	Touch	0	0	0	0	0	0	0	TOUCH_	00h	-
P1	2Eh	1st	W/R	Gate Number	NL[7:0]							C8h	1	
P1	31h	1st	W/R	Display Inversion	0	0	0	0	DINV[3:0]			00h	1	
P1	34h	1st	W/R	Dithering Enable	0	0	0	0	0	0	0	DITH_EN	00h	1
P1	40h	1st	W/R	Pump Clock Adjustment	0	EXT_CPCK_SEL[1:0]	1	0	0	1	VGHL_CLK	33h	1	
P1	42h	1st	W/R		0	VGHL_CLK_SELA[2:0]		0	VGHL_CLK_SELB[2:0]		44h	1		
P1	43h	1st	W/R		0	4002_RATIO_FREQA[2:0]		0	4002_RATIO_FREQB[2:0]		55h	1		
P1	50h	1st	W/R	Power Control 1	VREG1[7:0]							95h	1	
P1	51h	1st	W/R		VREG2[7:0]							95h	1	
P1	52h	1st	W/R	VCOM Control 1	0	0	0	0	0	0	0	VCM1[8]	00h	3
P1	53h	1st	W/R		VCM1[7:0]							7Bh	3	
P1	54h	1st	W/R		0	0	0	0	0	0	0	VCM2[8]	00h	3
P1	55h	1st	W/R		VCM2[7:0]							7Bh	3	
P1	56h	1st	W/R		0	0	0	NVM2	0	0	0	NVM1	00h	-
P1	58h	1st	W/R	Entry Mode Set	LVD_EN	0	0	0	0	0	0	0	00h	1
P1	60h	1st	W/R	Source Timing Adjust	0	0	SDT[5:0]				14h	1		
P1	61h	1st	W/R		0	0	CRT[5:0]				00h	1		
P1	62h	1st	W/R		0	0	EQT[5:0]				19h	1		
P1	63h	1st	W/R		0	0	PCT[5:0]				10h	1		
P1	A0h	1st	W/R	Positive Gamma Correction	0	0	VPO[5:0]				00h	2		
P1	A1h	1st	W/R		0	VP4[6:0]				0Dh	2			
P1	A2h	1st	W/R		0	VP8[6:0]				1Dh	2			
P1	A3h	1st	W/R		0	0	VP12[5:0]				11h	2		
P1	A4h	1st	W/R		0	0	VP16[5:0]				0Ch	2		
P1	A5h	1st	W/R		0	VP24[6:0]				23h	2			
P1	A6h	1st	W/R		0	0	VP36[5:0]				17h	2		
P1	A7h	1st	W/R		0	0	VP52[5:0]				1Ch	2		
P1	A8h	1st	W/R		VP80[7:0]				82h	2				
P1	A9h	1st	W/R		0	0	VP111[5:0]				21h	2		
P1	AAh	1st	W/R		0	0	VP144[5:0]				2Ah	2		
P1	ABh	1st	W/R		VP175[7:0]				6Bh	2				
P1	ACH	1st	W/R		0	0	VP203[5:0]				19h	2		
P1	ADh	1st	W/R		0	0	VP219[5:0]				14h	2		
P1	A Eh	1st	W/R		0	VP231[6:0]				45h	2			
P1	A Fh	1st	W/R		0	0	VP239[5:0]				1Dh	2		
P1	B0h	1st	W/R		0	0	VP243[5:0]				23h	2		
P1	B1h	1st	W/R		0	VP247[6:0]				52h	2			
P1	B2h	1st	W/R		0	VP251[6:0]				63h	2			
P1	B3h	1st	W/R		0	0	VP255[5:0]				39h	2		
P1	B6h	1st	W/R		Pad Control	IM_SW_EN	IM_SW[2:0]		RS_SW_EN	0	RS_SW[1:0]		00h	1
P1	B7h	1st	W/R			0	0	0	0	0	0	LANSEL_SW_EN	LANSEL_SW	00h

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P1	C0h	1st	W/R	Negative Gamma Correction	0	0	VN0[5:0]					00h	2	
P1	C1h	1st	W/R		0	VN4[6:0]					0Dh	2		
P1	C2h	1st	W/R		0	VN8[6:0]					1Dh	2		
P1	C3h	1st	W/R		0	0	VN12[5:0]					11h	2	
P1	C4h	1st	W/R		0	0	VN16[5:0]					0Ch	2	
P1	C5h	1st	W/R		0	VN24[6:0]					23h	2		
P1	C6h	1st	W/R		0	0	VN36[5:0]					17h	2	
P1	C7h	1st	W/R		0	0	VN52[5:0]					1Ch	2	
P1	C8h	1st	W/R		VN80[7:0]					82h	2			
P1	C9h	1st	W/R		0	0	VN111[5:0]					21h	2	
P1	CAh	1st	W/R		0	0	VN144[5:0]					2Ah	2	
P1	CBh	1st	W/R		VN175[7:0]					6Bh	2			
P1	CCh	1st	W/R		0	0	VN203[5:0]					19h	2	
P1	CDh	1st	W/R		0	0	VN219[5:0]					14h	2	
P1	CEh	1st	W/R		0	VN231[6:0]					45h	2		
P1	CFh	1st	W/R		0	0	VN239[5:0]					1Dh	2	
P1	D0h	1st	W/R		0	0	VN243[5:0]					23h	2	
P1	D1h	1st	W/R		0	VN247[6:0]					52h	2		
P1	D2h	1st	W/R		0	VN251[6:0]					63h	2		
P1	D3h	1st	W/R		0	0	VN255[5:0]					39h	2	
P1	E0h	1st	W/R		NV Memory Write	PGM_DATA[7:0]					00h	-		
P1	E1h	1st	W/R			PGM_ADR[7:0]					00h	-		
P1	E2h	1st	W/R			PGM_ADR[15:8]					00h	-		
P1	E3h	1st	W/R		NV Memory Protection Key	KEY[23:16]					00h	-		
P1	E4h	1st	W/R			KEY[15:8]					00h	-		
P1	E5h	1st	W/R			KEY[7:0]					00h	-		
P1	E6h	1st	R	NV Memory Status Read	0	ID2_MK[2:0]			0	ID1_MK[2:0]			00h	-
P1	E7h	1st	R		0	0	0	0	ID3_MK[2:0]			00h	-	
P1	E8h	1st	R		GAMMA_P_MK	GAMMA_N_MK	VCM2_MK[2:0]			VCM1_MK[2:0]			00h	-
P1	E9h	1st	R		OTP_BUSY	0	0	0	0	0	0	0	00h	-
P1	F0h	1st	W/R	Time Stamp	Time_Stamp_Week[7:0]							00h	1	
P1	F1h	1st	W/R		Time_Stamp_Year[7:0]							00h	1	
P1	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	0	1	81h	-
		3rd	W		PAGE[7:0]							01h	-	

5.2.3. Page 2 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P2	03h	1st	W/R	Dynamic Backlight Control 1	0	TT_STP_MED[2:0]		1	TT_STP_LOW[2:0]		29h		1	
P2	04h	1st	W/R		0	ST_TIM_LOW[2:0]		0	TT_STP_HIGH[2:0]		14h		1	
P2	05h	1st	W/R		0	ST_TIM_HIGH[2:0]		0	ST_TIM_MED[2:0]		32h		1	
P2	06h	1st	W/R	Dynamic Backlight Control 2	0	PWM_DUTY_PRECISION[2:0]		0	LEDPW_M_POL	LEDON_POL	LEDON		00h	1
P2	07h	1st	W/R		PWM_DIV[7:0]								0Eh	1
P2	10h	1st	W/R	IIE Function Control	0	0	0	0	0	PRT_EN	SKIN_EN	0	06h	1
P2	11h	1st	W/R		0	AUTO_MEAN	0	0	CN_EN	CN_INV	SHP_EN	0	00h	1
P2	12h	1st	W/R		0	0	0	0	0	0	CN_LV[1:0]		02h	1
P2	13h	1st	W/R		0	0	1	0	SRE_MIDIV_LV[1:0]		0	0	20h	1
P2	15h	1st	W/R		RGB_MEAN[7:0]								80h	1
P2	16h	1st	W/R		SRE_HYSTERESIS_EN	0	0	SRE_DIM_EN	SRE_SC_EN	SRE_CE_EN	0	0	1Ch	1
P2	17h	1st	W/R		0	SRE_OFFS[2:0]		0	SRE_DIM_STP[2:0]		01h		1	
P2	18h	1st	W/R		SRE_DIM_FRAME[7:0]								08h	1
P2	19h	1st	W/R		SRE_SC_GAIN_ADJ[2:0]				SRE_HYSTERESIS_LIMIT[4:0]				C0h	1
P2	1Ah	1st	W/R		IIE Saturation Enhancement Control 1				SE_RATIO_L[5:0]				07h	1
P2	1Bh	1st	W/R		0				SE_RATIO_M[5:0]				09h	1
P2	1Ch	1st	W/R	0				SE_RATIO_H[5:0]				0Ch	1	
P2	40h	1st	W/R	IIE Saturation Protection Control	0	0	0	LEVEL0_SR[4:0]				02h	1	
P2	41h	1st	W/R		0	0	0	LEVEL1_SR[4:0]				04h	1	
P2	42h	1st	W/R		0	0	0	LEVEL2_SR[4:0]				06h	1	
P2	43h	1st	W/R		0	0	0	LEVEL3_SR[4:0]				08h	1	
P2	44h	1st	W/R		0	0	0	LEVEL4_SR[4:0]				0Ah	1	
P2	45h	1st	W/R		0	0	0	LEVEL5_SR[4:0]				0Ch	1	
P2	46h	1st	W/R		0	0	0	LEVEL6_SR[4:0]				0Eh	1	
P2	47h	1st	W/R		0	0	0	LEVEL7_SR[4:0]				0Eh	1	
P2	48h	1st	W/R		0	0	0	LEVEL8_SR[4:0]				0Ch	1	
P2	49h	1st	W/R		0	0	0	LEVEL9_SR[4:0]				0Ah	1	
P2	4Ah	1st	W/R		0	0	0	LEVEL10_SR[4:0]				08h	1	
P2	4Bh	1st	W/R		0	0	0	LEVEL11_SR[4:0]				06h	1	
P2	4Ch	1st	W/R		0	0	0	LEVEL12_SR[4:0]				04h	1	
P2	4Dh	1st	W/R		0	0	0	LEVEL13_SR[4:0]				03h	1	
P2	4Eh	1st	W/R		0	0	0	LEVEL14_SR[4:0]				02h	1	
P2	4Fh	1st	W/R	0	0	0	LEVEL15_SR[4:0]				00h	1		
P2	5Ah	1st	W/R	IIE Sharpness Enhancement Control				SHP_RATIO[4:0]				18h	1	
P2	5Bh	1st	W/R	SHP_THR_H[7:0]								64h	1	
P2	5Ch	1st	W/R	SHP_THR_L[7:0]								1Eh	1	
P2	60h	1st	W/R	IIE Contrast Enhancement Control	0	0	CN_00[5:0]				0Eh		1	
P2	61h	1st	W/R		0	0	CN_01[5:0]				18h		1	
P2	62h	1st	W/R		0	0	CN_02[5:0]				24h		1	
P2	63h	1st	W/R		0	0	CN_03[5:0]				28h		1	
P2	64h	1st	W/R		0	0	CN_04[5:0]				24h		1	
P2	65h	1st	W/R		0	0	CN_05[5:0]				18h		1	
P2	66h	1st	W/R		0	0	CN_06[5:0]				0Eh		1	

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P2	D0	1st	W/R	IIE Auto White Balance 1	0	0	0	0	0	0	0	AWB_EN	00	1
P2	D1	1st	W/R	IIE Auto White Balance 2	0	0	R_AWB_1[9:8]		G_AWB_1[9:8]		B_AWB_1[9:8]		3Fh	2
P2	D2	1st	W/R		R_AWB_1[7:0]								FFh	2
P2	D3	1st	W/R		G_AWB_1[7:0]								FFh	2
P2	D4	1st	W/R		B_AWB_1[7:0]								FFh	2
P2	D5	1st	W/R	IIE Auto White Balance 3	0	0	R_AWB_2[9:8]		G_AWB_2[9:8]		B_AWB_2[9:8]		3Fh	2
P2	D6	1st	W/R		R_AWB_2[7:0]								FFh	2
P2	D7	1st	W/R		G_AWB_2[7:0]								FFh	2
P2	D8	1st	W/R		B_AWB_2[7:0]								FFh	2
P2	D9	1st	W/R	IIE Auto White Balance 4	0	0	R_AWB_3[9:8]		G_AWB_3[9:8]		B_AWB_3[9:8]		3Fh	2
P2	DA	1st	W/R		R_AWB_3[7:0]								FFh	2
P2	DB	1st	W/R		G_AWB_3[7:0]								FFh	2
P2	DC	1st	W/R		B_AWB_3[7:0]								FFh	2
P2	DD	1st	W/R	IIE Auto White Balance 5	0	0	R_AWB_4[9:8]		G_AWB_4[9:8]		B_AWB_4[9:8]		3Fh	2
P2	DE	1st	W/R		R_AWB_4[7:0]								FFh	2
P2	DF	1st	W/R		G_AWB_4[7:0]								FFh	2
P2	E0	1st	W/R		B_AWB_4[7:0]								FFh	2
P2	E1	1st	W/R	IIE Auto White Balance 6	0	0	R_AWB_5[9:8]		G_AWB_5[9:8]		B_AWB_5[9:8]		3Fh	2
P2	E2	1st	W/R		R_AWB_5[7:0]								FFh	2
P2	E3	1st	W/R		G_AWB_5[7:0]								FFh	2
P2	E4	1st	W/R		B_AWB_5[7:0]								FFh	2
P2	E5	1st	W/R	IIE Auto White Balance 7	0	0	R_AWB_6[9:8]		G_AWB_6[9:8]		B_AWB_6[9:8]		3Fh	2
P2	E6	1st	W/R		R_AWB_6[7:0]								FFh	2
P2	E7	1st	W/R		G_AWB_6[7:0]								FFh	2
P2	E8	1st	W/R		B_AWB_6[7:0]								FFh	2
P2	E9	1st	W/R	IIE Auto White Balance 8	0	0	R_AWB_7[9:8]		G_AWB_7[9:8]		B_AWB_7[9:8]		3Fh	2
P2	EA	1st	W/R		R_AWB_7[7:0]								FFh	2
P2	EB	1st	W/R		G_AWB_7[7:0]								FFh	2
P2	EC	1st	W/R		B_AWB_7[7:0]								FFh	2
P2	ED	1st	W/R	IIE Auto White Balance 9	Color_Temp_Adj[7:0]								60h	2
P2	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-
		2nd	W		1	0	0	0	0	0	0	1	81h	-
		3rd	W		PAGE[7:0]								02h	-

5.2.4. Page 3 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P3	01h	1st	W/R	GIP Setting 1	Reserve for other setting							-	1	
P3	02h	1st	W/R		Reserve for other setting							-	1	
P3	03h	1st	W/R		STV_A_Rise[9:8]	Phase_STV_A[1:0]	Overlap_STV_A[2:0]					-	1	
P3	04h	1st	W/R		STV_B_Rise[9:8]	Phase_STV_B[1:0]	Overlap_STV_B[2:0]					-	1	
P3	05h	1st	W/R		STV_C_Rise[9:8]	Phase_STV_C[1:0]	Overlap_STV_C[2:0]					-	1	
P3	06h	1st	W/R		STV_A_Rise[7:0]							-	1	
P3	07h	1st	W/R		STV_B_Rise[7:0]							-	1	
P3	08h	1st	W/R		STV_C_Rise[7:0]							-	1	
P3	09h	1st	W/R		FTI_1_Rise[7:0]							-	1	
P3	0Ah	1st	W/R		FTI_2_Rise[7:0]							-	1	
P3	0Bh	1st	W/R		FTI_3_Rise[7:0]							-	1	
P3	0Ch	1st	W/R		FTI_1_Fall[7:0]							-	1	
P3	0Dh	1st	W/R		FTI_2_Fall[7:0]							-	1	
P3	0Eh	1st	W/R		FTI_3_Fall[7:0]							-	1	
P3	0Fh	1st	W/R		CLW_1_Rise[7:0]							-	1	
P3	10h	1st	W/R		CLW_2_Rise[7:0]							-	1	
P3	11h	1st	W/R		Reserve for other setting							-	1	
P3	12h	1st	W/R		Reserve for other setting							-	1	
P3	13h	1st	W/R		CLW_X_Fall[7:0]							-	1	
P3	14h	1st	W/R		Reserve for other setting							-	1	
P3	15h	1st	W/R		GPM_R_Stage_i[7:0]							-	1	
P3	16h	1st	W/R		GPM_R_Stage_ii[7:0]							-	1	
P3	17h	1st	W/R		GPM_F_Stage_i[7:0]							-	1	
P3	18h	1st	W/R		GPM_F_Stage_ii[7:0]							-	1	
P3	19h	1st	W/R		Reserve for other setting							-	1	
P3	1Ah	1st	W/R		Reserve for other setting							-	1	
P3	1Bh	1st	W/R		Reserve for other setting							-	1	
P3	1Ch	1st	W/R		Reserve for other setting							-	1	
P3	1Dh	1st	W/R		Reserve for other setting							-	1	
P3	1Eh	1st	W/R		GS_ENA	CLK_A_Rise[10:8]		Reserve	CLK_A_Fall[10:8]				-	1
P3	1Fh	1st	W/R		Reserve	CLK_B_Rise[10:8]		Reserve	CLK_B_Fall[10:8]				-	1
P3	20h	1st	W/R		CLK_A_Rise[7:0]							-	1	
P3	21h	1st	W/R		CLK_A_Fall[7:0]							-	1	
P3	22h	1st	W/R		CLK_B_Rise[7:0]							-	1	
P3	23h	1st	W/R		Reserve for other setting							-	1	
P3	24h	1st	W/R		CLK_Keep_Pos1[7:0]							-	1	
P3	25h	1st	W/R		CLK_Keep_Pos2[7:0]							-	1	
P3	26h	1st	W/R		Reserve for other setting							-	1	
P3	27h	1st	W/R		Reserve for other setting							-	1	
P3	28h	1st	W/R		CLK_Disable	CLK_x_Numb[2:0]		CLK_Keep	Phase_CLK[2:0]				-	1
P3	29h	1st	W/R		Reserve for other setting			Overlap_CLK[3:0]				-	1	
P3	2Ah	1st	W/R		Reserve for other setting							-	1	
P3	2Bh	1st	W/R		Reserve for other setting							-	1	
P3	2Ch	1st	W/R		Reserve for other setting							-	1	
P3	2Dh	1st	W/R		Reserve for other setting							-	1	
P3	2Eh	1st	W/R		Reserve for other setting							-	1	
P3	2Fh	1st	W/R		Reserve for other setting							-	1	
P3	30h	1st	W/R		Reserve for other setting							-	1	
P3	31h	1st	W/R		Reserve for other setting							-	1	
P3	32h	1st	W/R		Reserve for other setting							-	1	
P3	33h	1st	W/R		Reserve for other setting							-	1	
P3	34h	1st	W/R		Reserve for other setting							-	1	
P3	35h	1st	W/R		Reserve for other setting							-	1	
P3	36h	1st	W/R		Reserve for other setting							-	1	
P3	37h	1st	W/R		Reserve for other setting							-	1	
P3	38h	1st	W/R		Reserve for other setting							-	1	
P3	39h	1st	W/R		Reserve for other setting							-	1	
P3	3Ah	1st	W/R		Reserve for other setting							-	1	
P3	3Bh	1st	W/R		Reserve for other setting							-	1	

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)				
Page	Address	Parameter																
P3	3Ch	1st	W/R	GIP Setting 1	Reserve for other setting								-	1				
P3	3Dh	1st	W/R		Reserve for other setting								-	1				
P3	3Eh	1st	W/R		Reserve for other setting								-	1				
P3	3Fh	1st	W/R		Reserve for other setting								-	1				
P3	40h	1st	W/R		Reserve for other setting								-	1				
P3	41h	1st	W/R		Reserve for other setting								-	1				
P3	42h	1st	W/R		Reserve for other setting								-	1				
P3	43h	1st	W/R		Reserve for other setting								-	1				
P3	44h	1st	W/R		Reserve for other setting								-	1				
P3	50h	1st	W/R		GIP Setting 2	STV_1_MUX[2:0]			STV_2_MUX[2:0]			STV_3_MUX[2:0]			STV_4_MUX[2:0]			-
P3	51h	1st	W/R	STV_5_MUX[2:0]			STV_6_MUX[2:0]			STV_7_MUX[2:0]			STV_8_MUX[2:0]			-	1	
P3	52h	1st	W/R	STV_9_MUX[2:0]			STV_10_MUX[2:0]			STV_11_MUX[2:0]			STV_12_MUX[2:0]			-	1	
P3	53h	1st	W/R	CLK_1_MUX[2:0]			CLK_2_MUX[2:0]			CLK_3_MUX[2:0]			CLK_4_MUX[2:0]			-	1	
P3	54h	1st	W/R	CLK_5_MUX[2:0]			CLK_6_MUX[2:0]			CLK_7_MUX[2:0]			CLK_8_MUX[2:0]			-	1	
P3	55h	1st	W/R	CLK_9_MUX[2:0]			CLK_10_MUX[2:0]			CLK_11_MUX[2:0]			CLK_12_MUX[2:0]			-	1	
P3	56h	1st	W/R	CLK_13_MUX[2:0]			CLK_14_MUX[2:0]			CLK_15_MUX[2:0]			CLK_16_MUX[2:0]			-	1	
P3	57h	1st	W/R	Reserve for other setting			BACKWA RDS	Reserve for other setting			FORWAR DS			-	1			
P3	5Eh	1st	W/R	0			GOUT_01_MUX_FW[4:0]						-	1				
P3	5Fh	1st	W/R	0			GOUT_02_MUX_FW[4:0]						-	1				
P3	60h	1st	W/R	0			GOUT_03_MUX_FW[4:0]						-	1				
P3	61h	1st	W/R	0			GOUT_04_MUX_FW[4:0]						-	1				
P3	62h	1st	W/R	0			GOUT_05_MUX_FW[4:0]						-	1				
P3	63h	1st	W/R	0			GOUT_06_MUX_FW[4:0]						-	1				
P3	64h	1st	W/R	0			GOUT_07_MUX_FW[4:0]						-	1				
P3	65h	1st	W/R	0			GOUT_08_MUX_FW[4:0]						-	1				
P3	66h	1st	W/R	0			GOUT_09_MUX_FW[4:0]						-	1				
P3	67h	1st	W/R	0			GOUT_10_MUX_FW[4:0]						-	1				
P3	68h	1st	W/R	0			GOUT_11_MUX_FW[4:0]						-	1				
P3	69h	1st	W/R	0			GOUT_12_MUX_FW[4:0]						-	1				
P3	6Ah	1st	W/R	0			GOUT_13_MUX_FW[4:0]						-	1				
P3	6Bh	1st	W/R	0			GOUT_14_MUX_FW[4:0]						-	1				
P3	6Ch	1st	W/R	0			GOUT_15_MUX_FW[4:0]						-	1				
P3	6Dh	1st	W/R	0			GOUT_16_MUX_FW[4:0]						-	1				
P3	6Eh	1st	W/R	0			GOUT_17_MUX_FW[4:0]						-	1				
P3	6Fh	1st	W/R	0			GOUT_18_MUX_FW[4:0]						-	1				
P3	70h	1st	W/R	0			GOUT_19_MUX_FW[4:0]						-	1				
P3	71h	1st	W/R	0			GOUT_20_MUX_FW[4:0]						-	1				
P3	72h	1st	W/R	0			GOUT_21_MUX_FW[4:0]						-	1				
P3	73h	1st	W/R	0			GOUT_22_MUX_FW[4:0]						-	1				
P3	74h	1st	W/R	0			GOUT_01_MUX_BW[4:0]						-	1				
P3	75h	1st	W/R	0			GOUT_02_MUX_BW[4:0]						-	1				
P3	76h	1st	W/R	0			GOUT_03_MUX_BW[4:0]						-	1				
P3	77h	1st	W/R	0			GOUT_04_MUX_BW[4:0]						-	1				
P3	78h	1st	W/R	0			GOUT_05_MUX_BW[4:0]						-	1				
P3	79h	1st	W/R	0			GOUT_06_MUX_BW[4:0]						-	1				
P3	7Ah	1st	W/R	0			GOUT_07_MUX_BW[4:0]						-	1				
P3	7Bh	1st	W/R	0			GOUT_08_MUX_BW[4:0]						-	1				
P3	7Ch	1st	W/R	0			GOUT_09_MUX_BW[4:0]						-	1				
P3	7Dh	1st	W/R	0			GOUT_10_MUX_BW[4:0]						-	1				
P3	7Eh	1st	W/R	0			GOUT_11_MUX_BW[4:0]						-	1				
P3	7Fh	1st	W/R	0			GOUT_12_MUX_BW[4:0]						-	1				
P3	80h	1st	W/R	0			GOUT_13_MUX_BW[4:0]						-	1				
P3	81h	1st	W/R	0			GOUT_14_MUX_BW[4:0]						-	1				
P3	82h	1st	W/R	0			GOUT_14_MUX_BW[4:0]						-	1				

Command				W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter													
P3	83h	1st	W/R	GIP Setting 3	0			GOUT_15_MUX_BW[4:0]				-	1		
P3	84h	1st	W/R		0			GOUT_16_MUX_BW[4:0]				-	1		
P3	85h	1st	W/R		0			GOUT_17_MUX_BW[4:0]				-	1		
P3	86h	1st	W/R		0			GOUT_18_MUX_BW[4:0]				-	1		
P3	87h	1st	W/R		0			GOUT_19_MUX_BW[4:0]				-	1		
P3	88h	1st	W/R		0			GOUT_20_MUX_BW[4:0]				-	1		
P3	89h	1st	W/R		0			GOUT_21_MUX_BW[4:0]				-	1		
P3	8Ah	1st	W/R		0			GOUT_22_MUX_BW[4:0]				-	1		
P3	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-	
		2nd	W		1	0	0	0	0	0	0	1	81h	-	
		3rd	W		PAGE[7:0]										03h

5.2.5. Page 4 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)	
Page	Address	Parameter													
P4	00h	1st	W/R	DSI Lanes Control	MIPI_LANE_SEL	0	0	0	0	0	0	0	80h	1	
P4	0Bh	1st	W/R	SSC Function	SSC_DIG_EN	SSC_DIG_STEP[2:0]			0	0	0	0	00h	-	
P4	0Eh	1st	W/R		SSC_DIG_CNT[7:0]									00h	-
P4	21h	1st	W/R	Charge-Pump Setting	DMY_PUMP	0	1	1	0	0	0	0	B0h	1	
P4	26h	1st	W/R	Internal SD Timing Control	DET_TOLERANCE_OP[3:0]			0	1	1	0	76h	1		
P4	27h	1st	W/R	Touch Synchronization Timing Adjust	TOUCH_OPT[1:0]	VSOD[1:0]		HSOM[1:0]		HFP_HP_OPT	VS_PW_OPT	00h	1		
P4	28h	1st	W/R		HSOD[7:0]									05h	1
P4	29h	1st	W/R		HSOHV[7:0]									19h	1
P4	2Ah	1st	W/R		VS_OUT_EN	HS_OUT_EN	VS_OUT_POL	HS_OUT_POL	0	0	STB_EN	0	F0h	1	
P4	2Dh	1st	W/R	BIST Mode Function	FRM_PT[7:0]									FFh	1
P4	2Fh	1st	W/R		0	0	FRM_CYC[1:0]	0	0	0	FRM_EN	00h	1		
P4	35h	1st	W/R	Source Timing Setting	0	0	0	1	HZ_OPT	1	1	1	17h	1	
P4	3Ah	1st	W/R	Power Saving Control	PS_EN	PCST[6:0]						A4h	1		
P4	69h	1st	W/R	Power Control 1	1	CP_VCL_CLP_OPTION_PRE[2:0]		0	1	1	1	D7h	-		
P4	6Eh	1st	W/R	Power Control 2	0	DI_PWR_REG	REG1_VRH_CP[5:0]					6Ah	1		
P4	6Fh	1st	W/R	Power Control 3	0	DI_CP_VGH_BH[2:0]		DI_CP_VGL_BL[2:0]		0	34h	1			
P4	7Ah	1st	W/R	VREG1/2 Setting	0	0	0	DI_REG_REG1_EN_CAP	0	0	0	00h	1		
P4	87h	1st	W/R	LVD Function 1	DI_LVD_CTL[3:0]			1	0	1	0	BAh	1		
P4	88h	1st	W/R	LVD Function 2	DIS_LVD_CHK	0	0	0	1	0	1	1	8Bh	1	
P4	8Bh	1st	W/R	VCOM Control 2	1	1	1	0	DI_VCM_SELO_E	0	1	1	E3h	1	
P4	8Dh	1st	W/R	Power Control 4	0	DI_VCOM_CP_VGLCLP[6:0]						14h	1		
P4	B2h	1st	W/R	Reload Gamma Setting	RELOAD_GMA_EN	RELOAD_GMA_L	0	1	0	0	0	1	D1h	1	
P4	B5h	1st	W/R	Gamma Bias Level	0	0	0	0	0	DI_GMA_GAP[2:0]		02h	1		
P4	BBh	1st	W/R	TS_CTRL 1	EN_TEMPL_PROC	0	CP_VGH_TAP_C[5:0]					1Eh	1		
P4	BCh	1st	W/R		0	0	CP_VGH_TAP_L[5:0]					1Eh	1		
P4	BDh	1st	W/R		0	0	CP_VGH_TAP_M[5:0]					1Eh	1		
P4	BEh	1st	W/R		0	0	CP_VGH_TAP_H[5:0]					1Eh	1		
P4	BFh	1st	W/R		VCOM_C[7:0]									4Ch	1
P4	C0h	1st	W/R		VCOM_L[7:0]									4Ch	1
P4	C1h	1st	W/R		VCOM_M[7:0]									4Ch	1
P4	C2h	1st	W/R		VCOM_H[7:0]									4Ch	1
P4	C4h	1st	R	Read VCOM OTP Data	0	0	0	0	0	0	0	0	OTP_VCM1[8]	00h	-
P4	C5h	1st	R		OTP_VCM1[7:0]									7Bh	-
P4	C6h	1st	R		0	0	0	0	0	0	0	0	OTP_VCM2[8]	00h	-
P4	C7h	1st	R		OTP_VCM2[7:0]									7Bh	-

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)	
Page	Address	Parameter													
P4	C8h	1st	W/R	TS_CTRL 2	TS_TH0[7:0]							00h	-		
P4	C9h	1st	W/R		TS_TH1[7:0]							00h	-		
P4	CAh	1st	W/R		TS_TH2[7:0]							00h	-		
P4	CBh	1st	W/R		TS_TH3[7:0]							00h	-		
P4	CCh	1st	W/R		TS_TH0[9:8]	TS_TH1[9:8]	TS_TH2[9:8]	TS_TH3[9:8]				00h	1		
P4	CDh	1st	W/R		TS_DEBT_OPT[3:0]			TS_HYST_OPT[3:0]						02h	1
P4	CEh	1st	W/R		EN_TS	VCOM_C [8]	VCOM_L [8]	VCOM_M [8]	VCOM_H [8]	1	0	0	04h	1	
P4	D7h	1st	W/R		OTP Control	0	0	0	OTP_PA TH	PROG_SEL[1:0]		0	0	1C	-
P4	FFh	1st	W	EXTC Command Set Enable Register	1	0	0	1	1	0	0	0	98h	-	
		2nd	W		1	0	0	0	0	0	0	1	81h	-	
		3rd	W		PAGE[7:0]									04h	-

5.2.6. Page 5 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)	
Page	Address	Parameter													
P5	00h	1st	W/R	Fine Digital Gamma Control 1	FineOffsetR00[5:0]						GRPR_OP0[9:8]		xxh	2	
P5	01h	1st	W/R		GRPR_OP0[7:0]									xxh	2
P5	02h	1st	W/R		FineOffsetR01[5:0]						GRPR_OP1[9:8]		xxh	2	
P5	03h	1st	W/R		GRPR_OP1[7:0]									xxh	2
P5	04h	1st	W/R		FineOffsetR02[5:0]						GRPR_OP2[9:8]		xxh	2	
P5	05h	1st	W/R		GRPR_OP1[7:0]									xxh	2
P5	06h	1st	W/R		FineOffsetR03[5:0]						GRPR_OP3[9:8]		xxh	2	
P5	07h	1st	W/R		GRPR_OP3[7:0]									xxh	2
P5	08h	1st	W/R		FineOffsetR04[5:0]						GRPR_OP4[9:8]		xxh	2	
P5	09h	1st	W/R		GRPR_OP4[7:0]									xxh	2
P5	:	1st	W/R		:									xxh	2
P5	:	1st	W/R		:									xxh	2
P5	38h	1st	W/R		FineOffsetR28[5:0]						GRPR_OP28[9:8]		xxh	2	
P5	39h	1st	W/R		GRPR_OP28[7:0]									xxh	2
P5	3Ah	1st	W/R		0	0	0	0	0	0	GRPR_OP29[9:8]		xxh	2	
P5	3Bh	1st	W/R		GRPR_OP29[7:0]									xxh	2
P5	3Ch	1st	W/R		0	0	0	0	0	0	GRPR_OP30[9:8]		xxh	2	
P5	3Dh	1st	W/R		GRPR_OP30[7:0]									xxh	2
P5	3Eh	1st	W/R		0	0	0	0	0	0	GRPR_OP31[9:8]		xxh	2	
P5	3Fh	1st	W/R		GRPR_OP31[7:0]									xxh	2
P5	:	1st	W/R		:									xxh	2
P5	:	1st	W/R		:									xxh	2
P5	5Ah	1st	W/R		0	0	0	0	0	0	GRPR_OP45[9:8]		xxh	2	
P5	5Bh	1st	W/R		GRPR_OP45[7:0]									xxh	2
P5	85h	1st	W/R		0	1	0	0	EN_3G	0	0	0	40h	1	
P5	FFh	1st	W		1	0	0	1	1	0	0	0	98h	-	
		2nd	W		1	0	0	0	0	0	0	1	81h	-	
		3rd	W		PAGE[7:0]									05h	-

5.2.7. Page 6 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)	
Page	Address	Parameter													
P6	00h	1st	W/R	Fine Digital Gamma Control 2	FineOffsetG00[5:0]					GRPG_OP0[9:8]			xxh	2	
P6	01h	1st	W/R		GRPG_OP0[7:0]								xxh	2	
P6	02h	1st	W/R		FineOffsetG01[5:0]					GRPG_OP1[9:8]			xxh	2	
P6	03h	1st	W/R		GRPG_OP1[7:0]								xxh	2	
P6	04h	1st	W/R		FineOffsetG02[5:0]					GRPG_OP2[9:8]			xxh	2	
P6	05h	1st	W/R		GRPG_OP1[7:0]								xxh	2	
P6	06h	1st	W/R		FineOffsetG03[5:0]					GRPG_OP3[9:8]			xxh	2	
P6	07h	1st	W/R		GRPG_OP3[7:0]								xxh	2	
P6	08h	1st	W/R		FineOffsetG04[5:0]					GRPG_OP4[9:8]			xxh	2	
P6	09h	1st	W/R		GRPG_OP4[7:0]								xxh	2	
P6	:	1st	W/R		:								xxh	2	
P6	:	1st	W/R		:								xxh	2	
P6	38h	1st	W/R		FineOffsetG28[5:0]					GRPG_OP28[9:8]			xxh	2	
P6	39h	1st	W/R		GRPG_OP28[7:0]								xxh	2	
P6	3Ah	1st	W/R		0	0	0	0	0	0	GRPG_OP29[9:8]			xxh	2
P6	3Bh	1st	W/R		GRPG_OP29[7:0]								xxh	2	
P6	3Ch	1st	W/R		0	0	0	0	0	GRPG_OP30[9:8]			xxh	2	
P6	3Dh	1st	W/R		GRPG_OP30[7:0]								xxh	2	
P6	3Eh	1st	W/R		0	0	0	0	0	0	GRPG_OP31[9:8]			xxh	2
P6	3Fh	1st	W/R		GRPG_OP31[7:0]								xxh	2	
P6	:	1st	W/R		:								xxh	2	
P6	:	1st	W/R		:								xxh	2	
P6	5Ah	1st	W/R		0	0	0	0	0	0	GRPG_OP45[9:8]			xxh	2
P6	5Bh	1st	W/R		GRPG_OP45[7:0]								xxh	2	
P6	FFh	1st	W	EXTC Command Set	1	0	0	1	1	0	0	0	98h	-	
		2nd	W	Enable Register	1	0	0	0	0	0	0	1	81h	-	
		3rd	W		PAGE[7:0]								06h	-	

5.2.8. Page 7 Command Set

Command			W/R	Function	D7	D6	D5	D4	D3	D2	D1	D0	Default (hex)	MTP (times)
Page	Address	Parameter												
P7	00h	1st	W/R	Fine Digital Gamma Control 3	FineOffsetB00[5:0]						GRP_B_OP0[9:8]		xxh	2
P7	01h	1st	W/R		GRP_B_OP0[7:0]								xxh	2
P7	02h	1st	W/R		FineOffsetB01[5:0]						GRP_B_OP1[9:8]		xxh	2
P7	03h	1st	W/R		GRP_B_OP1[7:0]								xxh	2
P7	04h	1st	W/R		FineOffsetB02[5:0]						GRP_B_OP2[9:8]		xxh	2
P7	05h	1st	W/R		GRP_B_OP2[7:0]								xxh	2
P7	06h	1st	W/R		FineOffsetB03[5:0]						GRP_B_OP3[9:8]		xxh	2
P7	07h	1st	W/R		GRP_B_OP3[7:0]								xxh	2
P7	08h	1st	W/R		FineOffsetB04[5:0]						GRP_B_OP4[9:8]		xxh	2
P7	09h	1st	W/R		GRP_B_OP4[7:0]								xxh	2
P7	:	1st	W/R										xxh	2
P7	:	1st	W/R										xxh	2
P7	38h	1st	W/R		FineOffsetB28[5:0]						GRP_B_OP28[9:8]		xxh	2
P7	39h	1st	W/R		GRP_B_OP28[7:0]								xxh	2
P7	3Ah	1st	W/R		0	0	0	0	0	0	GRP_B_OP29[9:8]		xxh	2
P7	3Bh	1st	W/R		GRP_B_OP29[7:0]								xxh	2
P7	3Ch	1st	W/R		0	0	0	0	0	GRP_B_OP30[9:8]		xxh	2	
P7	3Dh	1st	W/R		GRP_B_OP30[7:0]								xxh	2
P7	3Eh	1st	W/R		0	0	0	0	0	GRP_B_OP31[9:8]		xxh	2	
P7	3Fh	1st	W/R		GRP_B_OP31[7:0]								xxh	2
P7	:	1st	W/R										xxh	2
P7	:	1st	W/R										xxh	2
P7	5Ah	1st	W/R		0	0	0	0	0	GRP_B_OP45[9:8]		xxh	2	
P7	5Bh	1st	W/R		GRP_B_OP45[7:0]								xxh	2
P7	FFh	1st	W	1	0	0	1	1	0	0	0	0	98h	-
		2nd	W	1	0	0	0	0	0	0	1	81h	-	
		3rd	W	PAGE[7:0]										07h

5.3. Page 0 Command Description

5.3.1. NOP (00h)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
00h	-	W	No Argument								-								
Description	<p>00h: NOP (No Operation).</p> <p>This command is an empty command. It does not have any effect on the ILI9881C-04.</p> <p>However, it can be used to terminate Memory Write or Memory Write Continue as described in RAMWR (Memory Write) and RAMWRC (Memory Write Continue) Commands.</p>																		
Restriction	None																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>S/W Reset</td> <td>N/A</td> </tr> <tr> <td>H/W Reset</td> <td>N/A</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A
Status	Default Value																		
Power On Sequence	N/A																		
S/W Reset	N/A																		
H/W Reset	N/A																		
Flow Chart																			

5.3.2. Software Reset (01h)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
01h	-	W	No Argument									-							
Description	<p>01h: SWRESET (Software Reset).</p> <p>When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)</p> <p>The display is blank immediately.</p> <p><i>Note: The Frame Memory content is kept or not by this command</i></p>																		
Restriction	<p>It is necessary to wait 5msec before sending a new command after software reset. The display module loads all factory default values of the display supplier to the registers during this 5msec. If Software Reset is applied during the Sleep Out mode, it will be necessary to wait 120msec for Sleep In sequence before sending the Sleep Out command.</p> <p>The Software Reset Command cannot be sent during the Sleep Out sequence.</p>																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>S/W Reset</td> <td>N/A</td> </tr> <tr> <td>H/W Reset</td> <td>N/A</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	N/A	S/W Reset	N/A	H/W Reset	N/A
Status	Default Value																		
Power On Sequence	N/A																		
S/W Reset	N/A																		
H/W Reset	N/A																		
Flow Chart	<pre> graph TD A[SWRESET] --> B{{Display whole blank screen}} B --> C{{Set Commands to S/W Default Value}} C --> D([Sleep In Mode]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Hexagon Action: Pentagon Mode: Rounded Rectangle Sequential transfer: Oval with tail 																		

5.3.3. Read Number of the Errors on DSI (05h)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
05h	1st	R	P[7:0]									00h							
Description	<p>05h: RDNUMED (Read Number of the Errors on DSI).</p> <p>The parameter indicates the amount of errors on the DSI. The more detailed description of the bits is below.</p> <p>P[6..0] bits indicate the amount of the error.</p> <p>P[7] is set to 1 if there is overflow with P[6..0] bits.</p> <p>P[7..0] bits are set to 0 (and RDDSM (0Eh)'s D0 is set 0 at the same time) after the parameter information is sent (= the read function is completed).</p> <p>See also sections: "4.1.3.2.2 Acknowledge with Error Report (AwER)" and "5.3.9 Read Display Signal Mode (0Eh)".</p>																		
Restriction	None																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes																		
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Status	Default Value																		
Power On Sequence	00h																		
S/W Reset	00h																		
H/W Reset	00h																		
Flow Chart	<pre> graph TD A[Read Number of the Corrupted Errors] -- Host --> B{P[7..0] = 00h RDDSM(0Eh)'s D0 = '0''} B --- C[Display] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Oval Action: Arrow Mode: Circle Sequential transfer: Circle with tail 																		

5.3.4. Read Display Status (09h)

Command Page			Page 0																																																																																																								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																																																																																
09h	1st	R	D31	0	0	0	0	D26	0	D24	00h																																																																																																
	2nd	R	D23	0	0	0	D19	0	D17	D16	01h																																																																																																
	3rd	R	0	0	0	D12	D11	D10	D9	D8	00h																																																																																																
	4th	R	D7	D6	D5	0	0	0	0	D0	00h																																																																																																
Description	This command indicates the current status of the display, as described in the table below:																																																																																																										
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Value</th> <th>Status</th> </tr> </thead> <tbody> <tr> <td rowspan="2">D31</td> <td rowspan="2">Booster voltage status</td> <td>0</td> <td>Booster Off</td> </tr> <tr> <td>1</td> <td>Booster On</td> </tr> <tr> <td rowspan="2">D26</td> <td rowspan="2">RGB/BGR order</td> <td>0</td> <td>RGB (When MADCTL D3 = 0)</td> </tr> <tr> <td>1</td> <td>BGR (When MADCTL D3= 1)</td> </tr> <tr> <td rowspan="2">D24</td> <td rowspan="2">Source scan sequence</td> <td>0</td> <td>Source output Left to Right (When MADCTL D1 = 0)</td> </tr> <tr> <td>1</td> <td>Source output Right to Left (When MADCTL D1 = 1)</td> </tr> <tr> <td rowspan="2">D23</td> <td rowspan="2">Gate scan sequence</td> <td>0</td> <td>Gate output Top to Bottom (When MADCTL D0 = 0)</td> </tr> <tr> <td>1</td> <td>Gate output Bottom to Top (When MADCTL D0 = 1)</td> </tr> <tr> <td rowspan="2">D19</td> <td rowspan="2">Idle Mode On/Off</td> <td>0</td> <td>Idle Mode Off</td> </tr> <tr> <td>1</td> <td>Idle Mode On</td> </tr> <tr> <td rowspan="2">D17</td> <td rowspan="2">Sleep In/Out</td> <td>0</td> <td>Sleep In Mode</td> </tr> <tr> <td>1</td> <td>Sleep Out Mode</td> </tr> <tr> <td rowspan="2">D16</td> <td rowspan="2">Display Normal Mode On/Off</td> <td>0</td> <td>Display Normal Mode Off (All Pixels Off or All Pixels On mode)</td> </tr> <tr> <td>1</td> <td>Display Normal Mode On</td> </tr> <tr> <td rowspan="2">D13</td> <td rowspan="2">Inversion status</td> <td>0</td> <td>Inversion Off</td> </tr> <tr> <td>1</td> <td>Inversion On</td> </tr> <tr> <td rowspan="2">D12</td> <td rowspan="2">All Pixel On</td> <td>0</td> <td>Normal mode</td> </tr> <tr> <td>1</td> <td>All Pixels On</td> </tr> <tr> <td rowspan="2">D11</td> <td rowspan="2">All Pixel Off</td> <td>0</td> <td>Normal mode</td> </tr> <tr> <td>1</td> <td>All Pixels Off</td> </tr> <tr> <td rowspan="2">D10</td> <td rowspan="2">Display ON/OFF</td> <td>0</td> <td>Display is OFF</td> </tr> <tr> <td>1</td> <td>Display is ON</td> </tr> <tr> <td rowspan="2">D9</td> <td rowspan="2">TE ON/OFF</td> <td>0</td> <td>TE OFF</td> </tr> <tr> <td>1</td> <td>TE ON</td> </tr> <tr> <td>D8</td> <td rowspan="3">Gamma Curve Selection [2:0]</td> <td>000</td> <td>Gamma Curve 1</td> </tr> <tr> <td>D7</td> <td rowspan="2">others</td> <td rowspan="2">Not defined</td> </tr> <tr> <td>D6</td> </tr> <tr> <td rowspan="2">D5</td> <td rowspan="2">TE Mode</td> <td>0</td> <td>TE Mode 1</td> </tr> <tr> <td>1</td> <td>TE Mode 2</td> </tr> <tr> <td rowspan="2">D0</td> <td rowspan="2">Parity Error on DSI</td> <td>0</td> <td>No Parity Error</td> </tr> <tr> <td>1</td> <td>Parity Error</td> </tr> </tbody> </table>											Bit	Description	Value	Status	D31	Booster voltage status	0	Booster Off	1	Booster On	D26	RGB/BGR order	0	RGB (When MADCTL D3 = 0)	1	BGR (When MADCTL D3= 1)	D24	Source scan sequence	0	Source output Left to Right (When MADCTL D1 = 0)	1	Source output Right to Left (When MADCTL D1 = 1)	D23	Gate scan sequence	0	Gate output Top to Bottom (When MADCTL D0 = 0)	1	Gate output Bottom to Top (When MADCTL D0 = 1)	D19	Idle Mode On/Off	0	Idle Mode Off	1	Idle Mode On	D17	Sleep In/Out	0	Sleep In Mode	1	Sleep Out Mode	D16	Display Normal Mode On/Off	0	Display Normal Mode Off (All Pixels Off or All Pixels On mode)	1	Display Normal Mode On	D13	Inversion status	0	Inversion Off	1	Inversion On	D12	All Pixel On	0	Normal mode	1	All Pixels On	D11	All Pixel Off	0	Normal mode	1	All Pixels Off	D10	Display ON/OFF	0	Display is OFF	1	Display is ON	D9	TE ON/OFF	0	TE OFF	1	TE ON	D8	Gamma Curve Selection [2:0]	000	Gamma Curve 1	D7	others	Not defined	D6	D5	TE Mode	0	TE Mode 1	1	TE Mode 2	D0	Parity Error on DSI	0	No Parity Error	1	Parity Error
	Bit	Description	Value	Status																																																																																																							
	D31	Booster voltage status	0	Booster Off																																																																																																							
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	D26	RGB/BGR order	0	RGB (When MADCTL D3 = 0)																																																																																																							
			1	BGR (When MADCTL D3= 1)																																																																																																							
	D24	Source scan sequence	0	Source output Left to Right (When MADCTL D1 = 0)																																																																																																							
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	D16	Display Normal Mode On/Off	0	Display Normal Mode Off (All Pixels Off or All Pixels On mode)																																																																																																							
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	D9	TE ON/OFF	0	TE OFF																																																																																																							
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D8	Gamma Curve Selection [2:0]	000	Gamma Curve 1																																																																																																								
D7		others	Not defined																																																																																																								
D6																																																																																																											
D5	TE Mode	0	TE Mode 1																																																																																																								
		1	TE Mode 2																																																																																																								
D0	Parity Error on DSI	0	No Parity Error																																																																																																								
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Restriction	None																																																																																																										

<p>Register Availability</p>	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability								
Normal Mode On, Idle Mode Off, Sleep Out	Yes								
Normal Mode On, Idle Mode On, Sleep Out	Yes								
Sleep In	Yes								
<p>Default</p>	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h_01h_00h_00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h_01h_00h_00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h_01h_00h_00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h_01h_00h_00h	S/W Reset	00h_01h_00h_00h	H/W Reset	00h_01h_00h_00h
Status	Default Value								
Power On Sequence	00h_01h_00h_00h								
S/W Reset	00h_01h_00h_00h								
H/W Reset	00h_01h_00h_00h								

5.3.5. Read Display Power Mode (0Ah)

Command Page		Page 0																																										
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																	
0Ah	1st	R	D7	D6	0	D4	D3	D2	0	0	08h																																	
Description	0A: RDDPM (Read Display Power Mode). This command indicates the current status of the display, as described in the table below.																																											
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Value</th> <th>Status</th> </tr> </thead> <tbody> <tr> <td rowspan="2">D7</td> <td rowspan="2">Booster Voltage Status</td> <td>0</td> <td>Booster Off or has a fault.</td> </tr> <tr> <td>1</td> <td>Booster On and working OK</td> </tr> <tr> <td rowspan="2">D6</td> <td rowspan="2">Idle Mode On/Off</td> <td>0</td> <td>Idle Mode Off</td> </tr> <tr> <td>1</td> <td>Idle Mode On</td> </tr> <tr> <td rowspan="2">D4</td> <td rowspan="2">Sleep In/Out</td> <td>0</td> <td>Sleep In Mode</td> </tr> <tr> <td>1</td> <td>Sleep Out Mode</td> </tr> <tr> <td rowspan="2">D3</td> <td rowspan="2">Display Normal Mode On/Off</td> <td>0</td> <td>Display Normal Mode Off</td> </tr> <tr> <td>1</td> <td>Display Normal Mode On</td> </tr> <tr> <td rowspan="2">D2</td> <td rowspan="2">Display On/Off</td> <td>0</td> <td>Display is Off</td> </tr> <tr> <td>1</td> <td>Display is On</td> </tr> </tbody> </table>											Bit	Description	Value	Status	D7	Booster Voltage Status	0	Booster Off or has a fault.	1	Booster On and working OK	D6	Idle Mode On/Off	0	Idle Mode Off	1	Idle Mode On	D4	Sleep In/Out	0	Sleep In Mode	1	Sleep Out Mode	D3	Display Normal Mode On/Off	0	Display Normal Mode Off	1	Display Normal Mode On	D2	Display On/Off	0	Display is Off	1
Bit	Description	Value	Status																																									
D7	Booster Voltage Status	0	Booster Off or has a fault.																																									
		1	Booster On and working OK																																									
D6	Idle Mode On/Off	0	Idle Mode Off																																									
		1	Idle Mode On																																									
D4	Sleep In/Out	0	Sleep In Mode																																									
		1	Sleep Out Mode																																									
D3	Display Normal Mode On/Off	0	Display Normal Mode Off																																									
		1	Display Normal Mode On																																									
D2	Display On/Off	0	Display is Off																																									
		1	Display is On																																									
Restriction	None																																											
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																									
Status	Availability																																											
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Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>08h</td> </tr> <tr> <td>S/W Reset</td> <td>08h</td> </tr> <tr> <td>H/W Reset</td> <td>08h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	08h	S/W Reset	08h	H/W Reset	08h																									
Status	Default Value																																											
Power On Sequence	08h																																											
S/W Reset	08h																																											
H/W Reset	08h																																											
Flow Chart	<pre> graph TD subgraph Host C[Read RDDPM] end subgraph Display P[/Send Parameter/] end C --> P </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Hexagon Action: Arrow Mode: Oval Sequential transfer: Oval with tail 																																											

5.3.6. Read Display MADCTL (0Bh)

Command Page		Page 0																														
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																					
0Bh	1st	R	0	0	0	0	D3	0	D1	D0	00h																					
Description	0B: RDDMADCTL (Read Display MADCTL). This command indicates the current status of the display, as described in the table below.																															
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Value</th> <th>Status</th> </tr> </thead> <tbody> <tr> <td rowspan="2">D3</td> <td rowspan="2">RGB/BGR Order (RGB)</td> <td>0</td> <td>RGB (When MADCTL D3='0')</td> </tr> <tr> <td>1</td> <td>BGR (When MADCTL D3='1')</td> </tr> <tr> <td rowspan="2">D1</td> <td rowspan="2">Source scan sequence (SS)</td> <td>0</td> <td>Source output Left to Right (When MADCTL D1 = '0')</td> </tr> <tr> <td>1</td> <td>Source output Right to Left (When MADCTL D1 = '1')</td> </tr> <tr> <td rowspan="2">D0</td> <td rowspan="2">Gate scan sequence (GS)</td> <td>0</td> <td>Gate output Top to Bottom (When MADCTL D0 = '0')</td> </tr> <tr> <td>1</td> <td>Gate output Bottom to Top (When MADCTL D0 = '1')</td> </tr> </tbody> </table> <p><i>Note: For Bits D3, D1 and D0 also refer to 5.3.21Memory Access Control (36h).</i></p>											Bit	Description	Value	Status	D3	RGB/BGR Order (RGB)	0	RGB (When MADCTL D3='0')	1	BGR (When MADCTL D3='1')	D1	Source scan sequence (SS)	0	Source output Left to Right (When MADCTL D1 = '0')	1	Source output Right to Left (When MADCTL D1 = '1')	D0	Gate scan sequence (GS)	0	Gate output Top to Bottom (When MADCTL D0 = '0')	1
Bit	Description	Value	Status																													
D3	RGB/BGR Order (RGB)	0	RGB (When MADCTL D3='0')																													
		1	BGR (When MADCTL D3='1')																													
D1	Source scan sequence (SS)	0	Source output Left to Right (When MADCTL D1 = '0')																													
		1	Source output Right to Left (When MADCTL D1 = '1')																													
D0	Gate scan sequence (GS)	0	Gate output Top to Bottom (When MADCTL D0 = '0')																													
		1	Gate output Bottom to Top (When MADCTL D0 = '1')																													
Restriction	None																															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes													
Status	Availability																															
Normal Mode On, Idle Mode Off, Sleep Out	Yes																															
Normal Mode On, Idle Mode On, Sleep Out	Yes																															
Sleep In	Yes																															
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h													
Status	Default Value																															
Power On Sequence	00h																															
S/W Reset	00h																															
H/W Reset	00h																															
Flow Chart																																

5.3.7. Read Display Pixel Format (0Ch)

Command Page		Page 0																		
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default									
0Ch	1st	R	0	0	0	0	0	D[2:0]			07h									
Description	0Ch: RDDCOLMOD (Read Display COLMOD). This command indicates the current status of the display as described in the table below:																			
	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>DBI[2:0]</th> <th>Interface Pixel Format</th> </tr> </thead> <tbody> <tr> <td>101</td> <td>16 bit/pixel</td> </tr> <tr> <td>110</td> <td>18 bit/pixel</td> </tr> <tr> <td>111</td> <td>24 bit/pixel</td> </tr> <tr> <td>Others</td> <td>Not defined</td> </tr> </tbody> </table> <p><i>Note: For D[2:0] also refer to 5.3.24 Interface Pixel Format (3Ah).</i></p>											DBI[2:0]	Interface Pixel Format	101	16 bit/pixel	110	18 bit/pixel	111	24 bit/pixel	Others
DBI[2:0]	Interface Pixel Format																			
101	16 bit/pixel																			
110	18 bit/pixel																			
111	24 bit/pixel																			
Others	Not defined																			
Restriction	None																			
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability																			
Normal Mode On, Idle Mode Off, Sleep Out	Yes																			
Normal Mode On, Idle Mode On, Sleep Out	Yes																			
Sleep In	Yes																			
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>07h</td> </tr> <tr> <td>S/W Reset</td> <td>07h</td> </tr> <tr> <td>H/W Reset</td> <td>07h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	07h	S/W Reset	07h	H/W Reset	07h	
Status	Default Value																			
Power On Sequence	07h																			
S/W Reset	07h																			
H/W Reset	07h																			
Flow Chart	<div style="display: flex; align-items: center; justify-content: center;"> <div style="text-align: center; margin-right: 20px;"> <div style="border: 1px solid black; padding: 2px 10px; display: inline-block;">Read RDDCOLMOD</div> ↓ <div style="border: 1px solid black; padding: 2px 10px; display: inline-block;">Send Parameter</div> </div> <div style="text-align: center; margin-left: 20px;"> Host ----- Display </div> </div> <div style="margin-left: 20px;"> <div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <div style="border: 1px solid black; padding: 2px; display: inline-block; width: 50px; height: 15px; margin-bottom: 5px;"></div> Command <div style="border: 1px solid black; padding: 2px; display: inline-block; width: 50px; height: 15px; transform: rotate(-15deg); margin-bottom: 5px;"></div> Parameter <div style="border: 1px solid black; padding: 2px; display: inline-block; width: 50px; height: 15px; border-radius: 5px; margin-bottom: 5px;"></div> Display <div style="border: 1px solid black; padding: 2px; display: inline-block; width: 50px; height: 15px; border-radius: 5px; margin-bottom: 5px;"></div> Action <div style="border: 1px solid black; padding: 2px; display: inline-block; width: 50px; height: 15px; border-radius: 5px; margin-bottom: 5px;"></div> Mode <div style="border: 1px solid black; padding: 2px; display: inline-block; width: 50px; height: 15px; border-radius: 5px; margin-bottom: 5px;"></div> Sequential transfer </div> </div>																			

5.3.8. Read Display Image Mode (0Dh)

Command Page		Page 0																															
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																						
0Dh	1st	R	0	0	0	D4	D3	D[2:0]			00h																						
Description	<p>0D: RDDIM (Read Display Image Mode).</p> <p>This command indicates the Image Mode status of the display, as described in the Tables below:</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Value</th> <th>Status</th> </tr> </thead> <tbody> <tr> <td rowspan="2">D4</td> <td rowspan="2">All Pixels On</td> <td>0</td> <td>Normal Display</td> </tr> <tr> <td>1</td> <td>White Display</td> </tr> <tr> <td rowspan="2">D3</td> <td rowspan="2">All Pixels Off</td> <td>0</td> <td>Normal Display</td> </tr> <tr> <td>1</td> <td>Black Display</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th>D[2:0]</th> <th>Gamma Cure Selection</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>Gamma curve 1</td> </tr> <tr> <td>Others</td> <td>Not defined</td> </tr> </tbody> </table> <p><i>Note: For D[2:0] also refer to "5.3.16 Gamma Set (26h)"</i></p>											Bit	Description	Value	Status	D4	All Pixels On	0	Normal Display	1	White Display	D3	All Pixels Off	0	Normal Display	1	Black Display	D[2:0]	Gamma Cure Selection	000	Gamma curve 1	Others	Not defined
	Bit	Description	Value	Status																													
	D4	All Pixels On	0	Normal Display																													
1			White Display																														
D3	All Pixels Off	0	Normal Display																														
		1	Black Display																														
D[2:0]	Gamma Cure Selection																																
000	Gamma curve 1																																
Others	Not defined																																
Restriction	None																																
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes														
	Status	Availability																															
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																
Normal Mode On, Idle Mode On, Sleep Out	Yes																																
Sleep In	Yes																																
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h														
	Status	Default Value																															
Power On Sequence	00h																																
S/W Reset	00h																																
H/W Reset	00h																																
Flow Chart	<pre> sequenceDiagram participant Host participant Display Host->>Display: Read RDDIM Display-->Host: Send Parameter </pre>																																

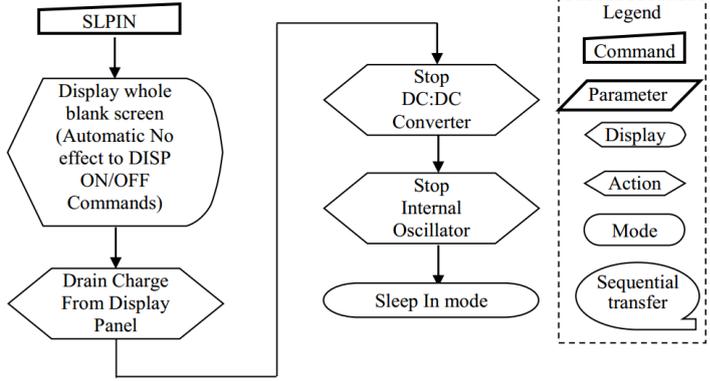
5.3.9. Read Display Signal Mode (0Eh)

Command Page		Page 0																																			
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																										
0Eh	1st	R	D7	D6	0	0	0	0	0	D0	00h																										
Description	<p>0E: RDDSM (Read Display Signal Mode).</p> <p>This command indicates the current status of the display, as described in the table below:</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Value</th> <th>Status</th> </tr> </thead> <tbody> <tr> <td rowspan="2">D7</td> <td rowspan="2">Tearing Effect Line On/Off</td> <td>0</td> <td>Tearing Effect Line Off</td> </tr> <tr> <td>1</td> <td>Tearing Effect On</td> </tr> <tr> <td rowspan="2">D6</td> <td rowspan="2">Tearing Effect Line Output Mode</td> <td>0</td> <td>Tearing Effect Line Mode 1</td> </tr> <tr> <td>1</td> <td>Tearing Effect Line Mode 2</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Value</th> <th>Status</th> </tr> </thead> <tbody> <tr> <td rowspan="2">D0</td> <td rowspan="2">Error on DSI</td> <td>0</td> <td>No Error on DSI</td> </tr> <tr> <td>1</td> <td>Error on DSI</td> </tr> </tbody> </table> <p>See also sections: "4.1.3.2.2 Acknowledge with Error Report (AwER)" and "5.3.3 Read Number of the Errors on DSI (05h)".</p> <p><i>Note: For Bit D6, also refer to 5.3.20 Tearing Effect Line On (35h).</i></p>											Bit	Description	Value	Status	D7	Tearing Effect Line On/Off	0	Tearing Effect Line Off	1	Tearing Effect On	D6	Tearing Effect Line Output Mode	0	Tearing Effect Line Mode 1	1	Tearing Effect Line Mode 2	Bit	Description	Value	Status	D0	Error on DSI	0	No Error on DSI	1	Error on DSI
	Bit	Description	Value	Status																																	
	D7	Tearing Effect Line On/Off	0	Tearing Effect Line Off																																	
1			Tearing Effect On																																		
D6	Tearing Effect Line Output Mode	0	Tearing Effect Line Mode 1																																		
		1	Tearing Effect Line Mode 2																																		
Bit	Description	Value	Status																																		
D0	Error on DSI	0	No Error on DSI																																		
		1	Error on DSI																																		
Restriction	None																																				
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																		
Status	Availability																																				
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																				
Normal Mode On, Idle Mode On, Sleep Out	Yes																																				
Sleep In	Yes																																				
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h																		
Status	Default Value																																				
Power On Sequence	00h																																				
S/W Reset	00h																																				
H/W Reset	00h																																				
Flow Chart	<pre> graph TD subgraph Host C[Read RDDSM] end subgraph Display P[/Send Parameter/] end C --> P </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Oval Action: Arrow Mode: Rounded Rectangle Sequential transfer: Oval with arrow 																																				

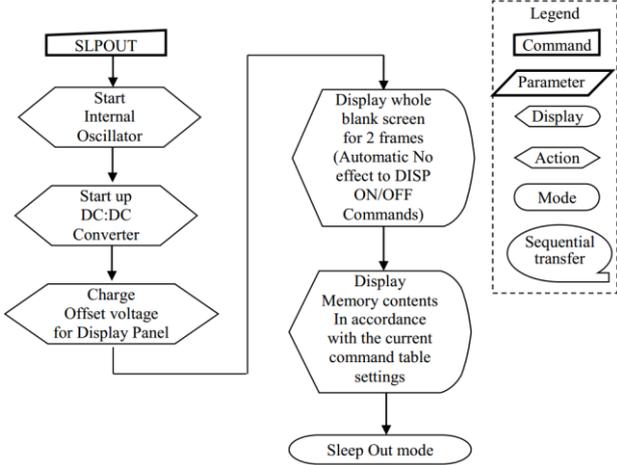
5.3.10. Read Display Self-Diagnostic Result (0Fh)

Command Page		Page 0																					
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
0Fh	1st	R	D7	D6	0	0	0	0	0	D0	00h												
Description	<p>0F: RDDSDR (Read Display Self-Diagnostic Result).</p> <p>This command indicates the status of the display self-diagnostic results after the Sleep Out command, as described in the table below:</p> <table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Action</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>Register Loading Detection</td> <td>Invert the D7 bit when the EEPROM and register values are the same.</td> </tr> <tr> <td>D6</td> <td>Functionality Detection</td> <td>Invert the D6 bit when the chip meets user's functionality requirements.</td> </tr> <tr> <td>D0</td> <td>Checksums Comparison</td> <td>0 = Checksums are the same 1 = Checksums are not the same</td> </tr> </tbody> </table>											Bit	Description	Action	D7	Register Loading Detection	Invert the D7 bit when the EEPROM and register values are the same.	D6	Functionality Detection	Invert the D6 bit when the chip meets user's functionality requirements.	D0	Checksums Comparison	0 = Checksums are the same 1 = Checksums are not the same
	Bit	Description	Action																				
D7	Register Loading Detection	Invert the D7 bit when the EEPROM and register values are the same.																					
D6	Functionality Detection	Invert the D6 bit when the chip meets user's functionality requirements.																					
D0	Checksums Comparison	0 = Checksums are the same 1 = Checksums are not the same																					
Restriction	It will be necessary to wait 300ms after there is the last write access on Page 0 area registers before there can read Bit D0 value.																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes				
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h				
Status	Default Value																						
Power On Sequence	00h																						
S/W Reset	00h																						
H/W Reset	00h																						
Flow Chart	<pre> sequenceDiagram participant Host participant Display Host->>Display: Read RDDSDR Display-->Host: Send Parameter </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Hexagon Action: Diamond Mode: Oval Sequential transfer: Oval with arrow 																						

5.3.11. Sleep In (10h)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
10h	-	W	No Argument									-							
Description	<p>10h: SLPIN (Sleep In). This command causes the ILI9881C-04 to enter the minimum power consumption mode. In this mode, the DC/DC converter, Internal oscillator, and panel scanning are all stopped.</p>  <p>MCU interface and memory are still working and the memory can keep its contents. Ambient light based control is off. Backlights and display are off. Dimming function does not work when there is changing mode from Sleep Out to Sleep In.</p>																		
Restriction	<p>This command has no effect when the module is already in the Sleep In mode. To leave the Sleep In Mode, only the Sleep Out Command (11h) is workable. It is necessary to wait 5msec before sending the next command; this is to allow time for the supply voltages and clock circuits to become stable. It is necessary to wait 120msec after sending the Sleep Out command (when in the Sleep In Mode) before the Sleep In command can be sent.</p>																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep In Mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep In Mode</td> </tr> <tr> <td>H/W Reset</td> <td>Sleep In Mode</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	Sleep In Mode	S/W Reset	Sleep In Mode	H/W Reset	Sleep In Mode
Status	Default Value																		
Power On Sequence	Sleep In Mode																		
S/W Reset	Sleep In Mode																		
H/W Reset	Sleep In Mode																		
Flow Chart	<p>It takes 120msec to get into Sleep In mode after SLPIN command issued.</p>  <div style="border: 1px dashed black; padding: 5px; margin-top: 10px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div>																		

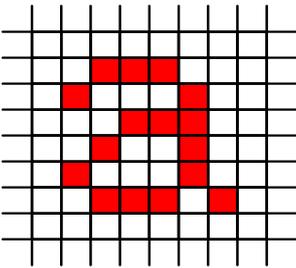
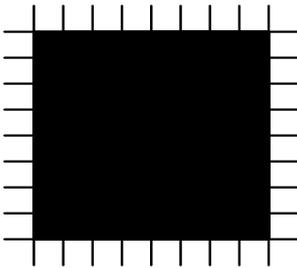
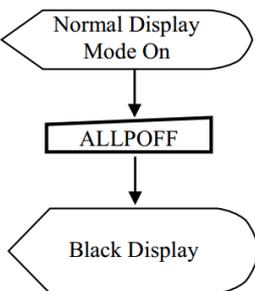
5.3.12. Sleep Out (11h)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
11h	-	W	No Argument									-							
Description	<p>11h: SLPOUT (Sleep Out). This command turns off the sleep mode. In this mode, the DC/DC converter is enabled, the Internal oscillator is started, and the panel scanning is started.</p> 																		
Restriction	<p>This command has no effect when the module is already in the Sleep Out mode. To leave the Sleep Out mode, only the Sleep In command (10h), SW Reset Command (01h) or HW Reset are workable. It is necessary to wait 5msec before sending the next command; this is to allow time for the supply voltages and clock circuits to become stable. The Driver IC loads all display supplier's factory default values to the registers during this 5msec. There cannot be any abnormal visual effect on the display image if factory default and register values are the same when this load is done and when the Driver IC is already in the Sleep Out mode. During this 5msec, the Driver IC also performs self-diagnostic functions. It is necessary to wait 120msec after sending the Sleep In command (when in the Sleep Out mode) before the Sleep Out command can be sent.</p>																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep In Mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep In Mode</td> </tr> <tr> <td>H/W Reset</td> <td>Sleep In Mode</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	Sleep In Mode	S/W Reset	Sleep In Mode	H/W Reset	Sleep In Mode
Status	Default Value																		
Power On Sequence	Sleep In Mode																		
S/W Reset	Sleep In Mode																		
H/W Reset	Sleep In Mode																		
Flow Chart	<p>It takes 120msec to become Sleep Out mode after SLPOUT command issued.</p> 																		

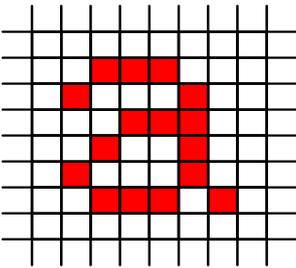
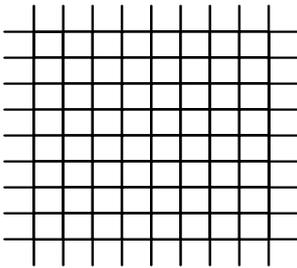
5.3.13. Normal Display Mode On (13h)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
13h	-	W	No Argument									-							
Description		13h: NORON (Normal Display Mode On). This command returns the display to normal mode.																	
Restriction		This command has no effect when the Normal Display Mode is active.																	
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal Display Mode On</td> </tr> <tr> <td>S/W Reset</td> <td>Normal Display Mode On</td> </tr> <tr> <td>H/W Reset</td> <td>Normal Display Mode On</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	Normal Display Mode On	S/W Reset	Normal Display Mode On	H/W Reset	Normal Display Mode On
Status	Default Value																		
Power On Sequence	Normal Display Mode On																		
S/W Reset	Normal Display Mode On																		
H/W Reset	Normal Display Mode On																		
Flow Chart																			

5.3.14. All Pixel Off (22h)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
22h	-	W	No Argument									-							
Description	<p>22h: ALLPOFF (All Pixels Off).</p> <p>This command turns the display panel black in 'Sleep Out' mode and a status bit of the 'Read Display Image Mode' register (0Dh) can be read.</p> <p>This command makes no change of contents of the input data (or frame memory). This command does not change any other status.</p>																		
	<div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Input Data/ Memory</p>  </div> <div style="font-size: 2em; margin: 0 20px;">→</div> <div style="text-align: center;"> <p>Display Panel</p>  </div> </div> <p>'All Pixels On' or 'Normal Display Mode On' commands are used to leave this mode. When ILI9881C-04 works in 'Idle Mode On' and 'Sleep Out' state, the display panel is showing the content of the frame memory after 'Normal Display Mode On' commands.</p>																		
Restriction	This command has no effect when module is already in all pixels off mode.																		
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OFF</td> </tr> <tr> <td>S/W Reset</td> <td>OFF</td> </tr> <tr> <td>H/W Reset</td> <td>OFF</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	OFF	S/W Reset	OFF	H/W Reset	OFF
Status	Default Value																		
Power On Sequence	OFF																		
S/W Reset	OFF																		
H/W Reset	OFF																		
Flow Chart	<div style="display: flex; justify-content: space-between; align-items: center;"> <div style="text-align: center;">  </div> <div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>																		

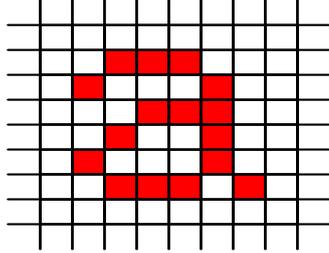
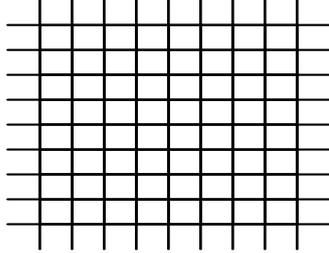
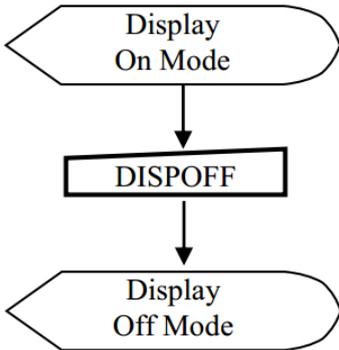
5.3.15. All Pixel On (23h)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
23h	-	W	No Argument									-							
Description	<p>23h: ALLPON (All Pixels On).</p> <p>This command turns the display panel white in 'Sleep out' mode and a status bit of the 'Read Display Image Mode' register (0Dh) can be read.</p> <p>This command makes no change of contents of the input data (or frame memory). This command does not change any other status.</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Input Data/ Memory</p>  </div> <div style="font-size: 2em; margin: 0 20px;">→</div> <div style="text-align: center;"> <p>Display Panel</p>  </div> </div> <p>'All Pixels Off' or 'Normal Display Mode On' commands are used to leave this mode.</p> <p>When ILI9881C-04 works in 'Idle Mode On' and 'Sleep Out' state, the display panel is showing the content of the frame memory after 'Normal Display Mode On' commands.</p>																		
	Restriction	This command has no effect when module is already in all pixels on mode.																	
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OFF</td> </tr> <tr> <td>S/W Reset</td> <td>OFF</td> </tr> <tr> <td>H/W Reset</td> <td>OFF</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	OFF	S/W Reset	OFF	H/W Reset	OFF
Status	Default Value																		
Power On Sequence	OFF																		
S/W Reset	OFF																		
H/W Reset	OFF																		
Flow Chart	<div style="display: flex; align-items: center; justify-content: center;"> <div style="text-align: center; margin-right: 20px;"> <p>Normal Display Mode On</p> <p>↓</p> <p>ALLPON</p> <p>↓</p> <p>White Display</p> </div> <div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>																		

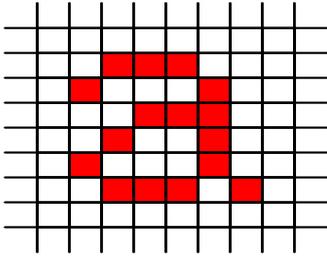
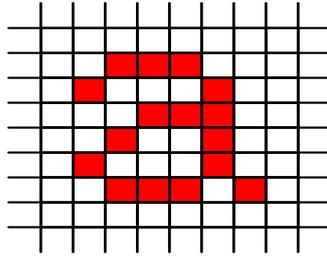
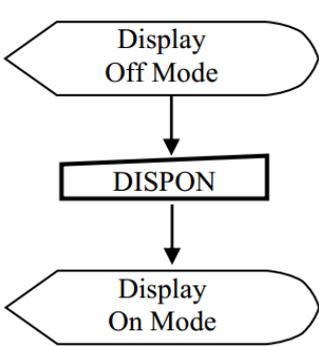
5.3.16. Gamma Set (26h)

Command Page		Page 0																	
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
26h	1st	W	0	0	0	0	GC [3:0]				01h								
Description	<p>26h: GAMSET (Gamma Set).</p> <p>This command is used to select the desired Gamma curve for the current display. A maximum of 1 fixed Gamma curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table below:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>GC [3:0]</th> <th>Curve Selected</th> </tr> </thead> <tbody> <tr> <td>1h</td> <td>Gamma curve 1</td> </tr> <tr> <td>Other</td> <td>Reserved</td> </tr> </tbody> </table> <p><i>Note: All others value are undefined.</i></p>											GC [3:0]	Curve Selected	1h	Gamma curve 1	Other	Reserved		
GC [3:0]	Curve Selected																		
1h	Gamma curve 1																		
Other	Reserved																		
Restriction	<p>Values of GC [3:0] not shown in the table above are invalid and will not change the current selected Gamma curve until a valid value is received.</p>																		
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>01h</td> </tr> <tr> <td>S/W Reset</td> <td>01h</td> </tr> <tr> <td>H/W Reset</td> <td>01h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	01h	S/W Reset	01h	H/W Reset	01h
Status	Default Value																		
Power On Sequence	01h																		
S/W Reset	01h																		
H/W Reset	01h																		
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <pre> graph TD A[GAMSET] --> B[/GC[7..0]/] B --> C[/New Gamma Curve Loaded/] </pre> </div> <div style="flex: 1; border: 1px dashed black; padding: 5px;"> <p style="text-align: center;">Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>																		

5.3.17. Display Off (28h)

Command Page		Page 0																	
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
28h	-	W	No Argument									-							
Description	<p>28h: DISPOFF (Display Off)</p> <p>This command is used to enter into the Display Off mode. Output from the input data (or frame memory) is disabled and a blank page inserted. This command makes no change of contents of the input data (or frame memory) and does not change any other status. There will be no abnormal visible effect on the display.</p>																		
	<div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Input Data/ Memory</p>  </div> <div style="font-size: 2em; margin: 0 20px;">→</div> <div style="text-align: center;"> <p>Display Panel</p>  </div> </div>																		
Restriction	This command has no effect when the module is already in the Display Off mode.																		
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Off</td> </tr> <tr> <td>S/W Reset</td> <td>Display Off</td> </tr> <tr> <td>H/W Reset</td> <td>Display Off</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	Display Off	S/W Reset	Display Off	H/W Reset	Display Off
Status	Default Value																		
Power On Sequence	Display Off																		
S/W Reset	Display Off																		
H/W Reset	Display Off																		
Flow Chart	<div style="display: flex; justify-content: space-between; align-items: center;"> <div style="text-align: center;">  </div> <div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>																		

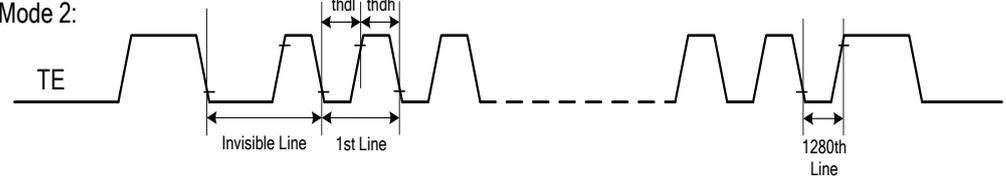
5.3.18. Display ON (29h)

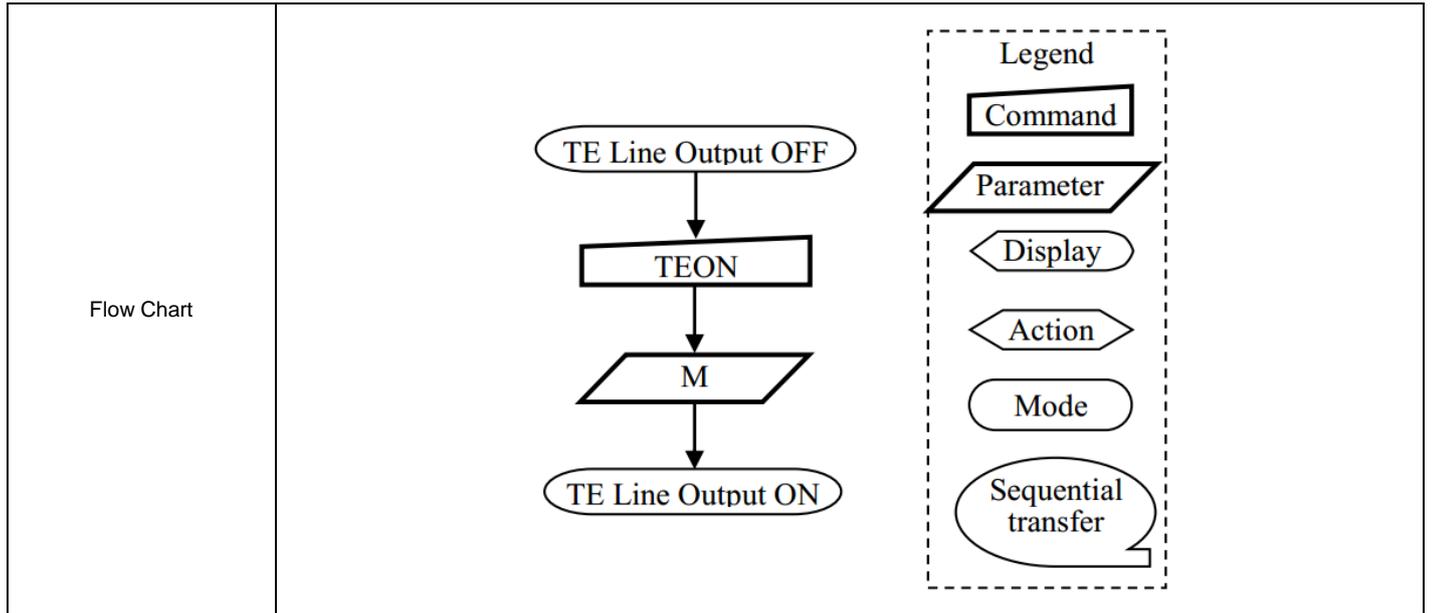
Command Page		Page 0																	
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
29h	-	W	No Argument									-							
Description	<p>29h: DISPON (Display On).</p> <p>This command is used to recover from the Display Off mode. Output from the input data (or frame memory) is enabled. This command makes no change of contents of the input data (or frame memory) and does not change any other status.</p>																		
	<div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>Input Data/ Memory</p>  </div> <div style="font-size: 2em; margin: 0 20px;">→</div> <div style="text-align: center;"> <p>Display Panel</p>  </div> </div>																		
Restriction	This command has no effect when the ILI9881C-04 is already in the Display On mode.																		
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Off</td> </tr> <tr> <td>S/W Reset</td> <td>Display Off</td> </tr> <tr> <td>H/W Reset</td> <td>Display Off</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	Display Off	S/W Reset	Display Off	H/W Reset	Display Off
Status	Default Value																		
Power On Sequence	Display Off																		
S/W Reset	Display Off																		
H/W Reset	Display Off																		
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;">  <pre> graph TD A[Display Off Mode] --> B[DISPON] B --> C[Display On Mode] </pre> </div> <div style="border: 1px dashed black; padding: 5px; margin-left: 20px;"> <p>Legend</p> <ul style="list-style-type: none"> Command: [DISPON] Parameter: [Parameter] Display: [Display] Action: [Action] Mode: [Mode] Sequential transfer: [Sequential transfer] </div> </div>																		

5.3.19. Tearing Effect Line Off (34h)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
34h	-	W	No Argument									-							
Description	<p>34h: TEOFF (Tearing Effect Line OFF). This command is used to turn off the Display module's Tearing Effect output signal from the TE signal line.</p>																		
Restriction	This command has no effect when the Tearing Effect output is already off.																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Off</td> </tr> <tr> <td>S/W Reset</td> <td>Off</td> </tr> <tr> <td>H/W Reset</td> <td>Off</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	Off	S/W Reset	Off	H/W Reset	Off
Status	Default Value																		
Power On Sequence	Off																		
S/W Reset	Off																		
H/W Reset	Off																		
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <pre> graph TD A([TE Line Output ON]) --> B[TEOFF] B --> C([TE Line Output OFF]) </pre> </div> <div style="flex: 1; border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>																		

5.3.20. Tearing Effect Line On (35h)

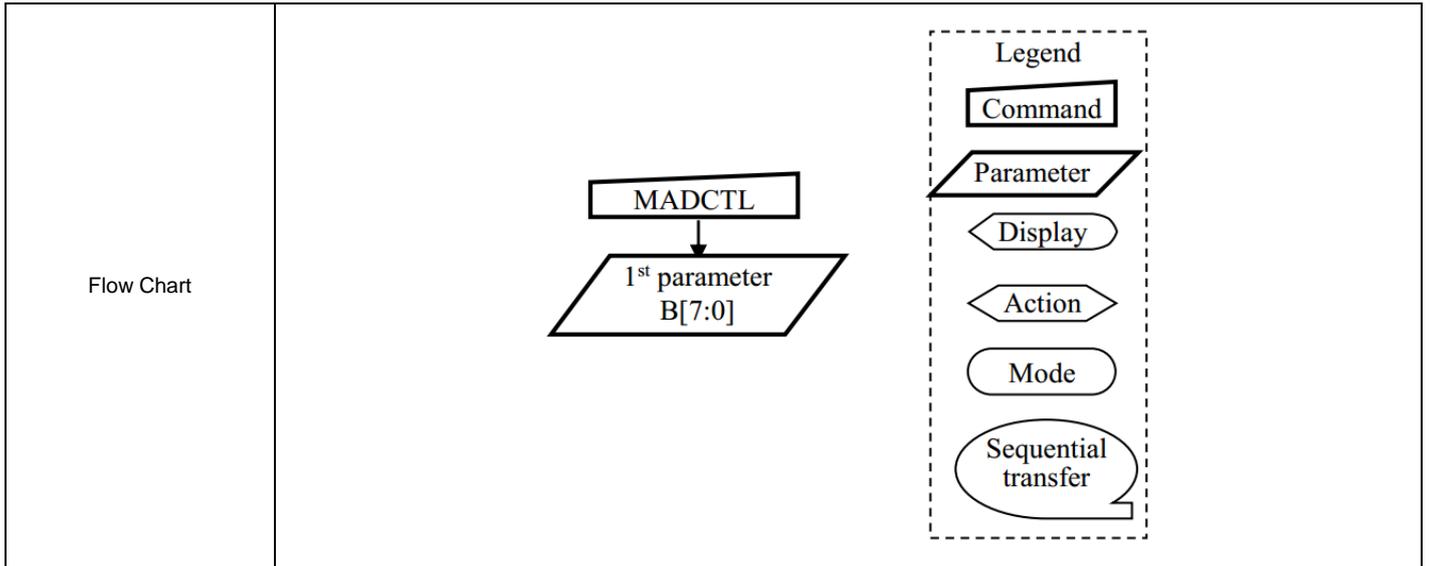
Command Page		Page 0																	
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
35h	1st	W	0	0	0	0	0	0	0	M	00								
Description	<p>35h: TEON (Tearing Effect Line ON).</p> <p>This command is used to turn on the Tearing Effect output signal from the TE signal line. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.</p> <p>When M=0: The Tearing Effect Output line consists of V-Blanking information only:</p> <p style="text-align: center;">Mode 1:</p>  <p style="text-align: center;">When M=1: The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:</p> <p style="text-align: center;">Mode 2:</p>  <p><i>Note : The Tearing Effect Output line shall be low when the display module is in Sleep mode</i></p>																		
	Restriction	This command has no effect when the Tearing Effect output is already ON.																	
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Off</td> </tr> <tr> <td>S/W Reset</td> <td>Off</td> </tr> <tr> <td>H/W Reset</td> <td>Off</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	Off	S/W Reset	Off	H/W Reset	Off
Status	Default Value																		
Power On Sequence	Off																		
S/W Reset	Off																		
H/W Reset	Off																		



5.3.21. Memory Access Control (36h)

Command Page		Page 0																									
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																
36h	1st	W	0	0	0	0	BGR	0	SS	GS	00h																
Description		36h: MADCTL (Memory Access Control).																									
		This command makes no change on the other status of the driver.																									
		<table border="1"> <thead> <tr> <th>Bit</th> <th>Symbol</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>D3</td> <td>BGR</td> <td>RGB/BGR Order</td> <td>Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)</td> </tr> <tr> <td>D1</td> <td>SS</td> <td>Flip Horizontal (SS)</td> <td>Select the Source driver scan direction on the panel module</td> </tr> <tr> <td>D0</td> <td>GS</td> <td>Flip Vertical (GS)</td> <td>Select the Gate driver scan direction on the panel module</td> </tr> </tbody> </table>										Bit	Symbol	Name	Description	D3	BGR	RGB/BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)	D1	SS	Flip Horizontal (SS)	Select the Source driver scan direction on the panel module	D0	GS	Flip Vertical (GS)	Select the Gate driver scan direction on the panel module
		Bit	Symbol	Name	Description																						
		D3	BGR	RGB/BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)																						
		D1	SS	Flip Horizontal (SS)	Select the Source driver scan direction on the panel module																						
		D0	GS	Flip Vertical (GS)	Select the Gate driver scan direction on the panel module																						
		BGR (RGB-BGR Order control bit)="0"					BGR (RGB-BGR Order control bit)="1"																				
		SS (Source Scan sequence)="0"					SS (Source Scan sequence)="1"																				
GS (Gate Scan sequence)="0"					GS (Gate Scan sequence)="1"																						
Restriction	None																										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes								
Status	Availability																										
Normal Mode On, Idle Mode Off, Sleep Out	Yes																										
Normal Mode On, Idle Mode On, Sleep Out	Yes																										
Sleep In	Yes																										
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h								
Status	Default Value																										
Power On Sequence	00h																										
S/W Reset	00h																										
H/W Reset	00h																										

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5.3.22. Idle Mode Off (38h)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
38h	-	W	No Argument									-							
Description	38h: IDMOFF (Idle mode off). This command causes the Display module to exit the Idle mode. In the Idle Mode Off, the display panel can display a maximum of 16.7M colors.																		
Restriction	This command has no effect when the module is already in the Idle Mode Off.																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Idle Mode Off</td> </tr> <tr> <td>S/W Reset</td> <td>Idle Mode Off</td> </tr> <tr> <td>H/W Reset</td> <td>Idle Mode Off</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	Idle Mode Off	S/W Reset	Idle Mode Off	H/W Reset	Idle Mode Off
Status	Default Value																		
Power On Sequence	Idle Mode Off																		
S/W Reset	Idle Mode Off																		
H/W Reset	Idle Mode Off																		
Flow Chart	<pre> graph TD A[Idle on mode] -- Action --> B[Command: IDMOFF] B -- Action --> C[Idle off mode] </pre> <p>The flow chart illustrates the process of switching from 'Idle on mode' to 'Idle off mode'. It starts with 'Idle on mode' (represented by a hexagon), followed by an arrow (Action) pointing to the 'IDMOFF' command (represented by a rectangle). Another arrow (Action) points from 'IDMOFF' to 'Idle off mode' (represented by a hexagon). A legend on the right defines the symbols used: Command (rectangle), Parameter (parallelogram), Display (hexagon), Action (arrow), Mode (oval), and Sequential transfer (speech bubble).</p>																		

5.3.23. Idle Mode On (39h)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
39h	-	W	No Argument									-							
Description	<p>39h: IDMON (Idle mode on).</p> <p>This command is used to enter into the Idle Mode On. In the Idle Mode On, color expression is reduced.</p> <p>The display panel shows de-compressed content of frame memory in the Idle Mode On and Sleep Out states.</p>																		
Restriction	This command has no effect when the module is already in the Idle Mode On.																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Idle Mode Off</td> </tr> <tr> <td>S/W Reset</td> <td>Idle Mode Off</td> </tr> <tr> <td>H/W Reset</td> <td>Idle Mode Off</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	Idle Mode Off	S/W Reset	Idle Mode Off	H/W Reset	Idle Mode Off
Status	Default Value																		
Power On Sequence	Idle Mode Off																		
S/W Reset	Idle Mode Off																		
H/W Reset	Idle Mode Off																		
Flow Chart	<pre> graph TD A([Idle off mode]) --> B[IDMON] B --> C([Idle on mode]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Oval Action: Diamond Mode: Rounded rectangle Sequential transfer: Loop arrow 																		

5.3.24. Interface Pixel Format (3Ah)

Command Page		Page 0																											
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																		
3Ah	1st	W	0	0	0	0	0	DBI[2:0]			07h																		
Description	<p>3A: COLMOD (Interface Pixel Format).</p> <p>This command is used to define the format of RGB picture data, which is to be transferred via the MIPI DSI Command Mode. The formats are shown in the table:</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Interface Format</th> <th>DBI[2:0]</th> </tr> </thead> <tbody> <tr><td>Not Defined</td><td>000</td></tr> <tr><td>Not Defined</td><td>001</td></tr> <tr><td>Not Defined</td><td>010</td></tr> <tr><td>Not Defined</td><td>011</td></tr> <tr><td>Not Defined</td><td>100</td></tr> <tr><td>16 bit/pixel</td><td>101</td></tr> <tr><td>18 bit/pixel</td><td>110</td></tr> <tr><td>24 bit/pixel</td><td>111</td></tr> </tbody> </table>											Interface Format	DBI[2:0]	Not Defined	000	Not Defined	001	Not Defined	010	Not Defined	011	Not Defined	100	16 bit/pixel	101	18 bit/pixel	110	24 bit/pixel	111
	Interface Format	DBI[2:0]																											
Not Defined	000																												
Not Defined	001																												
Not Defined	010																												
Not Defined	011																												
Not Defined	100																												
16 bit/pixel	101																												
18 bit/pixel	110																												
24 bit/pixel	111																												
Restriction	There is no visible effect until the Frame Memory is written to.																												
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes										
Status	Availability																												
Normal Mode On, Idle Mode Off, Sleep Out	Yes																												
Normal Mode On, Idle Mode On, Sleep Out	Yes																												
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Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>07h</td> </tr> <tr> <td>S/W Reset</td> <td>07h</td> </tr> <tr> <td>H/W Reset</td> <td>07h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	07h	S/W Reset	07h	H/W Reset	07h										
Status	Default Value																												
Power On Sequence	07h																												
S/W Reset	07h																												
H/W Reset	07h																												
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <pre> graph TD A([16 Bit/Pixel Mode]) --> B[COLMOD] B --> C[/111/] C --> D([24 Bit/Pixel Mode]) </pre> </div> <div style="flex: 1; border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>																												

5.3.25. Set_Tear_Scanline (44h)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
44h	1st	W	0	0	0	0	0	TE_LINE[10:8]			00h								
	2nd	W	TE_LINE[7:0]									00h							
Description		<p>44h: SET_TEAR_SCANLINE.</p> <p>This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N.</p> <p>The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode. After issuing a set_tear_scanline command to the display module, the Tearing Effect output signal, e.g. as in DBI-2 systems, shall be a delayed version of V-Blanking information as illustrated by below figure.</p> <p>In other words, the TE pulse width needs to be identical with normal mode Vsync related TE pulse.</p> <div style="text-align: center;"> </div> <p>Note that set_tear_scanline with N = 0 is equivalent to set_tear_on with M = 0.</p> <p>The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</p>																	
Restriction		<p>This command takes affect on the frame following the current frame.</p> <p>Therefore, if the Tear Effect (TE) output is already ON, the TE output shall continue to operate as programmed by the previous set_tear_on, or set_tear_scanline, command until the end of the frame.</p>																	
Register Availability		<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>No</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	No
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	No																		
Default		<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N=0</td> </tr> <tr> <td>S/W Reset</td> <td>N=0</td> </tr> <tr> <td>H/W Reset</td> <td>N=0</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	N=0	S/W Reset	N=0	H/W Reset	N=0
Status	Default Value																		
Power On Sequence	N=0																		
S/W Reset	N=0																		
H/W Reset	N=0																		
Flow Chart		<div style="text-align: center;"> </div>																	

5.3.26. Get_Tear_Scanline (45h)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
45h	1st	R	0	0	0	0	0	TE_LINE[10:8]			00h								
	2nd	R	TE_LINE[7:0]									00h							
Description		45h: GET_TEAR_SCANLINE. This command returns setting value of Set_Tear_Scanline command (44h).																	
Restriction		None																	
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>No</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	No
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	No																		
Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N=0</td> </tr> <tr> <td>S/W Reset</td> <td>N=0</td> </tr> <tr> <td>H/W Reset</td> <td>N=0</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	N=0	S/W Reset	N=0	H/W Reset	N=0
Status	Default Value																		
Power On Sequence	N=0																		
S/W Reset	N=0																		
H/W Reset	N=0																		
Flow Chart		<pre> graph TD subgraph Host C[Read GET_TEAR_SCANLINE] end subgraph Display P1[/Send 1st Parameter/] P2[/Send 2nd Parameter/] end C --> P1 P1 --> P2 </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Oval Action: Diamond Mode: Rounded rectangle Sequential transfer: Cloud shape 																	

5.3.27. Write Display Brightness Value (51h)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
51h	1st	W	0	0	0	0	DBV[11:8]				00h								
	2nd	W	DBV[7:0]									00h							
Description		<p>51h: WRDISBV (Write Display Brightness).</p> <p>This command is used to adjust the brightness value of the display.</p> <p>DBV[11:0]: 12 bit, for display brightness of manual brightness setting and the CABC in the ILI9881C-04. PWM output signal and LEDPWM pin will control the LED driver IC in order to control the display brightness. In principle relationship is that 0000h value means the lowest brightness and 0FFFh value means the highest brightness.</p>																	
Restriction		None																	
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h_00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h_00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h_00h</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	00h_00h	S/W Reset	00h_00h	H/W Reset	00h_00h
Status	Default Value																		
Power On Sequence	00h_00h																		
S/W Reset	00h_00h																		
H/W Reset	00h_00h																		
Flow Chart		<pre> graph TD A[WRDISBV] --> B[/DBV (MSB)/] B --> C[/DBV (LSB)/] C --> D{New Display Brightness Value Loaded} </pre>																	

5.3.28. Read Display Brightness Value (52h)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
52h	1st	R	0	0	0	0	DBV[11:8]				00h								
	2nd	R	DBV[7:0]								00h								
Description	<p>52h: RDDISBV (Read Display Brightness Value).</p> <p>This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification.</p> <p>In principle the relationship is that 0000h value means the lowest brightness and 0FFFh value means the highest brightness.</p> <p>DBV[11:0] is reset when display is in sleep-in mode.</p> <p>DBV[11:0] is '0' when bit BCTRL of "5.3.29Write CTRL Display Value (53h)" command is '0'.</p> <p>DBV[11:0] is manual set brightness specified with "5.3.29Write CTRL Display Value (53h)" command when bit BCTRL is '1'.</p>																		
Restriction	None																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h_00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h_00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h_00h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h_00h	S/W Reset	00h_00h	H/W Reset	00h_00h
Status	Default Value																		
Power On Sequence	00h_00h																		
S/W Reset	00h_00h																		
H/W Reset	00h_00h																		
Flow Chart	<pre> graph TD subgraph Host C[Read RDDISBV] end subgraph Display P1[/Send 1st Parameter/] P2[/Send 2nd Parameter/] end C --> P1 P1 --> P2 </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Oval Action: Arrow Mode: Rounded Rectangle Sequential transfer: Dashed line 																		

5.3.29. Write CTRL Display Value (53h)

Command Page		Page 0																	
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
53h	1st	W	0	0	BCTRL	0	DD	BL	0	0	00h								
Description	53h: WRCTRLD (Write Control Display). This command is used to control the display brightness. BCTRL : Brightness Control Block On/Off. This bit is always used to switch brightness for display.																		
	<table border="1"> <thead> <tr> <th>BCTRL</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Brightness Control Block Off (DBV[11:0] = 0000h)</td> </tr> <tr> <td>1</td> <td>Brightness Control Block On (DBV[11:0] is active)</td> </tr> </tbody> </table>											BCTRL	Description	0	Brightness Control Block Off (DBV[11:0] = 0000h)	1	Brightness Control Block On (DBV[11:0] is active)		
	BCTRL	Description																	
	0	Brightness Control Block Off (DBV[11:0] = 0000h)																	
	1	Brightness Control Block On (DBV[11:0] is active)																	
DD : Display Dimming Control.																			
<table border="1"> <thead> <tr> <th>DD</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Display Dimming Off</td> </tr> <tr> <td>1</td> <td>Display Dimming On</td> </tr> </tbody> </table>											DD	Description	0	Display Dimming Off	1	Display Dimming On			
DD	Description																		
0	Display Dimming Off																		
1	Display Dimming On																		
BL : Backlight Control On/Off																			
<table border="1"> <thead> <tr> <th>BL</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Backlight Control Off</td> </tr> <tr> <td>1</td> <td>Backlight Control On</td> </tr> </tbody> </table>											BL	Description	0	Backlight Control Off	1	Backlight Control On			
BL	Description																		
0	Backlight Control Off																		
1	Backlight Control On																		
Dimming function is adapted to the brightness registers for display when the bit BCTRL is changed at DD = 1, e.g. BCTRL: 0-> 1 or 1-> 0. When the BL bit changes from 'ON' to 'OFF', backlight is turned off without gradual dimming, even if Display Dimming On (DD = 1) are selected.																			
Restriction	None																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value																		
Power On Sequence	00h																		
S/W Reset	00h																		
H/W Reset	00h																		
Flow Chart	<pre> graph TD A[WRCTRLD] --> B[/HBM, BCTRL, DD, BL/] B --> C{{New Control Value Loaded}} </pre>																		

5.3.30. Read CTRL Display Value (54h)

Command Page		Page 0																											
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																		
54h	1st	R	0	0	BCTRL	0	DD	BL	0	0	00h																		
Description	<p>54h: RDCTRLD (Read Control Value Display).</p> <p>This command returns the display brightness control values.</p> <p>BCTRL: Brightness Control Block On/Off. This bit is always used to switch brightness for display.</p> <table border="1"> <thead> <tr> <th>BCTRL</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Brightness Control Block Off (DBV[11:0] = 0000h)</td> </tr> <tr> <td>1</td> <td>Brightness Control Block On (DBV[11:0] is active)</td> </tr> </tbody> </table> <p>DD: Display Dimming Control.</p> <table border="1"> <thead> <tr> <th>DD</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Display Dimming Off</td> </tr> <tr> <td>1</td> <td>Display Dimming On</td> </tr> </tbody> </table> <p>BL: Backlight Control On/Off</p> <table border="1"> <thead> <tr> <th>BL</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Backlight Control Off</td> </tr> <tr> <td>1</td> <td>Backlight Control On</td> </tr> </tbody> </table> <p>Dimming function is adapted to the brightness registers for display when the bit BCTRL is changed at DD = 1, e.g. BCTRL: 0-> 1 or 1-> 0.</p> <p>When the BL bit changes from 'ON' to 'OFF', backlight is turned off without gradual dimming, even if Display Dimming On (DD = 1) are selected.</p>											BCTRL	Description	0	Brightness Control Block Off (DBV[11:0] = 0000h)	1	Brightness Control Block On (DBV[11:0] is active)	DD	Description	0	Display Dimming Off	1	Display Dimming On	BL	Description	0	Backlight Control Off	1	Backlight Control On
	BCTRL	Description																											
	0	Brightness Control Block Off (DBV[11:0] = 0000h)																											
	1	Brightness Control Block On (DBV[11:0] is active)																											
	DD	Description																											
0	Display Dimming Off																												
1	Display Dimming On																												
BL	Description																												
0	Backlight Control Off																												
1	Backlight Control On																												
Restriction	None																												
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes										
Status	Availability																												
Normal Mode On, Idle Mode Off, Sleep Out	Yes																												
Normal Mode On, Idle Mode On, Sleep Out	Yes																												
Sleep In	Yes																												
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h										
Status	Default Value																												
Power On Sequence	00h																												
S/W Reset	00h																												
H/W Reset	00h																												
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <pre> graph TD A[Read RDCTRLD] --> B[/Send Parameter/] </pre> <p style="text-align: center;">Host ----- Display</p> </div> <div style="border: 1px dashed black; padding: 5px; margin-left: 20px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>																												

5.3.31. Write Power Save (55h)

Command Page			Page 0																																												
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																				
55h	1st	W	PWRSAVE[7:0]									00h																																			
Description	55h: PWRSAVE (Write Power Save). This command is used to write the settings for power save control functionalities.																																														
	<table border="1"> <thead> <tr> <th>PWRSAVE[7:0]</th> <th>Function</th> <th>Note</th> </tr> </thead> <tbody> <tr> <td>00000000</td> <td>Power Save Off</td> <td>-</td> </tr> <tr> <td>00000001</td> <td>Power Save Low</td> <td>Conservative Setting of CABC/DBLC</td> </tr> <tr> <td>00000010</td> <td>Power Save Medium</td> <td>Medium Setting of CABC/DBLC</td> </tr> <tr> <td>00000011</td> <td>Power Save High</td> <td>Aggressive Setting of CABC/DBLC</td> </tr> <tr> <td>1000XXXX</td> <td>IE On – Low</td> <td>Low Enhancement of LCD</td> </tr> <tr> <td>1001XXXX</td> <td>IE On – Medium</td> <td>Medium Enhancement of LCD</td> </tr> <tr> <td>1011XXXX</td> <td>IE On – High</td> <td>High Enhancement of LCD</td> </tr> <tr> <td>0100XXXX</td> <td>SRE - Low</td> <td>Sunlight readability enhancement</td> </tr> <tr> <td>0101XXXX</td> <td>SRE - Medium</td> <td>Sunlight readability enhancement</td> </tr> <tr> <td>0110XXXX</td> <td>SRE - High</td> <td>Sunlight readability enhancement</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>-</td> </tr> </tbody> </table>											PWRSAVE[7:0]	Function	Note	00000000	Power Save Off	-	00000001	Power Save Low	Conservative Setting of CABC/DBLC	00000010	Power Save Medium	Medium Setting of CABC/DBLC	00000011	Power Save High	Aggressive Setting of CABC/DBLC	1000XXXX	IE On – Low	Low Enhancement of LCD	1001XXXX	IE On – Medium	Medium Enhancement of LCD	1011XXXX	IE On – High	High Enhancement of LCD	0100XXXX	SRE - Low	Sunlight readability enhancement	0101XXXX	SRE - Medium	Sunlight readability enhancement	0110XXXX	SRE - High	Sunlight readability enhancement	Others	Reserved	-
	PWRSAVE[7:0]	Function	Note																																												
	00000000	Power Save Off	-																																												
	00000001	Power Save Low	Conservative Setting of CABC/DBLC																																												
	00000010	Power Save Medium	Medium Setting of CABC/DBLC																																												
	00000011	Power Save High	Aggressive Setting of CABC/DBLC																																												
	1000XXXX	IE On – Low	Low Enhancement of LCD																																												
	1001XXXX	IE On – Medium	Medium Enhancement of LCD																																												
	1011XXXX	IE On – High	High Enhancement of LCD																																												
0100XXXX	SRE - Low	Sunlight readability enhancement																																													
0101XXXX	SRE - Medium	Sunlight readability enhancement																																													
0110XXXX	SRE - High	Sunlight readability enhancement																																													
Others	Reserved	-																																													
CABC = Content Adaptive Brightness Control DBLC = Dynamic Backlight Control IE = Image Enhancement																																															
Restriction	None																																														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																												
Status	Availability																																														
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																														
Normal Mode On, Idle Mode On, Sleep Out	Yes																																														
Sleep In	Yes																																														
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h																												
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Power On Sequence	00h																																														
S/W Reset	00h																																														
H/W Reset	00h																																														
Flow Chart	<div style="display: flex; align-items: center;"> <div style="flex: 1;"> <pre> graph TD A[WRPWRSAVE] --> B[/Parameter/] B --> C{{New Power Save Mode}} </pre> </div> <div style="flex: 1; border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div> </div>																																														

5.3.32. Read Power Save (56h)

Command Page			Page 0																																												
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																				
56h	1st	R	PWRSAVE[7:0]									00h																																			
Description	56h: RDPWRSAVE (Read Power Save). This command is used to read the settings for power save control functionalities.																																														
	<table border="1"> <thead> <tr> <th>PWRSAVE[7:0]</th> <th>Function</th> <th>Note</th> </tr> </thead> <tbody> <tr> <td>00000000</td> <td>Power Save Off</td> <td>-</td> </tr> <tr> <td>00000001</td> <td>Power Save Low</td> <td>Conservative Setting of CABC/DBLC</td> </tr> <tr> <td>00000010</td> <td>Power Save Medium</td> <td>Medium Setting of CABC/DBLC</td> </tr> <tr> <td>00000011</td> <td>Power Save High</td> <td>Aggressive Setting of CABC/DBLC</td> </tr> <tr> <td>1000XXXX</td> <td>IE On – Low</td> <td>Low Enhancement of LCD</td> </tr> <tr> <td>1001XXXX</td> <td>IE On – Medium</td> <td>Medium Enhancement of LCD</td> </tr> <tr> <td>1011XXXX</td> <td>IE On – High</td> <td>High Enhancement of LCD</td> </tr> <tr> <td>0100XXXX</td> <td>SRE - Low</td> <td>Sunlight readability enhancement</td> </tr> <tr> <td>0101XXXX</td> <td>SRE - Medium</td> <td>Sunlight readability enhancement</td> </tr> <tr> <td>0110XXXX</td> <td>SRE - High</td> <td>Sunlight readability enhancement</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>-</td> </tr> </tbody> </table>											PWRSAVE[7:0]	Function	Note	00000000	Power Save Off	-	00000001	Power Save Low	Conservative Setting of CABC/DBLC	00000010	Power Save Medium	Medium Setting of CABC/DBLC	00000011	Power Save High	Aggressive Setting of CABC/DBLC	1000XXXX	IE On – Low	Low Enhancement of LCD	1001XXXX	IE On – Medium	Medium Enhancement of LCD	1011XXXX	IE On – High	High Enhancement of LCD	0100XXXX	SRE - Low	Sunlight readability enhancement	0101XXXX	SRE - Medium	Sunlight readability enhancement	0110XXXX	SRE - High	Sunlight readability enhancement	Others	Reserved	-
	PWRSAVE[7:0]	Function	Note																																												
	00000000	Power Save Off	-																																												
	00000001	Power Save Low	Conservative Setting of CABC/DBLC																																												
	00000010	Power Save Medium	Medium Setting of CABC/DBLC																																												
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0100XXXX	SRE - Low	Sunlight readability enhancement																																													
0101XXXX	SRE - Medium	Sunlight readability enhancement																																													
0110XXXX	SRE - High	Sunlight readability enhancement																																													
Others	Reserved	-																																													
CABC = Content Adaptive Brightness Control DBLC = Dynamic Backlight Control IE = Image Enhancement																																															
Restriction	None																																														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																												
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Normal Mode On, Idle Mode On, Sleep Out	Yes																																														
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Status	Default Value																																														
Power On Sequence	00h																																														
S/W Reset	00h																																														
H/W Reset	00h																																														
Flow Chart	<div style="display: flex; align-items: center; justify-content: center;"> <div style="border: 1px solid black; padding: 5px; margin-right: 20px;">Read RDPWRSAVE</div> <div style="text-align: center;">↓</div> <div style="border: 1px solid black; padding: 5px; margin-right: 20px;">Send Parameter</div> <div style="text-align: center;">→</div> <div style="text-align: center;">Host Display</div> </div> <div style="border: 1px dashed black; padding: 10px; margin-top: 20px;"> <p style="text-align: center;">Legend</p> <div style="display: flex; flex-direction: column; gap: 10px;"> <div style="border: 1px solid black; padding: 2px; width: 60px; margin: 0 auto;">Command</div> <div style="border: 1px solid black; padding: 2px; width: 60px; margin: 0 auto;">Parameter</div> <div style="border: 1px solid black; padding: 2px; width: 60px; margin: 0 auto;">Display</div> <div style="border: 1px solid black; padding: 2px; width: 60px; margin: 0 auto;">Action</div> <div style="border: 1px solid black; padding: 2px; width: 60px; margin: 0 auto;">Mode</div> <div style="border: 1px solid black; padding: 2px; width: 60px; margin: 0 auto;">Sequential transfer</div> </div> </div>																																														

5.3.33. Stop Transition (59h)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
59h	-	W	No Argument									-							
Description	<p>59h: STOP_TR (Stop Transition).</p> <p>When DD bit status of "5.3.29Write CTRL Display Value (53h)" register is '1', applying this command instantly stops the ongoing transition of Display Dimming.</p> <p>When display module receives this command, the current output value stays active.</p>																		
Restriction	This command has no effect when Display Dimming transition is not active.																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
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Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Off</td> </tr> <tr> <td>S/W Reset</td> <td>Off</td> </tr> <tr> <td>H/W Reset</td> <td>Off</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	Off	S/W Reset	Off	H/W Reset	Off
Status	Default Value																		
Power On Sequence	Off																		
S/W Reset	Off																		
H/W Reset	Off																		
Flow Chart	<pre> graph TD A[Display Dimming transition is active] --> B[STOP TR] B --> C[Stop ongoing transition] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Display shape Action: Action shape Mode: Oval Sequential transfer: Oval with tail 																		

5.3.34. Write CABC Minimum Brightness (5Eh)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
5Eh	1st	W	0	0	0	0	CMB[11:8]				00h								
	2nd	W	CMB[7:0]									00h							
Description		5Eh: WRCABCMB (Write CABC minimum brightness). This command is used to set the minimum brightness value of the display for CABC function. In principle relationship is that 0000h value means the lowest brightness for CABC and 0FFFh value means the highest brightness for CABC.																	
Restriction		None																	
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h_00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h_00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h_00h</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	00h_00h	S/W Reset	00h_00h	H/W Reset	00h_00h
Status	Default Value																		
Power On Sequence	00h_00h																		
S/W Reset	00h_00h																		
H/W Reset	00h_00h																		
Flow Chart		<pre> graph TD WRCABCMB[WRCABCMB] --> CMB[CMB[7..0]] CMB --> Display[New Display Luminance Value Loaded] </pre>																	

5.3.35. Read CABC Minimum Brightness (5Fh)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
5Fh	1st	R	0	0	0	0	CMB[11:8]				00h								
	2nd	R	CMB[7:0]								00h								
Description		<p>5Fh: RDCABCMB (Read CABC Minimum Brightness).</p> <p>This command returns the minimum brightness value of CABC function.</p> <p>In principle the relationship is that 0000h value means the lowest brightness and 0FFFh value means the highest brightness.</p> <p>CMB[11:0] is CABC minimum brightness specified by the Write CABC minimum brightness (5Eh) command.</p>																	
Restriction		None																	
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
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Sleep In	Yes																		
Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h_00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h_00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h_00h</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	00h_00h	S/W Reset	00h_00h	H/W Reset	00h_00h
Status	Default Value																		
Power On Sequence	00h_00h																		
S/W Reset	00h_00h																		
H/W Reset	00h_00h																		
Flow Chart		<pre> graph TD subgraph Host C[Read RDCABCMB] end subgraph Display P[/Send Parameter/] end C --> P </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Oval Action: Arrow Mode: Rounded Rectangle Sequential transfer: Cloud shape 																	

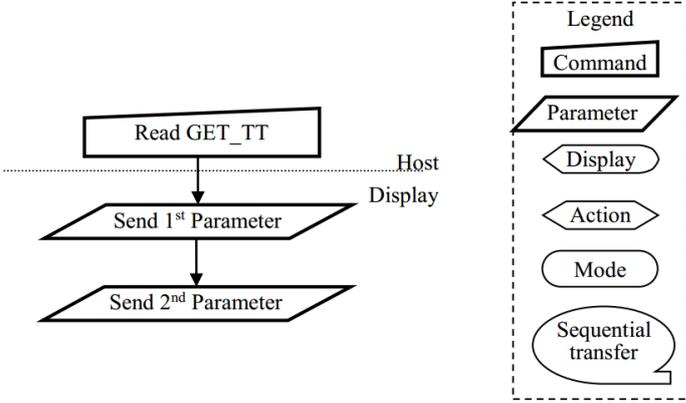
5.3.36. Set Transition Time (68h)

Command Page			Page 0																																																																		
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																																										
68h	1st	W	TT_STP[7:0]								00h																																																										
	2nd	W	ST_TIM[7:0]								00h																																																										
Description	<p>68h: SET_TT (Set Transition Time).</p> <p>This command controls the total transition time of Display Dimming function.</p> <p>Transition time is adjusted with two parameters, defining as follows:</p> <p>1st Parameter TT_STP [7:0] defines the number of dimming steps for transition.</p> <table border="1"> <thead> <tr> <th>TT_STP [7:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>00h</td><td>1 step</td></tr> <tr><td>01h</td><td>2 step</td></tr> <tr><td>02h</td><td>4 step</td></tr> <tr><td>03h</td><td>8 step</td></tr> <tr><td>04h</td><td>16 step</td></tr> <tr><td>05h</td><td>32 step</td></tr> <tr><td>06h</td><td>64 step</td></tr> <tr><td>07h</td><td>128 step</td></tr> <tr><td>08h</td><td>256 step</td></tr> <tr><td>09h</td><td>512 step</td></tr> <tr><td>0Ah</td><td>1024 step</td></tr> <tr><td>0Bh</td><td>2048 step</td></tr> <tr><td>0Ch</td><td>4096 step</td></tr> <tr><td>Others</td><td>Reserved</td></tr> </tbody> </table> <p>2nd Parameter ST_TIM [7:0] defines the step time as frame units for each dimming step.</p> <table border="1"> <thead> <tr> <th>ST_TIM [7:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>00h</td><td>1 frame</td></tr> <tr><td>01h</td><td>1 frame</td></tr> <tr><td>02h</td><td>2 frame</td></tr> <tr><td>03h</td><td>3 frame</td></tr> <tr><td>04h</td><td>4 frame</td></tr> <tr><td>05h</td><td>5 frame</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>FBh</td><td>251 frame</td></tr> <tr><td>FCh</td><td>252 frame</td></tr> <tr><td>FDh</td><td>253 frame</td></tr> <tr><td>FEh</td><td>254 frame</td></tr> <tr><td>FFh</td><td>255 frame</td></tr> </tbody> </table> <p>Thereby, total transition time for dimming can be calculated as follows:</p> <p>TT_STP [7:0] * ST_TIM [7:0] = TT, where TT unit is frame. Value 0000h means the transition is instant</p>											TT_STP [7:0]	Description	00h	1 step	01h	2 step	02h	4 step	03h	8 step	04h	16 step	05h	32 step	06h	64 step	07h	128 step	08h	256 step	09h	512 step	0Ah	1024 step	0Bh	2048 step	0Ch	4096 step	Others	Reserved	ST_TIM [7:0]	Description	00h	1 frame	01h	1 frame	02h	2 frame	03h	3 frame	04h	4 frame	05h	5 frame	:	:	:	:	FBh	251 frame	FCh	252 frame	FDh	253 frame	FEh	254 frame	FFh	255 frame
	TT_STP [7:0]	Description																																																																			
00h	1 step																																																																				
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04h	16 step																																																																				
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Status	Default Value								
Power On Sequence	00h_00h								
S/W Reset	00h_00h								
H/W Reset	00h_00h								
Flow Chart	<pre> graph TD A[SET TT] --> B[/TT_STP/] B --> C[/ST_TIM/] C --> D{{New TT setting loaded}} </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 								

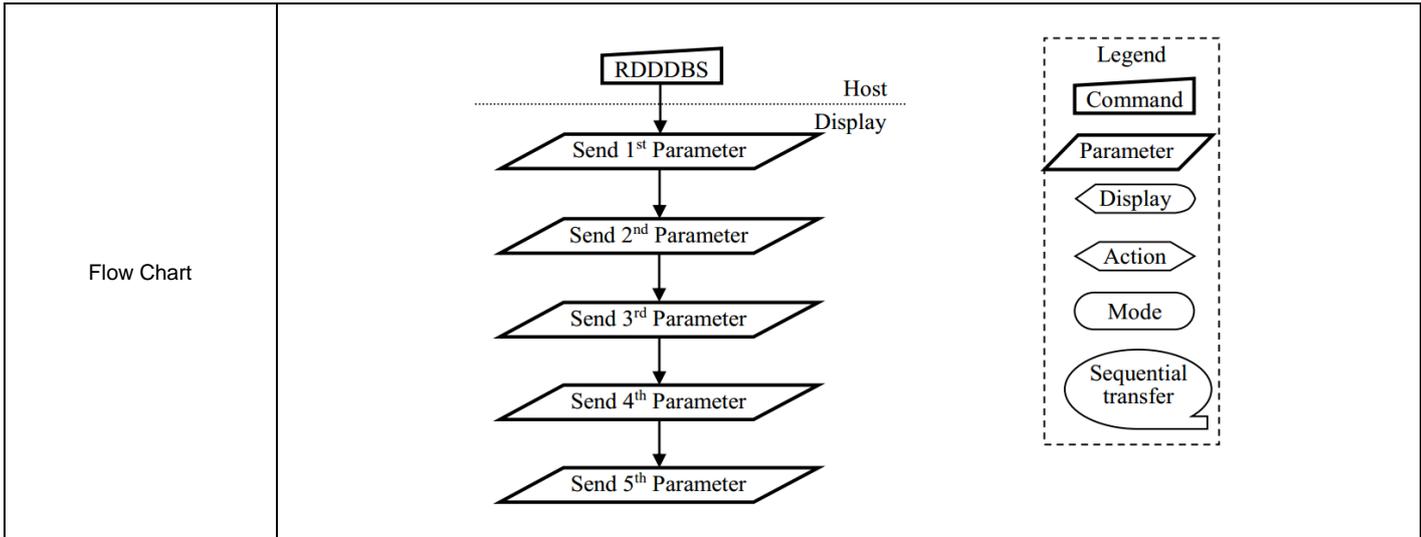
5.3.37. Get Transition Time (69h)

Command Page			Page 0																																																																		
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																																										
69h	1st	R	TT_STP[7:0]								00h																																																										
	2nd	R	ST_TIM[7:0]								00h																																																										
Description	<p>69h: GET_TT (Get Transition Time Value).</p> <p>This readout returns the Transition Time value of Display Dimming function, described in section "5.3.36Set Transition Time (68h)".</p> <p>Transition time is adjusted with two parameters, defining as follows:</p> <p>1st Parameter TT_STP [7:0] defines the number of dimming steps for transition.</p> <table border="1"> <thead> <tr> <th>TT_STP [7:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>00h</td><td>1 step</td></tr> <tr><td>01h</td><td>2 step</td></tr> <tr><td>02h</td><td>4 step</td></tr> <tr><td>03h</td><td>8 step</td></tr> <tr><td>04h</td><td>16 step</td></tr> <tr><td>05h</td><td>32 step</td></tr> <tr><td>06h</td><td>64 step</td></tr> <tr><td>07h</td><td>128 step</td></tr> <tr><td>08h</td><td>256 step</td></tr> <tr><td>09h</td><td>512 step</td></tr> <tr><td>0Ah</td><td>1024 step</td></tr> <tr><td>0Bh</td><td>2048 step</td></tr> <tr><td>0Ch</td><td>4096 step</td></tr> <tr><td>Others</td><td>Reserved</td></tr> </tbody> </table> <p>2nd Parameter ST_TIM [7:0] defines the step time as frame units for each dimming step.</p> <table border="1"> <thead> <tr> <th>ST_TIM [7:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>00h</td><td>1 frame</td></tr> <tr><td>01h</td><td>1 frame</td></tr> <tr><td>02h</td><td>2 frame</td></tr> <tr><td>03h</td><td>3 frame</td></tr> <tr><td>04h</td><td>4 frame</td></tr> <tr><td>05h</td><td>5 frame</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>FBh</td><td>251 frame</td></tr> <tr><td>FCh</td><td>252 frame</td></tr> <tr><td>FDh</td><td>253 frame</td></tr> <tr><td>FEh</td><td>254 frame</td></tr> <tr><td>FFh</td><td>255 frame</td></tr> </tbody> </table>											TT_STP [7:0]	Description	00h	1 step	01h	2 step	02h	4 step	03h	8 step	04h	16 step	05h	32 step	06h	64 step	07h	128 step	08h	256 step	09h	512 step	0Ah	1024 step	0Bh	2048 step	0Ch	4096 step	Others	Reserved	ST_TIM [7:0]	Description	00h	1 frame	01h	1 frame	02h	2 frame	03h	3 frame	04h	4 frame	05h	5 frame	:	:	:	:	FBh	251 frame	FCh	252 frame	FDh	253 frame	FEh	254 frame	FFh	255 frame
	TT_STP [7:0]	Description																																																																			
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Restriction	None																																																																				
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																																																		
Status	Availability																																																																				
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																																																				
Normal Mode On, Idle Mode On, Sleep Out	Yes																																																																				
Sleep In	Yes																																																																				

Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h_00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h_00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h_00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h_00h	S/W Reset	00h_00h	H/W Reset	00h_00h
Status	Default Value								
Power On Sequence	00h_00h								
S/W Reset	00h_00h								
H/W Reset	00h_00h								
Flow Chart	 <p>The flow chart illustrates the sequence of operations for the Read GET_TT command. It begins with a 'Read GET_TT' command box. Below this, a dashed horizontal line separates the 'Host' (top) from the 'Display' (bottom). The process continues with 'Send 1st Parameter' and 'Send 2nd Parameter', both represented by parallelogram shapes. A legend on the right side of the chart defines the symbols used: a rectangle for 'Command', a parallelogram for 'Parameter', a trapezoid for 'Display', an arrow for 'Action', an oval for 'Mode', and an oval with an arrow for 'Sequential transfer'.</p>								

5.3.38. Read DDB Start (A1h)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
A1h	1st	R	SID[7:0]								0000h								
	2nd	R	SID[15:8]																
	3rd	R	MRID[7:0]								0000h								
	4th	R	MRID[15:8]																
	5th	R	SID2[7:0]								0000h								
	6th	R	SID2[15:8]																
	7th	R	1	1	1	1	1	1	1	1	1	FFh							
Description	<p>A1h: RDDDBS (Read DDB Start).</p> <p>This command reads the supplier identification and display module mode/revision information.</p> <p><i>Note: This information is not the same as which "Read ID1 (DAh)", "Read ID2 (DBh)" and "Read ID3 (DCh)" commands return.</i></p> <p>Parameter 1: SID[7:0] LCD module's manufacturer ID.</p> <p>Parameter 2: SID[15:8] LCD module/driver version ID.</p> <p>Parameter 3: MRID[7:0] LCD module/driver ID.</p> <p>Parameter 4: MRID[15:8] IC version code.</p> <p>Parameter 5: SID2[7:0]</p> <p>Parameter 6: SID2[15:8]</p> <p>Parameter 7: FFh - Exit code – there is no more data in the Descriptor Block</p> <p>This read sequence can be interrupted by any command and it can be continued by the Read DDB Continue (A8h) command. For example, RDDDBS => 1st parameter has been sent => 2nd parameter has been sent => interrupt => RDDDBC => 3rd parameter of the RDDDBS has been sent.</p> <p><i>Note: Maximum DDB data length is 4 bytes with OTP program.</i></p>																		
Restriction	None																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h_00h_00h_00h_00h_00h_FFh</td> </tr> <tr> <td>S/W Reset</td> <td>00h_00h_00h_00h_00h_00h_FFh</td> </tr> <tr> <td>H/W Reset</td> <td>00h_00h_00h_00h_00h_00h_FFh</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h_00h_00h_00h_00h_00h_FFh	S/W Reset	00h_00h_00h_00h_00h_00h_FFh	H/W Reset	00h_00h_00h_00h_00h_00h_FFh
Status	Default Value																		
Power On Sequence	00h_00h_00h_00h_00h_00h_FFh																		
S/W Reset	00h_00h_00h_00h_00h_00h_FFh																		
H/W Reset	00h_00h_00h_00h_00h_00h_FFh																		



5.3.39. Read DDB Continue (A8h)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
A8h	1st	R	D1[7:0]								00h								
	2nd	R	D2[7:0]								00h								
	:	R	:								00h								
	Nth	R	Dn[7:0]								00h								
Description	A8h: RDDDBC (Read DDB Continue). This command is used to read the supplier's identification and revision information from the point where RDDDBS (A1h) was interrupted by another command																		
Restriction	None																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value																		
Power On Sequence	00h																		
S/W Reset	00h																		
H/W Reset	00h																		
Flow Chart																			

5.3.40. Read First Checksum (AAh)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
AAh	1st	R	FCS[7:0]									00h							
Description	AAh: RDFCS (Read First Checksum). This command returns the first checksum what has been calculated from Page 0 area registers after the write access to those registers has been done.																		
Restriction	It will be necessary to wait 150ms after there is the last write access on Page 0 area registers before there can read this checksum value.																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value																		
Power On Sequence	00h																		
S/W Reset	00h																		
H/W Reset	00h																		
Flow Chart	<div style="display: flex; align-items: center; justify-content: center;"> <div style="text-align: center; margin-right: 20px;"> <div style="border: 1px solid black; padding: 2px 5px; display: inline-block;">RDFCS</div> ↓ <div style="border: 1px solid black; padding: 2px 5px; display: inline-block;">Send FCS[7:0]</div> </div> <div style="text-align: center; margin-left: 20px;"> Host ----- Display </div> </div> <div style="margin-left: 20px;"> <p>Legend</p> <div style="border: 1px dashed black; padding: 5px; width: fit-content;"> <div style="border: 1px solid black; padding: 2px; display: inline-block; margin-bottom: 5px;">Command</div> <div style="border: 1px solid black; padding: 2px; display: inline-block; margin-bottom: 5px;">Parameter</div> <div style="border: 1px solid black; padding: 2px; display: inline-block; margin-bottom: 5px;">Display</div> <div style="border: 1px solid black; padding: 2px; display: inline-block; margin-bottom: 5px;">Action</div> <div style="border: 1px solid black; padding: 2px; display: inline-block; margin-bottom: 5px;">Mode</div> <div style="border: 1px solid black; padding: 2px; display: inline-block; margin-bottom: 5px;">Sequential transfer</div> </div> </div>																		

5.3.41. Read Continue Checksum (AFh)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
AFh	1st	R	CCS[7:0]								00h								
Description	AFh: RDCCS (Read Continue Checksum). This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from Page 0 area registers after the write access to those registers has been done.																		
Restriction	It will be necessary to wait 300ms after there is the last write access on Page 0 area registers before there can read this checksum value in the first time.																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value																		
Power On Sequence	00h																		
S/W Reset	00h																		
H/W Reset	00h																		
Flow Chart	<div style="display: flex; align-items: center; justify-content: center;"> <div style="text-align: center;"> <div style="border: 1px solid black; padding: 2px 5px; margin-bottom: 5px;">RDCCS</div> <div style="border-bottom: 1px dashed black; width: 100px; margin: 0 auto;"></div> <div style="border: 1px solid black; padding: 2px 5px; margin-bottom: 5px;">Send CCS[7:0]</div> <div style="border-bottom: 1px dashed black; width: 100px; margin: 0 auto;"></div> <div style="display: flex; justify-content: space-between; width: 100px;"> Host Display </div> </div> <div style="margin-left: 20px;"> <p>Legend</p> <div style="border: 1px dashed black; padding: 5px; width: fit-content;"> <div style="border: 1px solid black; width: 20px; height: 10px; margin-bottom: 5px;"></div> <div style="border: 1px solid black; width: 20px; height: 10px; transform: rotate(-45deg); margin-bottom: 5px;"></div> <div style="border: 1px solid black; width: 20px; height: 10px; border-radius: 5px; margin-bottom: 5px;"></div> <div style="border: 1px solid black; width: 20px; height: 10px; border-radius: 5px; margin-bottom: 5px;"></div> <div style="border: 1px solid black; width: 20px; height: 10px; border-radius: 5px; margin-bottom: 5px;"></div> <div style="border: 1px solid black; width: 20px; height: 10px; border-radius: 5px; margin-bottom: 5px;"></div> </div> </div> </div>																		

5.3.42. Read ID1 (DAh)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
DAh	1st	R	ID1[7:0]								00h								
Description	Dah: RDID1 (Read ID1). This read byte identifies the display module's manufacturer. The ID1[7:0] is programmed by the OTP function.																		
Restriction	None																		
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value																		
Power On Sequence	00h																		
S/W Reset	00h																		
H/W Reset	00h																		
Flow Chart	<div style="display: flex; align-items: center; justify-content: center;"> <div style="text-align: center; margin-right: 20px;"> <p>Read ID1</p> <p>↓</p> <p>Send Parameter</p> </div> <div style="border-top: 1px dashed black; padding-top: 5px;"> <p style="margin: 0;">Host</p> <p style="margin: 0;">Display</p> </div> </div> <div style="border: 1px dashed black; padding: 10px; margin-left: 20px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div>																		

5.3.43. Read ID2 (DBh)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
DBh	1st	R	ID2[7:0]								00h								
Description	<p>DBh: RDID2 (Read ID2).</p> <p>This read byte is used to track the display module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications.</p> <p>The ID2[7:0] is programmed by the OTP function.</p>																		
Restriction	None																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value																		
Power On Sequence	00h																		
S/W Reset	00h																		
H/W Reset	00h																		
Flow Chart	<p>The flow chart illustrates the communication between the Host and the Display. The Host initiates the process by sending a 'Read ID2' command to the Display. In response, the Display sends back a 'Send Parameter' parameter to the Host. A legend on the right side of the chart defines the symbols used: a rectangle for 'Command', a parallelogram for 'Parameter', a diamond for 'Display', an arrow for 'Action', an oval for 'Mode', and a speech bubble for 'Sequential transfer'.</p>																		

5.3.44. Read ID3 (DCh)

Command Page			Page 0																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
DCh	1st	R	ID3[7:0]								00h								
Description	DCh: RDID3 (Read ID3). This read byte identifies the display module/driver. The ID3[7:0] is programmed by the OTP function.																		
Restriction	None																		
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value																		
Power On Sequence	00h																		
S/W Reset	00h																		
H/W Reset	00h																		
Flow Chart	<div style="display: flex; align-items: center; justify-content: center;"> <div style="text-align: center; margin-right: 20px;"> <p>Read ID3</p> <p>↓</p> <p>Send Parameter</p> </div> <div style="text-align: center; margin-right: 20px;"> <p>Host</p> <p>-----</p> <p>Display</p> </div> <div style="border: 1px dashed black; padding: 5px;"> <p>Legend</p> <ul style="list-style-type: none"> Command: Parameter: Display: Action: Mode: Sequential transfer: </div> </div>																		

5.3.45. EXTC Command Set Enable Register (FFh)

Command Page			Page 0																																		
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																										
FFh	1st	W	1	0	0	1	1	0	0	0	98h																										
	2nd	W	1	0	0	0	0	0	0	1	81h																										
	3rd	W	PAGE[7:0]								00h																										
Description	<p>PAGE[7:0]: Set the command page.</p> <table border="1"> <thead> <tr> <th>PAGE[7:0]</th> <th>Command Page</th> </tr> </thead> <tbody> <tr><td>00h</td><td>Page 0</td></tr> <tr><td>01h</td><td>Page 1</td></tr> <tr><td>02h</td><td>Page 2</td></tr> <tr><td>03h</td><td>Page 3</td></tr> <tr><td>04h</td><td>Page 4</td></tr> <tr><td>05h</td><td>Page 5</td></tr> <tr><td>06h</td><td>Page 6</td></tr> <tr><td>07h</td><td>Page 7</td></tr> <tr><td>08h</td><td>Page 8</td></tr> <tr><td>09h</td><td>Page 9</td></tr> <tr><td>0Ah</td><td>Page 10</td></tr> <tr><td>Others</td><td>Reserved</td></tr> </tbody> </table> <p>Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available</p> <p>See section "5.1 Command Flow".</p>											PAGE[7:0]	Command Page	00h	Page 0	01h	Page 1	02h	Page 2	03h	Page 3	04h	Page 4	05h	Page 5	06h	Page 6	07h	Page 7	08h	Page 8	09h	Page 9	0Ah	Page 10	Others	Reserved
	PAGE[7:0]	Command Page																																			
	00h	Page 0																																			
	01h	Page 1																																			
	02h	Page 2																																			
	03h	Page 3																																			
	04h	Page 4																																			
	05h	Page 5																																			
	06h	Page 6																																			
	07h	Page 7																																			
	08h	Page 8																																			
	09h	Page 9																																			
	0Ah	Page 10																																			
Others	Reserved																																				
Restriction	None																																				
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																		
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Sleep In	Yes																																				
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h																		
Status	Default Value																																				
Power On Sequence	00h																																				
S/W Reset	00h																																				
H/W Reset	00h																																				

5.4. Page 1 Command Description

5.4.1. Read ID4 (00h~02h)

Command Page			Page 1																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
00h	1st	R	ID4[23:16]								98h								
01h	1st	R	ID4[15:8]								81h								
02h	1st	R	ID4[7:0]								5Ch								
Description		ID4[23:0] : mean the IC model name.																	
Restriction		None																	
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>98h_81h_5Ch</td> </tr> <tr> <td>S/W Reset</td> <td>98h_81h_5Ch</td> </tr> <tr> <td>H/W Reset</td> <td>98h_81h_5Ch</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	98h_81h_5Ch	S/W Reset	98h_81h_5Ch	H/W Reset	98h_81h_5Ch
Status	Default Value																		
Power On Sequence	98h_81h_5Ch																		
S/W Reset	98h_81h_5Ch																		
H/W Reset	98h_81h_5Ch																		

5.4.2. Set Panel Operation Mode and Data Complement Setting (22h)

Command Page		Page 1																																																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																							
22h	1st	W/R	0	0	EPF[1:0]		BGR_PA NEL	REV_PA NEL	SS_PAN EL	GS_PAN EL	30h																																							
Description	<p>This command defines the panel operation mode</p> <p>EPF[1:0]: Set the data format from 16/18-bit (R,G,B) to 24-bit (r, g, b) that is mapping into the internal circuit. See section “4.2.2 16/18-bit Color Data Mapping to 24-bit Pixel Data Operation” for detail description.</p> <p>BGR_PANEL:</p> <table border="1"> <thead> <tr> <th>Symbol</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>BGR_PANEL</td> <td>Panel RGB-BGR Order</td> <td>Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)</td> </tr> </tbody> </table> <p>REV_PANEL: Normally white or normally black panel select.</p> <table border="1"> <thead> <tr> <th>REV_PANEL</th> <th>Panel</th> <th>Data</th> <th>Color</th> <th>Source</th> </tr> </thead> <tbody> <tr> <td rowspan="2">0</td> <td rowspan="2">Normally black</td> <td>0x00</td> <td>Black</td> <td>Smallest gamma voltage</td> </tr> <tr> <td>0xFF</td> <td>White</td> <td>Largest gamma voltage</td> </tr> <tr> <td rowspan="2">1</td> <td rowspan="2">normally white</td> <td>0x00</td> <td>Black</td> <td>Largest gamma voltage</td> </tr> <tr> <td>0xFF</td> <td>White</td> <td>Smallest gamma voltage</td> </tr> </tbody> </table> <p>SS_PANEL: Select the shift direction of outputs from the source driver.</p> <table border="1"> <thead> <tr> <th>SS_PANEL</th> <th>Source Output Scan Direction</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Forward</td> </tr> <tr> <td>1</td> <td>Backward</td> </tr> </tbody> </table> <p>GS_PANEL: Select the shift direction of outputs from the gate driver.</p> <table border="1"> <thead> <tr> <th>GS_PANEL</th> <th>Gate Output Scan Direction</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Top → Bottom</td> </tr> <tr> <td>1</td> <td>Bottom → Top</td> </tr> </tbody> </table>											Symbol	Name	Description	BGR_PANEL	Panel RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)	REV_PANEL	Panel	Data	Color	Source	0	Normally black	0x00	Black	Smallest gamma voltage	0xFF	White	Largest gamma voltage	1	normally white	0x00	Black	Largest gamma voltage	0xFF	White	Smallest gamma voltage	SS_PANEL	Source Output Scan Direction	0	Forward	1	Backward	GS_PANEL	Gate Output Scan Direction	0	Top → Bottom	1	Bottom → Top
	Symbol	Name	Description																																															
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Status	Default Value (Before OTP program)																																																	
Power On Sequence	30h																																																	
S/W Reset	30h																																																	
H/W Reset	30h																																																	

5.4.3. Blanking Porch Control (25h~26h)

Command Page			Page 1																														
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																						
25h	1st	W/R	VFP[7:0]									14h																					
26h	1st	W/R	VBP[7:0]									14h																					
Description	<p>VFP[7:0] / VBP[7:0]: The VFP[7:0] and VBP[7:0] bits specify the line number of vertical front and back porch period respectively in the non-Video Mode.</p> <table border="1"> <thead> <tr> <th>VFP[7:0] VBP[7:0]</th> <th>Number of HSYNC of front/back porch (Dec.)</th> </tr> </thead> <tbody> <tr> <td>00000000</td> <td>Setting prohibited</td> </tr> <tr> <td>00000001</td> <td>Setting prohibited</td> </tr> <tr> <td>00000010</td> <td>2</td> </tr> <tr> <td>00000011</td> <td>3</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>00001110</td> <td>14 (VFP[7:0] /VBP[7:0] default)</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>11111101</td> <td>253</td> </tr> <tr> <td>11111110</td> <td>254</td> </tr> <tr> <td>11111111</td> <td>255</td> </tr> </tbody> </table>											VFP[7:0] VBP[7:0]	Number of HSYNC of front/back porch (Dec.)	00000000	Setting prohibited	00000001	Setting prohibited	00000010	2	00000011	3	:	:	00001110	14 (VFP[7:0] /VBP[7:0] default)	:	:	11111101	253	11111110	254	11111111	255
	VFP[7:0] VBP[7:0]	Number of HSYNC of front/back porch (Dec.)																															
	00000000	Setting prohibited																															
	00000001	Setting prohibited																															
	00000010	2																															
	00000011	3																															
	:	:																															
	00001110	14 (VFP[7:0] /VBP[7:0] default)																															
	:	:																															
	11111101	253																															
	11111110	254																															
	11111111	255																															
Restriction	None																																
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Sleep In	Yes																																
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>14h_14h</td> </tr> <tr> <td>S/W Reset</td> <td>14h_14h</td> </tr> <tr> <td>H/W Reset</td> <td>14h_14h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	14h_14h	S/W Reset	14h_14h	H/W Reset	14h_14h														
Status	Default Value																																
Power On Sequence	14h_14h																																
S/W Reset	14h_14h																																
H/W Reset	14h_14h																																

5.4.4. Touch Synchronization Control (29h)

Command Page			Page 1																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
29h	1st	W/R	0	0	0	0	0	0	0	TOUCH_VHSYNC	00h								
Description		TOUCH_VHSYNC: Enable VSOUT / HSOUT signal output.																	
Restriction		None																	
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value																		
Power On Sequence	00h																		
S/W Reset	00h																		
H/W Reset	00h																		

5.4.5. Gate Number (2Eh)

Command Page			Page 1																														
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																						
2Eh	1st	W/R	NL[7:0]								C8h																						
Description	<p>NL[7:0]: Set the number of lines to drive the LCD at an interval of 4 lines. The number of lines must be the same or more than the number of lines necessary for the size of the LCD panel.</p> <table border="1"> <thead> <tr> <th>NL[7:0]</th> <th>The Line Number of the LCD</th> </tr> </thead> <tbody> <tr><td>00h</td><td>480</td></tr> <tr><td>01h</td><td>484</td></tr> <tr><td>02h</td><td>488</td></tr> <tr><td>03h</td><td>492</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>C5h</td><td>1268</td></tr> <tr><td>C6h</td><td>1272</td></tr> <tr><td>C7h</td><td>1276</td></tr> <tr><td>C8h</td><td>1280</td></tr> <tr><td>Others</td><td>Reserved</td></tr> </tbody> </table>											NL[7:0]	The Line Number of the LCD	00h	480	01h	484	02h	488	03h	492	:	:	C5h	1268	C6h	1272	C7h	1276	C8h	1280	Others	Reserved
	NL[7:0]	The Line Number of the LCD																															
	00h	480																															
	01h	484																															
	02h	488																															
	03h	492																															
	:	:																															
	C5h	1268																															
	C6h	1272																															
	C7h	1276																															
C8h	1280																																
Others	Reserved																																
Restriction	None																																
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Normal Mode On, Idle Mode On, Sleep Out	Yes																																
Sleep In	Yes																																
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>C8h</td> </tr> <tr> <td>S/W Reset</td> <td>C8h</td> </tr> <tr> <td>H/W Reset</td> <td>C8h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	C8h	S/W Reset	C8h	H/W Reset	C8h														
Status	Default Value																																
Power On Sequence	C8h																																
S/W Reset	C8h																																
H/W Reset	C8h																																

5.4.6. Gate Number (2Fh)

Command Page			Page 1																							
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default															
2Fh	1st	W/R	Add_1024	0	0	0	0	0	0	Add_two	00h															
Description	<p>Add_1024: The line number add 1024</p> <p>Add_two: The line number add two</p> <table border="1"> <thead> <tr> <th>Add_1024</th> <th>Add_two</th> <th>The Line Number of the LCD</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>4NL+480</td> </tr> <tr> <td>0</td> <td>1</td> <td>4NL+480+2</td> </tr> <tr> <td>1</td> <td>0</td> <td>4NL+480+1024</td> </tr> <tr> <td>1</td> <td>1</td> <td>4NL+480+1024+2</td> </tr> </tbody> </table>											Add_1024	Add_two	The Line Number of the LCD	0	0	4NL+480	0	1	4NL+480+2	1	0	4NL+480+1024	1	1	4NL+480+1024+2
	Add_1024	Add_two	The Line Number of the LCD																							
	0	0	4NL+480																							
	0	1	4NL+480+2																							
	1	0	4NL+480+1024																							
1	1	4NL+480+1024+2																								
Restriction	None																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																									
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Status	Default Value																									
Power On Sequence	00h																									
S/W Reset	No change																									
H/W Reset	00h																									

Display Inversion Control (31h)

Command Page		Page 1																																																																																																																																																																																																															
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																																																																																																																																																																																						
31h	1st	W/R	0	0	0	0	DINV[3:0]				00h																																																																																																																																																																																																						
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5.4.7. Dithering Enable (34h)

Command Page			Page 1																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
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Description	DITH_EN: 0 : dithering function disable 1 : dithering function enable																		
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Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value																		
Power On Sequence	00h																		
S/W Reset	00h																		
H/W Reset	00h																		

5.4.8. Pump Clock Adjustment (40h~43h)

Command Page			Page 1																																																				
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																												
40h	1st	W/R	0	EXT_CPCK_SEL[1:0]		1	0	0	1	VGHL_CLK_EN	33h																																												
42h	1st	W/R	0	VGHL_CLK_SELA[2:0]			0	VGHL_CLK_SELB[2:0]			44h																																												
43h	1st	W/R	0	4002_RATIO_FREQA[2:0]			0	4002_RATIO_FREQB[2:0]			55h																																												
Description	<p>EXT_CPCK_SEL[1:0]: Pumping clock control signals selection to external control IC (ILI4003).Set the register before Sleep Out(R11h), when external pumping control be used.</p> <table border="1"> <thead> <tr> <th>EXT_CPCK_SEL[1:0]</th> <th>EXTP & EXTN Output</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Output x 1.5 waveform</td> </tr> <tr> <td>1h</td> <td>Output x 2 waveform</td> </tr> <tr> <td>2h</td> <td>Output x 3 waveform</td> </tr> <tr> <td>3h</td> <td>Output Low (power down)</td> </tr> </tbody> </table> <p>VGHL_CLK_EN: Enable the pumping cycle of step-up circuit of VGH and VGL.</p> <p>VGHL_CLK_SELA[2:0]: Selects the pumping cycle of step-up circuit of VGH and VGL in the Normal Mode.</p> <p>VGHL_CLK_SELB[2:0]: Selects the pumping cycle of step-up circuit of VGH and VGL in the Idle Mode.</p> <p>4002_RATIO_FREQA[2:0]: Selects the pumping cycle of step-up circuit of external control IC (ILI4003) in the Normal Mode.</p> <p>4002_RATIO_FREQB[2:0]: Selects the pumping cycle of step-up circuit of external control IC (ILI4003) in the Idle Mode.</p> <p>Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.</p> <table border="1"> <thead> <tr> <th>VGHL_CLK_SELA[2:0], VGHL_CLK_SELB[2:0]</th> <th>Pumping cycle</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>16H</td> </tr> <tr> <td>1h</td> <td>8H</td> </tr> <tr> <td>2h</td> <td>4H</td> </tr> <tr> <td>3h</td> <td>2H</td> </tr> <tr> <td>4h</td> <td>1H</td> </tr> <tr> <td>5h</td> <td>1/2H</td> </tr> <tr> <td>Others</td> <td>Reserved</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th>4002_RATIO_FREQA[2:0], 4002_RATIO_FREQB[2:0]</th> <th>Pumping cycle</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>16H</td> </tr> <tr> <td>1h</td> <td>8H</td> </tr> <tr> <td>2h</td> <td>4H</td> </tr> <tr> <td>3h</td> <td>2H</td> </tr> <tr> <td>4h</td> <td>1H</td> </tr> <tr> <td>5h</td> <td>1/2H</td> </tr> <tr> <td>6h</td> <td>1/4H</td> </tr> <tr> <td>7h</td> <td>1/8H</td> </tr> </tbody> </table>											EXT_CPCK_SEL[1:0]	EXTP & EXTN Output	0h	Output x 1.5 waveform	1h	Output x 2 waveform	2h	Output x 3 waveform	3h	Output Low (power down)	VGHL_CLK_SELA[2:0], VGHL_CLK_SELB[2:0]	Pumping cycle	0h	16H	1h	8H	2h	4H	3h	2H	4h	1H	5h	1/2H	Others	Reserved	4002_RATIO_FREQA[2:0], 4002_RATIO_FREQB[2:0]	Pumping cycle	0h	16H	1h	8H	2h	4H	3h	2H	4h	1H	5h	1/2H	6h	1/4H	7h	1/8H
	EXT_CPCK_SEL[1:0]	EXTP & EXTN Output																																																					
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4002_RATIO_FREQA[2:0], 4002_RATIO_FREQB[2:0]	Pumping cycle																																																						
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6h	1/4H																																																						
7h	1/8H																																																						
Restriction	None																																																						

<p>Register Availability</p>	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability								
Normal Mode On, Idle Mode Off, Sleep Out	Yes								
Normal Mode On, Idle Mode On, Sleep Out	Yes								
Sleep In	Yes								
<p>Default</p>	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>33h_44h_55h</td> </tr> <tr> <td>S/W Reset</td> <td>33h_44h_55h</td> </tr> <tr> <td>H/W Reset</td> <td>33h_44h_55h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	33h_44h_55h	S/W Reset	33h_44h_55h	H/W Reset	33h_44h_55h
Status	Default Value								
Power On Sequence	33h_44h_55h								
S/W Reset	33h_44h_55h								
H/W Reset	33h_44h_55h								

5.4.9. Power Control 1 (50h~51h)

Command Page			Page 1																																																																														
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																																																						
50h	1st	W/R	VREG1[7:0]									95h																																																																					
51h	1st	W/R	VREG2[7:0]									95h																																																																					
Description	<p>VREG1[7:0]: Set the VREG1OUT voltage for positive Gamma. (12mV/step)</p> <table border="1"> <thead> <tr> <th>VREG1[7:0]</th> <th>VREG1OUT voltage (V)</th> </tr> </thead> <tbody> <tr><td>42h</td><td>3.504</td></tr> <tr><td>43h</td><td>3.516</td></tr> <tr><td>44h</td><td>3.528</td></tr> <tr><td>45h</td><td>3.540</td></tr> <tr><td>46h</td><td>3.552</td></tr> <tr><td>47h</td><td>3.564</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>94h</td><td>4.488</td></tr> <tr><td>95h</td><td>4.500</td></tr> <tr><td>96h</td><td>4.512</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>E8h</td><td>5.496</td></tr> <tr><td>E9h</td><td>5.508</td></tr> <tr><td>EAh</td><td>5.520</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>EFh</td><td>5.580</td></tr> <tr><td>F0h</td><td>5.592</td></tr> <tr><td>F1h</td><td>5.604</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>08h</td><td>5.628</td></tr> <tr><td>09h</td><td>5.640</td></tr> <tr><td>0Ah</td><td>5.652</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>0Dh</td><td>5.688</td></tr> <tr><td>0Eh</td><td>5.700</td></tr> <tr><td>0Fh</td><td>5.712</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>12h</td><td>5.748</td></tr> <tr><td>13h</td><td>5.760</td></tr> <tr><td>14h</td><td>5.772</td></tr> <tr><td>15h</td><td>5.784</td></tr> <tr><td>16h</td><td>5.796</td></tr> <tr><td>17h</td><td>5.808</td></tr> <tr><td>Other</td><td>Reserved</td></tr> </tbody> </table>											VREG1[7:0]	VREG1OUT voltage (V)	42h	3.504	43h	3.516	44h	3.528	45h	3.540	46h	3.552	47h	3.564	:	:	94h	4.488	95h	4.500	96h	4.512	:	:	E8h	5.496	E9h	5.508	EAh	5.520	:	:	EFh	5.580	F0h	5.592	F1h	5.604	:	:	08h	5.628	09h	5.640	0Ah	5.652	:	:	0Dh	5.688	0Eh	5.700	0Fh	5.712	:	:	12h	5.748	13h	5.760	14h	5.772	15h	5.784	16h	5.796	17h	5.808	Other	Reserved
	VREG1[7:0]	VREG1OUT voltage (V)																																																																															
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17h	5.808																																																																																
Other	Reserved																																																																																

VREG2[7:0]: Set the VREG2OUT voltage for negative Gamma. (12mV/step)

VREG2[7:0]	VREG2OUT voltage (V)
42h	-3.564
43h	-3.576
44h	-3.588
45h	-3.600
46h	-3.612
47h	-3.624
:	:
94h	-4.548
95h	-4.560
96h	-4.572
:	:
E8h	-5.556
E9h	-5.568
EAh	-5.580
:	:
EFh	-5.640
F0h	-5.652
F1h	-5.664
:	:
08h	-5.688
09h	-5.700
0Ah	-5.712
:	:
0Dh	-5.748
0Eh	-5.760
0Fh	-5.772
:	:
12h	-5.808
13h	-5.820
14h	-5.832
15h	-5.844
16h	-5.856
17h	-5.868
Other	Reserved

Restriction	None

<p>Register Availability</p>	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability								
Normal Mode On, Idle Mode Off, Sleep Out	Yes								
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Sleep In	Yes								
<p>Default</p>	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>95h_95h</td> </tr> <tr> <td>S/W Reset</td> <td>95h_95h</td> </tr> <tr> <td>H/W Reset</td> <td>95h_95h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	95h_95h	S/W Reset	95h_95h	H/W Reset	95h_95h
Status	Default Value								
Power On Sequence	95h_95h								
S/W Reset	95h_95h								
H/W Reset	95h_95h								

VCOM Control 1 (52h~56h)

Command Page			Page 1																																												
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																				
52h	1st	W/R	0	0	0	0	0	0	0	VCM1[8]	00h																																				
53h	1st	W/R	VCM1[7:0]									7Bh																																			
54h	1st	W/R	0	0	0	0	0	0	0	VCM2[8]	00h																																				
55h	1st	W/R	VCM2[7:0]									7Bh																																			
56h	1st	R	0	0	0	NVM2	0	0	0	NVM1	00h																																				
Description	<p>VCM1[8:0]: Set the VCOM level used for vertical forward scan (GS_PANEL= 1'b0), when NV memory isn't programmed. (12mV/step)</p> <p>VCM2[8:0]: Set the VCOM level used for vertical backward scan (GS_PANEL= 1'b1), when NV memory isn't programmed. (12mV/step)</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>VCM1[8:0] VCM2[8:0]</th> <th>VCOM voltage (V)</th> </tr> </thead> <tbody> <tr><td>010h</td><td>-0.204</td></tr> <tr><td>011h</td><td>-0.216</td></tr> <tr><td>012h</td><td>-0.228</td></tr> <tr><td>013h</td><td>-0.24</td></tr> <tr><td>014h</td><td>-0.252</td></tr> <tr><td>015h</td><td>-0.264</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>07Ah</td><td>-1.476</td></tr> <tr><td>07Bh</td><td>-1.488</td></tr> <tr><td>07Ch</td><td>-1.5</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>149h</td><td>-3.96</td></tr> <tr><td>14Ah</td><td>-3.972</td></tr> <tr><td>14Bh</td><td>-3.984</td></tr> <tr><td>14Ch</td><td>-3.996</td></tr> <tr><td>14Dh</td><td>-4.008</td></tr> <tr><td>Others</td><td>Reserved</td></tr> </tbody> </table> <p><i>Note: VCOM ≥ VSN + 0.5V</i></p> <p>NVM1 : Selection of the VCM source setting used for vertical forward scan (GS_PANEL= 1'b0). When the NV memory is programmed, the NVM1 will be set as '1' automatically.</p> <p>0 : Register Page 1 R52h and R53h for VCM setting</p> <p>1 : Register Page 4 RC4h and RC5h for VCM setting</p> <p>NVM2 : Selection of the VCM source setting used for vertical backward scan (GS_PANEL= 1'b1). When the NV memory is programmed, the NVM2 will be set as '1' automatically.</p> <p>0 : Register 54h and 55h for VCM setting</p> <p>1 : Register Page 4 RC6h and RC7h for VCM setting</p> <p>Note : If 1-byte program , VCOM OTP program address is register pg1_cmd_52h~55h, If auto program, VCOM OTP program address is register pg4_cmd_C4h~C7h,</p>											VCM1[8:0] VCM2[8:0]	VCOM voltage (V)	010h	-0.204	011h	-0.216	012h	-0.228	013h	-0.24	014h	-0.252	015h	-0.264	:	:	07Ah	-1.476	07Bh	-1.488	07Ch	-1.5	:	:	149h	-3.96	14Ah	-3.972	14Bh	-3.984	14Ch	-3.996	14Dh	-4.008	Others	Reserved
	VCM1[8:0] VCM2[8:0]	VCOM voltage (V)																																													
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	07Bh	-1.488																																													
	07Ch	-1.5																																													
	:	:																																													
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	14Ah	-3.972																																													
14Bh	-3.984																																														
14Ch	-3.996																																														
14Dh	-4.008																																														
Others	Reserved																																														
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Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability								
	Normal Mode On, Idle Mode Off, Sleep Out	Yes								
	Normal Mode On, Idle Mode On, Sleep Out	Yes								
Sleep In	Yes									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h_7Bh_00h_7Bh_00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h_7Bh_00h_7Bh_00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h_7Bh_00h_7Bh_00h</td> </tr> </tbody> </table>		Status	Default Value	Power On Sequence	00h_7Bh_00h_7Bh_00h	S/W Reset	00h_7Bh_00h_7Bh_00h	H/W Reset	00h_7Bh_00h_7Bh_00h
	Status	Default Value								
	Power On Sequence	00h_7Bh_00h_7Bh_00h								
	S/W Reset	00h_7Bh_00h_7Bh_00h								
H/W Reset	00h_7Bh_00h_7Bh_00h									

5.4.10. Entry Mode Set (58h)

Command Page			Page 1																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
58h	1st	W/R	LVD_EN	0	0	0	0	0	0	0	00h								
Description	LVD_EN: Low voltage detection control.																		
	<table border="1"> <thead> <tr> <th>LVD</th> <th>Low voltage detection</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Enable</td> </tr> <tr> <td>1</td> <td>Disable</td> </tr> </tbody> </table>											LVD	Low voltage detection	0	Enable	1	Disable		
LVD	Low voltage detection																		
0	Enable																		
1	Disable																		
Restriction																			
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
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Status	Default Value																		
Power On Sequence	00h																		
S/W Reset	00h																		
H/W Reset	00h																		

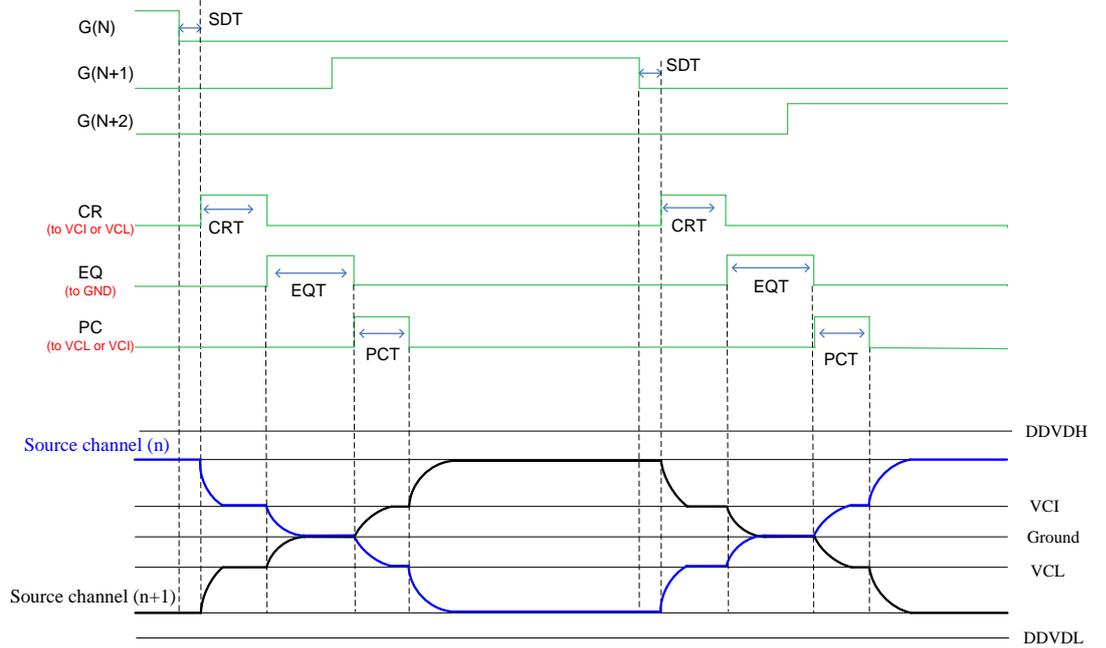
5.4.11. Source Timing Adjust (60h~63h)

Command Page			Page 1								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
60h	1st	W/R	0	0	SDT[5:0]						14h
61h	1st	W/R	0	0	CRT[5:0]						00h
62h	1st	W/R	0	0	EQT[5:0]						19h
63h	1st	W/R	0	0	PCT[5:0]						10h

SDT[5:0]: Source SD timing adjustment (time scale: internal T_{OP_CLK}). The timing can be adjusted 0 to 63 time scales.
CRT[5:0]: Source CR timing adjustment (time scale: internal T_{OP_CLK}). The timing can be adjusted 0 to 63 time scales.
EQT[5:0]: Source EQ timing adjustment (time scale: internal T_{OP_CLK}). The timing can be adjusted 8 to 71 time scales.
PCT[5:0]: Source PC timing adjustment (time scale: internal T_{OP_CLK}). The timing can be adjusted 0 to 63 time scales.

Note: T_{OP_CLK} : 62.5ns

Description



Restriction	None
-------------	------

Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability							
	Normal Mode On, Idle Mode Off, Sleep Out	Yes							
	Normal Mode On, Idle Mode On, Sleep Out	Yes							
Sleep In	Yes								

Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>14h_00h_19h_10h</td> </tr> <tr> <td>S/W Reset</td> <td>14h_00h_19h_10h</td> </tr> <tr> <td>H/W Reset</td> <td>14h_00h_19h_10h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	14h_00h_19h_10h	S/W Reset	14h_00h_19h_10h	H/W Reset	14h_00h_19h_10h
	Status	Default Value							
	Power On Sequence	14h_00h_19h_10h							
	S/W Reset	14h_00h_19h_10h							
H/W Reset	14h_00h_19h_10h								

5.4.12. Positive Gamma Correction (A0h~B3h)

Command Page			Page 1																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
A0h	1st	W/R	0	0	VP0[5:0]						00h								
A1h	1st	W/R	0	VP4[6:0]						0Dh									
A2h	1st	W/R	0	VP8[6:0]						1Dh									
A3h	1st	W/R	0	0	VP12[5:0]						11h								
A4h	1st	W/R	0	0	VP16[5:0]						0Ch								
A5h	1st	W/R	0	VP24[6:0]						23h									
A6h	1st	W/R	0	0	VP36[5:0]						17h								
A7h	1st	W/R	0	0	VP52[5:0]						1Ch								
A8h	1st	W/R	VP80[7:0]								82h								
A9h	1st	W/R	0	0	VP111[5:0]						21h								
AAh	1st	W/R	0	0	VP144[5:0]						2Ah								
ABh	1st	W/R	VP175[7:0]								6Bh								
ACh	1st	W/R	0	0	VP203[5:0]						19h								
ADh	1st	W/R	0	0	VP219[5:0]						14h								
A Eh	1st	W/R	0	VP231[6:0]						45h									
AFh	1st	W/R	0	0	VP239[5:0]						1Dh								
B0h	1st	W/R	0	0	VP243[5:0]						23h								
B1h	1st	W/R	0	VP247[6:0]						52h									
B2h	1st	W/R	0	VP251[6:0]						63h									
B3h	1st	W/R	0	0	VP255[5:0]						39h								
Description		Set the gray scale voltage to adjust the Gamma characteristics of the TFT panel.																	
Restriction		None																	
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h_2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h</td> </tr> <tr> <td>S/W Reset</td> <td>00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h_2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h</td> </tr> <tr> <td>H/W Reset</td> <td>00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h_2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h_2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h	S/W Reset	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h_2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h	H/W Reset	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h_2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h
Status	Default Value																		
Power On Sequence	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h_2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h																		
S/W Reset	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h_2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h																		
H/W Reset	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h_2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h																		

5.4.13. Pad Control (B6h~B7h)

Command Page			Page 1																																																																																																							
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																																																																															
B6h	1st	W/R	IM_SW_EN	IM_SW[2:0]			RS_SW_EN	0	RS_SW[1:0]		00h																																																																																															
B7h	1st	W/R	0	0	0	0	0	0	LANSEL_SW_EN	LANSEL_SW	00h																																																																																															
Description	<p>IM_SW_EN: Enable/Disable the lane sequence and polarity from internal command setting. The external hardware pin IM[2:0] has no effect when IM_SW_EN is "1".</p> <p>IM_SW[2:0]: Set the configuration of lane sequence and polarity. (The bottom table is an example for MIPI 4 lane setting)</p> <table border="1"> <thead> <tr> <th colspan="3">Internal Pad Control</th> <th colspan="5">Configuration of MIPI Lane</th> </tr> <tr> <th>IM_SW2</th> <th>IM_SW1</th> <th>IM_SW0</th> <th>D0P/N Pin</th> <th>D1P/N Pin</th> <th>CLKP/N Pin</th> <th>D2P/N Pin</th> <th>D3P/N Pin</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>D3P/N</td><td>D2P/N</td><td>CLKP/N</td><td>D1P/N</td><td>D0P/N</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>D3N/P</td><td>D2N/P</td><td>CLKN/P</td><td>D1N/P</td><td>D0N/P</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>D0P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D2P/N</td><td>D3P/N</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>D0N/P</td><td>D1N/P</td><td>CLKN/P</td><td>D2N/P</td><td>D3N/P</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>D3P/N</td><td>D0P/N</td><td>CLKP/N</td><td>D1P/N</td><td>D2P/N</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>D3N/P</td><td>D0N/P</td><td>CLKN/P</td><td>D1N/P</td><td>D2N/P</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>D2P/N</td><td>D1P/N</td><td>CLKP/N</td><td>D0P/N</td><td>D3P/N</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>D2N/P</td><td>D1N/P</td><td>CLKN/P</td><td>D0N/P</td><td>D3N/P</td></tr> </tbody> </table> <p>RS_SW_EN: Enable/Disable the resolution from internal command setting. The external hardware pin RS[1:0] has no effect when RS_SW_EN is "1".</p> <p>RS_SW[1:0]: Set the resolution.</p> <table border="1"> <thead> <tr> <th>RS_SW1</th> <th>RS_SW0</th> <th>Resolution</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>800 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line</td></tr> <tr><td>0</td><td>1</td><td>768 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line</td></tr> <tr><td>1</td><td>0</td><td>720 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line</td></tr> <tr><td>1</td><td>1</td><td>640 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line</td></tr> </tbody> </table> <p>LANSEL_SW_EN: Enable/Disable the lane number from internal command setting. The external hardware pin LANSEL has no effect when LANSEL_SW_EN is "1".</p> <p>LANSEL_SW: Set the lane number. LANSEL_SW="1", MIPI DSI is 2 Lane mode LANSEL_SW="0", MIPI DSI is 3 or 4 Lane mode <i>Note: Please reference "Table 2: DSI Interface Lane Mode Selection"</i></p>											Internal Pad Control			Configuration of MIPI Lane					IM_SW2	IM_SW1	IM_SW0	D0P/N Pin	D1P/N Pin	CLKP/N Pin	D2P/N Pin	D3P/N Pin	0	0	0	D3P/N	D2P/N	CLKP/N	D1P/N	D0P/N	0	0	1	D3N/P	D2N/P	CLKN/P	D1N/P	D0N/P	0	1	0	D0P/N	D1P/N	CLKP/N	D2P/N	D3P/N	0	1	1	D0N/P	D1N/P	CLKN/P	D2N/P	D3N/P	1	0	0	D3P/N	D0P/N	CLKP/N	D1P/N	D2P/N	1	0	1	D3N/P	D0N/P	CLKN/P	D1N/P	D2N/P	1	1	0	D2P/N	D1P/N	CLKP/N	D0P/N	D3P/N	1	1	1	D2N/P	D1N/P	CLKN/P	D0N/P	D3N/P	RS_SW1	RS_SW0	Resolution	0	0	800 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line	0	1	768 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line	1	0	720 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line	1	1	640 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line
	Internal Pad Control			Configuration of MIPI Lane																																																																																																						
	IM_SW2	IM_SW1	IM_SW0	D0P/N Pin	D1P/N Pin	CLKP/N Pin	D2P/N Pin	D3P/N Pin																																																																																																		
	0	0	0	D3P/N	D2P/N	CLKP/N	D1P/N	D0P/N																																																																																																		
	0	0	1	D3N/P	D2N/P	CLKN/P	D1N/P	D0N/P																																																																																																		
	0	1	0	D0P/N	D1P/N	CLKP/N	D2P/N	D3P/N																																																																																																		
	0	1	1	D0N/P	D1N/P	CLKN/P	D2N/P	D3N/P																																																																																																		
	1	0	0	D3P/N	D0P/N	CLKP/N	D1P/N	D2P/N																																																																																																		
	1	0	1	D3N/P	D0N/P	CLKN/P	D1N/P	D2N/P																																																																																																		
	1	1	0	D2P/N	D1P/N	CLKP/N	D0P/N	D3P/N																																																																																																		
1	1	1	D2N/P	D1N/P	CLKN/P	D0N/P	D3N/P																																																																																																			
RS_SW1	RS_SW0	Resolution																																																																																																								
0	0	800 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line																																																																																																								
0	1	768 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line																																																																																																								
1	0	720 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line																																																																																																								
1	1	640 (RGB) x (1024(option) + 480 + (4 x NL) + 2(option)) gate line																																																																																																								
Restriction																																																																																																										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Sleep In</td><td>Yes</td></tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																																																																																							
Status	Availability																																																																																																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																																																																																									
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Sleep In	Yes																																																																																																									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr><td>Power On Sequence</td><td>00h_00h</td></tr> <tr><td>S/W Reset</td><td>00h_00h</td></tr> <tr><td>H/W Reset</td><td>00h_00h</td></tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h_00h	S/W Reset	00h_00h	H/W Reset	00h_00h																																																																																							
Status	Default Value																																																																																																									
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S/W Reset	00h_00h																																																																																																									
H/W Reset	00h_00h																																																																																																									

5.4.14. Negative Gamma Correction (C0h~D3h)

Command Page			Page 1																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
C0h	1st	W/R	0	0	VN0[5:0]						00h								
C1h	1st	W/R	0	VN4[6:0]						0Dh									
C2h	1st	W/R	0	VN8[6:0]						1Dh									
C3h	1st	W/R	0	0	VN12[5:0]						11h								
C4h	1st	W/R	0	0	VN16[5:0]						0Ch								
C5h	1st	W/R	0	VN24[6:0]						23h									
C6h	1st	W/R	0	0	VN36[5:0]						17h								
C7h	1st	W/R	0	0	VN52[5:0]						1Ch								
C8h	1st	W/R	VN80[7:0]						82h										
C9h	1st	W/R	0	0	VN111[5:0]						21h								
CAh	1st	W/R	0	0	VN144[5:0]						2Ah								
CBh	1st	W/R	VN175[7:0]						6Bh										
CCh	1st	W/R	0	0	VN203[5:0]						19h								
CDh	1st	W/R	0	0	VN219[5:0]						14h								
CEh	1st	W/R	0	VN231[6:0]						45h									
CFh	1st	W/R	0	0	VN239[5:0]						1Dh								
D0h	1st	W/R	0	0	VN243[5:0]						23h								
D1h	1st	W/R	0	VN247[6:0]						52h									
D2h	1st	W/R	0	VN251[6:0]						63h									
D3h	1st	W/R	0	0	VN255[5:0]						39h								
Description		Set the gray scale voltage to adjust the Gamma characteristics of the TFT panel.																	
Restriction		None																	
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h_2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h</td> </tr> <tr> <td>S/W Reset</td> <td>00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h_2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h</td> </tr> <tr> <td>H/W Reset</td> <td>00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h_2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h_2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h	S/W Reset	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h_2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h	H/W Reset	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h_2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h
Status	Default Value																		
Power On Sequence	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h_2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h																		
S/W Reset	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h_2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h																		
H/W Reset	00h_0Dh_1Dh_11h_0Ch_23h_17h_1Ch_82h_21h_2Ah_6Bh_19h_14h_45h_1Dh_23h_52h_63h_39h																		

5.4.15. NV Memory Write (E0h~E2h)

Command Page			Page 1										
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default		
E0h	1st	W/R	PGM_DATA[7:0]									00h	
E1h	1st	W/R	PGM_ADR[7:0]									00h	
E2h	1st	W/R	PGM_ADR[15:8]									00h	
Description	<p>This command is used to program or read the NV memory data.</p> <p>After a successful OTP operation, the information of PGM_DATA[7:0] will be programmed to the NV memory.</p> <p>PGM_DATA[7:0]: The programmed data.</p> <p>PGM_ADR[15:0]: Set the address of the NV memory for programming data. See chapter 14 "NV Memory Programming Flow".</p>												
				PGM_ADR[15:0]		Programming data							
				1h		ID1							
				2h		ID2							
				3h		ID3							
				4h		VCM1[8]							
				5h		VCM1[7:0]							
				6h		VCM2[8]							
				7h		VCM2[7:0]							
				8h		VREG1[7:0]							
				9h		VREG2[7:0]							
				68h~7Bh		REGAM0_P~ REGAM255_P							
			7Ch~8Fh		REGAM0_N~ REGAM255_N								
Restriction	None												
Register Availability				Status				Availability					
				Normal Mode On, Idle Mode Off, Sleep Out				Yes					
				Normal Mode On, Idle Mode On, Sleep Out				Yes					
				Sleep In				Yes					
Default				Status		Default Value							
				Power On Sequence		00h_00h_00h							
				S/W Reset		00h_00h_00h							
				H/W Reset		00h_00h_00h							

5.4.16. NV Memory Protection Key (E3h~E5h)

Command Page			Page 1																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
E3h	1st	W/R	KEY[23:16]									00h							
E4h	1st	W/R	KEY[15:8]									00h							
E5h	1st	W/R	KEY[7:0]									00h							
Description	<p>KEY[23:0]: NV memory programming protection key.</p> <p>Write an OTP data to PGM_DATA[7:0], this KEY[23:0] must set 0x55AA66h to enable OTP programming. If the KEY[23:0] is not 0x55AA66h, the NV Memory program will be aborted.</p>																		
Restriction	None																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
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Status	Default Value																		
Power On Sequence	00h_00h_00h																		
S/W Reset	00h_00h_00h																		
H/W Reset	00h_00h_00h																		

5.4.17. NV Memory Status Read (E6h~E9h)

Command Page			Page 1																																																																																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																																																								
E6h	1st	R	0	ID2_MK[2:0]			0	ID1_MK[2:0]			00h																																																																								
E7h	1st	R	0	0	0	0	0	ID3_MK[2:0]			00h																																																																								
E8h	1st	R	GAMMA P_MK	GAMMA N_MK	VCM2_MK[2:0]			VCM1_MK[2:0]			00h																																																																								
E9h	1st	R	OTP_BU SY	0	0	0	0	0	0	0	00h																																																																								
Description	<p>These registers uses a mark to record the NV memory programmed time. The bits are increase "+1" automatically after writing the PGM_DATA [7:0] to the NV memory.</p> <p>ID1_MK[2:0]/ID2_MK[2:0]:</p> <table border="1"> <thead> <tr> <th colspan="3">ID1_MK[2:0] / ID2_MK[2:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>No Programmed</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Programmed 1 time already</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Programmed 2 times already</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Programmed 3 times already</td> </tr> </tbody> </table> <p>ID3_MK[2:0]:</p> <table border="1"> <thead> <tr> <th colspan="3">ID3_MK[2:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>No Programmed</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Programmed 1 time already</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Programmed 2 times already</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Programmed 3 times already</td> </tr> </tbody> </table> <p>VCM1_MK[2:0] / VCM2_MK[2:0]:</p> <table border="1"> <thead> <tr> <th colspan="3">VCM1_MK[2:0] / VCM2_MK[2:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>No Programmed</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>Programmed 1 time already</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>Programmed 2 times already</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Programmed 3 times already</td> </tr> </tbody> </table> <p>GAMP_MK / GAMN_MK :</p> <table border="1"> <thead> <tr> <th>GAMP_MK / GAMN_MK</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>No Programmed</td> </tr> <tr> <td>1</td> <td>Programmed 1 time already</td> </tr> </tbody> </table> <p>OTP BUSY: The status bit of the NV memory programming.</p> <table border="1"> <thead> <tr> <th>OTP_BUSY</th> <th>The Status of NV Memory</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Idle</td> </tr> <tr> <td>1</td> <td>Busy</td> </tr> </tbody> </table>											ID1_MK[2:0] / ID2_MK[2:0]			Description	0	0	0	No Programmed	0	0	1	Programmed 1 time already	0	1	1	Programmed 2 times already	1	1	1	Programmed 3 times already	ID3_MK[2:0]			Description	0	0	0	No Programmed	0	0	1	Programmed 1 time already	0	1	1	Programmed 2 times already	1	1	1	Programmed 3 times already	VCM1_MK[2:0] / VCM2_MK[2:0]			Description	0	0	0	No Programmed	0	0	1	Programmed 1 time already	0	1	1	Programmed 2 times already	1	1	1	Programmed 3 times already	GAMP_MK / GAMN_MK	Description	0	No Programmed	1	Programmed 1 time already	OTP_BUSY	The Status of NV Memory	0	Idle	1	Busy
	ID1_MK[2:0] / ID2_MK[2:0]			Description																																																																															
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	Status	Default Value							
	Power On Sequence	00h_00h_00h_00h							
	S/W Reset	00h_00h_00h_00h							
H/W Reset	00h_00h_00h_00h								

5.4.18. Time Stamp (F0h~F1h)

Command Page			Page 1																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
F0h	1st	W/R	Time_Stamp_Week[7:0]								00h								
F1h	1st	W/R	Time_Stamp_Year[7:0]								00h								
Description	<p>This command identifies the display module's manufacture date</p> <p>Time_Stamp_Week[7:0]: Week of manufacture.</p> <p>Time_Stamp_Year[7:0]: Year of manufacture.</p>																		
Restriction																			
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
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Status	Default Value																		
Power On Sequence	00h_00h																		
S/W Reset	00h_00h																		
H/W Reset	00h_00h																		

5.4.19. EXTC Command Set Enable Register (FFh)

Command Page			Page 1																																		
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																										
FFh	1st	W	1	0	0	1	1	0	0	0	98h																										
	2nd	W	1	0	0	0	0	0	0	1	81h																										
	3rd	W	PAGE[7:0]								01h																										
Description	<p>PAGE[7:0]: Set the command page.</p> <table border="1"> <thead> <tr> <th>PAGE[7:0]</th> <th>Command Page</th> </tr> </thead> <tbody> <tr><td>00h</td><td>Page 0</td></tr> <tr><td>01h</td><td>Page 1</td></tr> <tr><td>02h</td><td>Page 2</td></tr> <tr><td>03h</td><td>Page 3</td></tr> <tr><td>04h</td><td>Page 4</td></tr> <tr><td>05h</td><td>Page 5</td></tr> <tr><td>06h</td><td>Page 6</td></tr> <tr><td>07h</td><td>Page 7</td></tr> <tr><td>08h</td><td>Page 8</td></tr> <tr><td>09h</td><td>Page 9</td></tr> <tr><td>0Ah</td><td>Page 10</td></tr> <tr><td>Others</td><td>Reserved</td></tr> </tbody> </table> <p>Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available</p> <p>See section "5.1 Command Flow".</p>											PAGE[7:0]	Command Page	00h	Page 0	01h	Page 1	02h	Page 2	03h	Page 3	04h	Page 4	05h	Page 5	06h	Page 6	07h	Page 7	08h	Page 8	09h	Page 9	0Ah	Page 10	Others	Reserved
	PAGE[7:0]	Command Page																																			
	00h	Page 0																																			
	01h	Page 1																																			
	02h	Page 2																																			
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Status	Default Value																																				
Power On Sequence	01h																																				
S/W Reset	01h																																				
H/W Reset	01h																																				

5.5. Page 2 Command Description

5.5.1. Dynamic Backlight Control 1 (03h~05h)

Command Page			Page 2																																												
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																				
03h	1st	W/R	0	TT_STP_MED[2:0]			1	TT_STP_LOW[2:0]			29h																																				
04h	1st	W/R	0	ST_TIM_LOW[2:0]			0	TT_STP_HIGH[2:0]			14h																																				
05h	1st	W/R	0	ST_TIM_HIGH[2:0]			0	ST_TIM_MED[2:0]			32h																																				
Description	<p>TT_STP_HIGH[2:0]: This parameter is used set the dimming transition step for CABC high enhancement.</p> <p>TT_STP_MED[2:0]: This parameter is used set the dimming transition step for CABC medium enhancement.</p> <p>TT_STP_LOW[2:0]: This parameter is used set the dimming transition step for CABC low enhancement.</p> <table border="1"> <thead> <tr> <th>TT_STP_HIGH[2:0] TT_STP_MED[2:0] TT_STP_LOW[2:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>0h</td><td>1 step</td></tr> <tr><td>1h</td><td>2 step</td></tr> <tr><td>2h</td><td>4 step</td></tr> <tr><td>3h</td><td>8 step</td></tr> <tr><td>4h</td><td>16 step</td></tr> <tr><td>5h</td><td>32 step</td></tr> <tr><td>6h</td><td>64 step</td></tr> <tr><td>7h</td><td>128 step</td></tr> </tbody> </table> <p>ST_TIM_HIGH[2:0]: This parameter is used set the dimming time for CABC high enhancement.</p> <p>ST_TIM_MED[2:0]: This parameter is used set the dimming time for CABC medium enhancement.</p> <p>ST_TIM_LOW[2:0]: This parameter is used set the dimming time for CABC low enhancement.</p> <table border="1"> <thead> <tr> <th>ST_TIM_HIGH[2:0] ST_TIM_MED[2:0] ST_TIM_LOW[2:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>0h</td><td>1 frame</td></tr> <tr><td>1h</td><td>2 frame</td></tr> <tr><td>2h</td><td>4 frame</td></tr> <tr><td>3h</td><td>8 frame</td></tr> <tr><td>4h</td><td>16 frame</td></tr> <tr><td>5h</td><td>32 frame</td></tr> <tr><td>6h</td><td>64 frame</td></tr> <tr><td>7h</td><td>128 frame</td></tr> </tbody> </table>											TT_STP_HIGH[2:0] TT_STP_MED[2:0] TT_STP_LOW[2:0]	Description	0h	1 step	1h	2 step	2h	4 step	3h	8 step	4h	16 step	5h	32 step	6h	64 step	7h	128 step	ST_TIM_HIGH[2:0] ST_TIM_MED[2:0] ST_TIM_LOW[2:0]	Description	0h	1 frame	1h	2 frame	2h	4 frame	3h	8 frame	4h	16 frame	5h	32 frame	6h	64 frame	7h	128 frame
	TT_STP_HIGH[2:0] TT_STP_MED[2:0] TT_STP_LOW[2:0]	Description																																													
0h	1 step																																														
1h	2 step																																														
2h	4 step																																														
3h	8 step																																														
4h	16 step																																														
5h	32 step																																														
6h	64 step																																														
7h	128 step																																														
ST_TIM_HIGH[2:0] ST_TIM_MED[2:0] ST_TIM_LOW[2:0]	Description																																														
0h	1 frame																																														
1h	2 frame																																														
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Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>29h_14h_32h</td> </tr> <tr> <td>S/W Reset</td> <td>29h_14h_32h</td> </tr> <tr> <td>H/W Reset</td> <td>29h_14h_32h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	29h_14h_32h	S/W Reset	29h_14h_32h	H/W Reset	29h_14h_32h																												
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Power On Sequence	29h_14h_32h																																														
S/W Reset	29h_14h_32h																																														
H/W Reset	29h_14h_32h																																														

5.5.2. Dynamic Backlight Control 2 (06h~07h)

Command Page		Page 2																																																				
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																											
06h	1st	W/R	0	PWM_DUTY_PRECISION[2:0]			0	LEDPW_M_POL	LEDON_POL	LEDON	00h																																											
07h	1st	W/R	PWM_DIV[7:0]								0Eh																																											
Description	<p>LEDON: The bit is used to define LEDON enable.</p> <p>LEDON_POL: The bit is used to define polarity of LEDON.</p> <p>LEDPWM_POL: The bit is used to define polarity of LEDPWM signal.</p> <table border="1"> <thead> <tr> <th>BL</th> <th>LEDPWM_POL</th> <th>LEDPWM pin</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Always low</td> </tr> <tr> <td>0</td> <td>1</td> <td>Always high</td> </tr> <tr> <td>1</td> <td>0</td> <td>Original polarity of LEDPWM signal</td> </tr> <tr> <td>1</td> <td>1</td> <td>Inversed polarity of LEDPWM signal</td> </tr> </tbody> </table> <p>PWM_DUTY_PRECISION[2:0] / PWM_DIV[7:0]: LEDPWM output period control. This command is used to adjust the PWM waveform period of PWM_OUT. The PWM period is calculated using the following equation.</p> $f_{LEDPWM} = \frac{32 \text{ MHz}}{(PWM_DIV[7:0] + 1) \times PWM_DUTY_PRECISION}$ <table border="1"> <thead> <tr> <th>PWM_DUTY_PRECISION[2:0]</th> <th>PWM_DUTY_PRECISION</th> <th>f_{LEDPWM} (MAX) (PWM_DIV[7:0]=0)</th> <th>f_{LEDPWM} (min) (PWM_DIV[7:0]=255)</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>4096</td> <td>7.8 KHz</td> <td>31 Hz</td> </tr> <tr> <td>1h</td> <td>2048</td> <td>15.6 KHz</td> <td>61 Hz</td> </tr> <tr> <td>2h</td> <td>1024</td> <td>31.2 KHz</td> <td>122 Hz</td> </tr> <tr> <td>3h</td> <td>512</td> <td>62.5 KHz</td> <td>244 Hz</td> </tr> <tr> <td>4h</td> <td>256</td> <td>125 KHz</td> <td>488 Hz</td> </tr> <tr> <td>5h~7h</td> <td>Reserved</td> <td>X</td> <td>X</td> </tr> </tbody> </table> <p>Note : The output frequency tolerance of internal frequency divider in CABC is ±10%</p> <p>X = void.</p>											BL	LEDPWM_POL	LEDPWM pin	0	0	Always low	0	1	Always high	1	0	Original polarity of LEDPWM signal	1	1	Inversed polarity of LEDPWM signal	PWM_DUTY_PRECISION[2:0]	PWM_DUTY_PRECISION	f _{LEDPWM} (MAX) (PWM_DIV[7:0]=0)	f _{LEDPWM} (min) (PWM_DIV[7:0]=255)	0h	4096	7.8 KHz	31 Hz	1h	2048	15.6 KHz	61 Hz	2h	1024	31.2 KHz	122 Hz	3h	512	62.5 KHz	244 Hz	4h	256	125 KHz	488 Hz	5h~7h	Reserved	X	X
	BL	LEDPWM_POL	LEDPWM pin																																																			
	0	0	Always low																																																			
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	1	0	Original polarity of LEDPWM signal																																																			
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	PWM_DUTY_PRECISION[2:0]	PWM_DUTY_PRECISION	f _{LEDPWM} (MAX) (PWM_DIV[7:0]=0)	f _{LEDPWM} (min) (PWM_DIV[7:0]=255)																																																		
	0h	4096	7.8 KHz	31 Hz																																																		
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3h	512	62.5 KHz	244 Hz																																																			
4h	256	125 KHz	488 Hz																																																			
5h~7h	Reserved	X	X																																																			
Restriction																																																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																																			
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Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h_0Eh</td> </tr> <tr> <td>S/W Reset</td> <td>00h_0Eh</td> </tr> <tr> <td>H/W Reset</td> <td>00h_0Eh</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h_0Eh	S/W Reset	00h_0Eh	H/W Reset	00h_0Eh																																			
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H/W Reset	00h_0Eh																																																					

5.5.3. IIE Function Control (10h~19h)

Command Page			Page 2																																								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																
10h	1st	W/R	0	0	0	0	0	PRT_EN	SKIN_EN	0	06h																																
11h	1st	W/R	0	AUTO_MEAN	0	0	CN_EN	CN_INV	SHP_EN	0	00h																																
12h	1st	W/R	0	0	0	0	0	0	CN_LV[1:0]		02h																																
13h	1st	W/R	0	0	1	0	SRE_MIDIV_LV[1:0]		0	0	20h																																
15h	1st	W/R	RGB_MEAN[7:0]								80h																																
16h	1st	W/R	SRE_HYSTERESIS_EN	0	0	SRE_DIM_EN	SRE_SC_EN	SRE_CE_EN	0	0	1Ch																																
17h	1st	W/R	0	SRE_OFFSETS[2:0]			0	SRE_DIM_STP[2:0]			01h																																
18h	1st	W/R	SRE_DIM_FRAME[7:0]									08h																															
19h	1st	W/R	SRE_SC_GAIN_ADJ[2:0]			SRE_HYSTERESIS_LIMIT[4:0]				C0h																																	
Description	<p>PRT_EN: Enable the over-saturation protection of saturation enhancement.</p> <p>SKIN_EN: Enable the skin-tone protection of saturation enhancement.</p> <p>AUTO_MEAN: Enable auto image mean calculation RGB_MEAN[7:0] is not available when AUTO_MEAN=1h.</p> <p>CN_EN: Enable contrast enhancement.</p> <p>CN_INV: Select contrast enhancement Function.</p> <table border="1"> <thead> <tr> <th>CN_INV</th> <th>Contrast Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Contrast increase</td> </tr> <tr> <td>1</td> <td>Contrast decrease</td> </tr> </tbody> </table> <p>SHP_EN: Enable sharpness enhancement.</p> <p>CN_LV[1:0] : Define contrast enhancement level.</p> <p>SRE_MIDIV_LV[1:0] : Define SRE medium level enhancement select.</p> <table border="1"> <thead> <tr> <th>SRE_MIDIV_LV[1:0]</th> <th>Enhancement level</th> </tr> </thead> <tbody> <tr> <td>00h / 11h</td> <td>Level_M</td> </tr> <tr> <td>01h</td> <td>Level_H</td> </tr> <tr> <td>10h</td> <td>Level_L</td> </tr> </tbody> </table> <p>RGB_MEAN[7:0]: Setting image mean value, available when AUTO_MEAN=0h.</p> <p>SRE_HYSTERESIS_EN: SRE hysteresis mode enable signal.</p> <p>SRE_DIM_EN: SRE dimming function enable signal.</p> <p>SRE_SC_EN: SRE saturation compensation enable.</p> <p>SRE_CE_EN: SRE contrast enhancement enable.</p> <p>SRE_OFFSETS[2:0]: SRE offset value</p> <p>SRE_DIM_STP[2:0]: Setting the number of dimming steps for transition</p> <table border="1"> <thead> <tr> <th>SRE_DIM_STP[2:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>2 step</td> </tr> <tr> <td>1h</td> <td>4 step</td> </tr> <tr> <td>2h</td> <td>8 step</td> </tr> <tr> <td>3h</td> <td>16 step</td> </tr> <tr> <td>4h</td> <td>32 step</td> </tr> <tr> <td>5h</td> <td>64 step</td> </tr> <tr> <td>6h</td> <td>128 step</td> </tr> <tr> <td>7h</td> <td>256 step</td> </tr> </tbody> </table> <p>SRE_DIM_FRAME[7:0]: Setting the step time as frame units for each dimming step</p>											CN_INV	Contrast Function	0	Contrast increase	1	Contrast decrease	SRE_MIDIV_LV[1:0]	Enhancement level	00h / 11h	Level_M	01h	Level_H	10h	Level_L	SRE_DIM_STP[2:0]	Description	0h	2 step	1h	4 step	2h	8 step	3h	16 step	4h	32 step	5h	64 step	6h	128 step	7h	256 step
CN_INV	Contrast Function																																										
0	Contrast increase																																										
1	Contrast decrease																																										
SRE_MIDIV_LV[1:0]	Enhancement level																																										
00h / 11h	Level_M																																										
01h	Level_H																																										
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SRE_DIM_STP[2:0]	Description																																										
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SRE_DIM_FRAME[7:0]	Description																				
0h~2h	2 frame																				
3	4 frame																				
4	4 frame																				
5	5 frame																				
6	6 frame																				
:	:																				
:	:																				
254	254 frame																				
255	255 frame																				
Restriction	None																				
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes												
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S/W Reset	06h_00h_02h_20h_80h_1Ch_01h_08h_C0h																				
H/W Reset	06h_00h_02h_20h_80h_1Ch_01h_08h_C0h																				

5.5.4. IIE Saturation Enhancement Control 1 (1Ah~1Ch)

Command Page			Page 2																																																																												
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																																																				
1Ah	1st	W/R	0	0	SE_RATIO_L[5:0]					07h																																																																					
1Bh	1st	W/R	0	0	SE_RATIO_M[5:0]					09h																																																																					
1Ch	1st	W/R	0	0	SE_RATIO_H[5:0]					0Ch																																																																					
Description	<p>SE_RATIO_L[5:0]: Define low saturation enhancement level of User Command 55h (Page0_R55h).</p> <p>SE_RATIO_M[5:0]: Define medium saturation enhancement level of User Command 55h (Page0_R55h).</p> <p>SE_RATIO_H[5:0]: Define high saturation enhancement level of User Command 55h (Page0_R55h).</p> <p style="text-align: center;">$Saturation_{enhanced} = Saturation_{original} + (Saturation_{original} \times SE_RATIO)$</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>SE_RATIO_L[5:0] SE_RATIO_M[5:0] SE_RATIO_H[5:0]</th> <th>Ratio (Dec)</th> <th>SE_RATIO_L[5:0] SE_RATIO_M[5:0] SE_RATIO_H[5:0]</th> <th>Ratio (Dec)</th> </tr> </thead> <tbody> <tr><td>00h</td><td>0.0</td><td>10h</td><td>1.0</td></tr> <tr><td>01h</td><td>0.0625</td><td>11h</td><td>1.0625</td></tr> <tr><td>02h</td><td>0.125</td><td>12h</td><td>1.125</td></tr> <tr><td>03h</td><td>0.1875</td><td>13h</td><td>1.1875</td></tr> <tr><td>04h</td><td>0.25</td><td>14h</td><td>1.25</td></tr> <tr><td>05h</td><td>0.3125</td><td>15h</td><td>1.3125</td></tr> <tr><td>06h</td><td>0.375</td><td>16h</td><td>1.375</td></tr> <tr><td>07h</td><td>0.4375</td><td>17h</td><td>1.4375</td></tr> <tr><td>08h</td><td>0.5</td><td>18h</td><td>1.5</td></tr> <tr><td>09h</td><td>0.5625</td><td>19h</td><td>1.5625</td></tr> <tr><td>0Ah</td><td>0.625</td><td>1Ah</td><td>1.625</td></tr> <tr><td>0Bh</td><td>0.6875</td><td>1Bh</td><td>1.6875</td></tr> <tr><td>0Ch</td><td>0.75</td><td>1Ch</td><td>1.75</td></tr> <tr><td>0Dh</td><td>0.8125</td><td>1Dh</td><td>1.8125</td></tr> <tr><td>0Eh</td><td>0.875</td><td>1Eh</td><td>1.875</td></tr> <tr><td>0Fh</td><td>0.9375</td><td>1Fh</td><td>1.9375</td></tr> </tbody> </table>											SE_RATIO_L[5:0] SE_RATIO_M[5:0] SE_RATIO_H[5:0]	Ratio (Dec)	SE_RATIO_L[5:0] SE_RATIO_M[5:0] SE_RATIO_H[5:0]	Ratio (Dec)	00h	0.0	10h	1.0	01h	0.0625	11h	1.0625	02h	0.125	12h	1.125	03h	0.1875	13h	1.1875	04h	0.25	14h	1.25	05h	0.3125	15h	1.3125	06h	0.375	16h	1.375	07h	0.4375	17h	1.4375	08h	0.5	18h	1.5	09h	0.5625	19h	1.5625	0Ah	0.625	1Ah	1.625	0Bh	0.6875	1Bh	1.6875	0Ch	0.75	1Ch	1.75	0Dh	0.8125	1Dh	1.8125	0Eh	0.875	1Eh	1.875	0Fh	0.9375	1Fh	1.9375
	SE_RATIO_L[5:0] SE_RATIO_M[5:0] SE_RATIO_H[5:0]	Ratio (Dec)	SE_RATIO_L[5:0] SE_RATIO_M[5:0] SE_RATIO_H[5:0]	Ratio (Dec)																																																																											
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	02h	0.125	12h	1.125																																																																											
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	04h	0.25	14h	1.25																																																																											
	05h	0.3125	15h	1.3125																																																																											
	06h	0.375	16h	1.375																																																																											
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	08h	0.5	18h	1.5																																																																											
	09h	0.5625	19h	1.5625																																																																											
	0Ah	0.625	1Ah	1.625																																																																											
	0Bh	0.6875	1Bh	1.6875																																																																											
	0Ch	0.75	1Ch	1.75																																																																											
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S/W Reset	07h_09h_0Ch																																																																														
H/W Reset	07h_09h_0Ch																																																																														

5.5.5. IIE Saturation Protection Control (40h~4Fh)

Command Page			Page 2								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
40h	1st	W/R	0	0	0	LEVEL0_SR[4:0]				02h	
41h	1st	W/R	0	0	0	LEVEL1_SR[4:0]				04h	
42h	1st	W/R	0	0	0	LEVEL2_SR[4:0]				06h	
43h	1st	W/R	0	0	0	LEVEL3_SR[4:0]				08h	
44h	1st	W/R	0	0	0	LEVEL4_SR[4:0]				0Ah	
45h	1st	W/R	0	0	0	LEVEL5_SR[4:0]				0Ch	
46h	1st	W/R	0	0	0	LEVEL6_SR[4:0]				0Eh	
47h	1st	W/R	0	0	0	LEVEL7_SR[4:0]				0Eh	
48h	1st	W/R	0	0	0	LEVEL8_SR[4:0]				0Ch	
49h	1st	W/R	0	0	0	LEVEL9_SR[4:0]				0Ah	
4Ah	1st	W/R	0	0	0	LEVEL10_SR[4:0]				08h	
4Bh	1st	W/R	0	0	0	LEVEL11_SR[4:0]				06h	
4Ch	1st	W/R	0	0	0	LEVEL12_SR[4:0]				04h	
4Dh	1st	W/R	0	0	0	LEVEL13_SR[4:0]				03h	
4Eh	1st	W/R	0	0	0	LEVEL14_SR[4:0]				02h	
4Fh	1st	W/R	0	0	0	LEVEL15_SR[4:0]				00h	

Description

This register is used to restrict the enhancement gain of saturation enhancement. This function is able to use when PRT_EN=1.

LEVEL0_SR[4:0]: Adjust the weight value of saturation steps 0~15.

LEVEL1_SR[4:0]: Adjust the weight value of saturation steps 16~31.

LEVEL2_SR[4:0]: Adjust the weight value of saturation steps 32~47.

LEVEL3_SR[4:0]: Adjust the weight value of saturation steps 48~63.

LEVEL4_SR[4:0]: Adjust the weight value of saturation steps 64~79.

LEVEL5_SR[4:0]: Adjust the weight value of saturation steps 80~95.

LEVEL6_SR[4:0]: Adjust the weight value of saturation steps 96~111.

LEVEL7_SR[4:0]: Adjust the weight value of saturation steps 128~143.

LEVEL8_SR[4:0]: Adjust the weight value of saturation steps 144~159.

LEVEL9_SR[4:0]: Adjust the weight value of saturation steps 160~175.

LEVEL10_SR[4:0]: Adjust the weight value of saturation steps 176~191.

LEVEL11_SR[4:0]: Adjust the weight value of saturation steps 192~207.

LEVEL12_SR[4:0]: Adjust the weight value of saturation steps 208~223.

LEVEL13_SR[4:0]: Adjust the weight value of saturation steps 224~239.

LEVEL14_SR[4:0]: Adjust the weight value of saturation steps 240~255.

LEVEL15_SR[4:0]: Adjust the weight value of saturation steps 256.

$$\text{Saturation}_{\text{enhanced}} = \text{Saturation}_{\text{original}} + (\text{Saturation}_{\text{original}} \times SE_RATIO \times PRT_RATIO)$$

$$PRT_RATIO = 0 \sim 1.0$$

	<p>The graph shows the relationship between the grayscale ratio (prt_ratio) and the reference saturation (saturation_{reference}). The curve is parabolic, starting at 0 for saturation 0 and ending at 0 for saturation 240. The peak is at saturation 112 with a prt_ratio of 1.0. The curve is divided into 16 levels, labeled from level00_sr to level15_sr.</p>								
<p>Restriction</p>	<p>None</p>								
<p>Register Availability</p>	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes								
Sleep In	Yes								
<p>Default</p>	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>02h_04h_06h_08h_0Ah_0Ch_0Eh_0Eh_0Ch_0Ah_08h_06h_04h_03h_02h_00h</td> </tr> <tr> <td>S/W Reset</td> <td>02h_04h_06h_08h_0Ah_0Ch_0Eh_0Eh_0Ch_0Ah_08h_06h_04h_03h_02h_00h</td> </tr> <tr> <td>H/W Reset</td> <td>02h_04h_06h_08h_0Ah_0Ch_0Eh_0Eh_0Ch_0Ah_08h_06h_04h_03h_02h_00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	02h_04h_06h_08h_0Ah_0Ch_0Eh_0Eh_0Ch_0Ah_08h_06h_04h_03h_02h_00h	S/W Reset	02h_04h_06h_08h_0Ah_0Ch_0Eh_0Eh_0Ch_0Ah_08h_06h_04h_03h_02h_00h	H/W Reset	02h_04h_06h_08h_0Ah_0Ch_0Eh_0Eh_0Ch_0Ah_08h_06h_04h_03h_02h_00h
Status	Default Value								
Power On Sequence	02h_04h_06h_08h_0Ah_0Ch_0Eh_0Eh_0Ch_0Ah_08h_06h_04h_03h_02h_00h								
S/W Reset	02h_04h_06h_08h_0Ah_0Ch_0Eh_0Eh_0Ch_0Ah_08h_06h_04h_03h_02h_00h								
H/W Reset	02h_04h_06h_08h_0Ah_0Ch_0Eh_0Eh_0Ch_0Ah_08h_06h_04h_03h_02h_00h								

5.5.6. IIE Sharpness Enhancement Control (5Ah~5Ch)

Command Page			Page 2																																																																												
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																																																				
5Ah	1st	W/R	0	0	0	SHP_RATIO[4:0]				18h																																																																					
5Bh	1st	W/R	SHP_THR_H[7:0]								64h																																																																				
5Ch	1st	W/R	SHP_THR_L[7:0]								1Eh																																																																				
Description	<p>This register sets the enhancement level of the sharpness enhancement. This function is able to use when SHP_EN=1</p> <p>SHP_RATIO[4:0]: Adjust the ratio of sharpness enhancement.</p> $Y_{enh} = Y_{org} + (Y_{org} - blur(Y_{org})) \times SHP_RATIO$ <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>SHP_RATIO[4:0]</th> <th>Ratio (Dec)</th> <th>SHP_RATIO[4:0]</th> <th>Ratio (Dec)</th> </tr> </thead> <tbody> <tr><td>00h</td><td>0.0</td><td>10h</td><td>2.0</td></tr> <tr><td>01h</td><td>0.125</td><td>11h</td><td>2.125</td></tr> <tr><td>02h</td><td>0.25</td><td>12h</td><td>2.25</td></tr> <tr><td>03h</td><td>0.375</td><td>13h</td><td>2.375</td></tr> <tr><td>04h</td><td>0.5</td><td>14h</td><td>2.5</td></tr> <tr><td>05h</td><td>0.625</td><td>15h</td><td>2.625</td></tr> <tr><td>06h</td><td>0.75</td><td>16h</td><td>2.75</td></tr> <tr><td>07h</td><td>0.875</td><td>17h</td><td>2.875</td></tr> <tr><td>08h</td><td>1.0</td><td>18h</td><td>3.0</td></tr> <tr><td>09h</td><td>1.125</td><td>19h</td><td>3.125</td></tr> <tr><td>0Ah</td><td>1.25</td><td>1Ah</td><td>3.25</td></tr> <tr><td>0Bh</td><td>1.375</td><td>1Bh</td><td>3.375</td></tr> <tr><td>0Ch</td><td>1.5</td><td>1Ch</td><td>3.5</td></tr> <tr><td>0Dh</td><td>1.625</td><td>1Dh</td><td>3.625</td></tr> <tr><td>0Eh</td><td>1.75</td><td>1Eh</td><td>3.75</td></tr> <tr><td>0Fh</td><td>1.875</td><td>1Fh</td><td>3.875</td></tr> </tbody> </table> <p>SHP_THR_H[7:0]: Define Sharpness enhancement upper bound threshold.</p> <p>SHP_THR_L[7:0]: Define Sharpness enhancement lower bound threshold.</p>											SHP_RATIO[4:0]	Ratio (Dec)	SHP_RATIO[4:0]	Ratio (Dec)	00h	0.0	10h	2.0	01h	0.125	11h	2.125	02h	0.25	12h	2.25	03h	0.375	13h	2.375	04h	0.5	14h	2.5	05h	0.625	15h	2.625	06h	0.75	16h	2.75	07h	0.875	17h	2.875	08h	1.0	18h	3.0	09h	1.125	19h	3.125	0Ah	1.25	1Ah	3.25	0Bh	1.375	1Bh	3.375	0Ch	1.5	1Ch	3.5	0Dh	1.625	1Dh	3.625	0Eh	1.75	1Eh	3.75	0Fh	1.875	1Fh	3.875
	SHP_RATIO[4:0]	Ratio (Dec)	SHP_RATIO[4:0]	Ratio (Dec)																																																																											
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	01h	0.125	11h	2.125																																																																											
	02h	0.25	12h	2.25																																																																											
	03h	0.375	13h	2.375																																																																											
	04h	0.5	14h	2.5																																																																											
	05h	0.625	15h	2.625																																																																											
	06h	0.75	16h	2.75																																																																											
	07h	0.875	17h	2.875																																																																											
	08h	1.0	18h	3.0																																																																											
	09h	1.125	19h	3.125																																																																											
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	0Bh	1.375	1Bh	3.375																																																																											
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0Eh	1.75	1Eh	3.75																																																																												
0Fh	1.875	1Fh	3.875																																																																												
Restriction	None																																																																														
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Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>18h_64h_1Eh</td> </tr> <tr> <td>S/W Reset</td> <td>18h_64h_1Eh</td> </tr> <tr> <td>H/W Reset</td> <td>18h_64h_1Eh</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	18h_64h_1Eh	S/W Reset	18h_64h_1Eh	H/W Reset	18h_64h_1Eh																																																												
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5.5.7. IIE Contrast Enhancement Control (60h~66h)

Command Page			Page 2																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
60h	1st	W/R	0	0	CN_00[5:0]						0Eh								
61h	1st	W/R	0	0	CN_01[5:0]						18h								
62h	1st	W/R	0	0	CN_02[5:0]						24h								
63h	1st	W/R	0	0	CN_03[5:0]						28h								
64h	1st	W/R	0	0	CN_04[5:0]						24h								
65h	1st	W/R	0	0	CN_05[5:0]						18h								
66h	1st	W/R	0	0	CN_06[5:0]						0Eh								
Description	<p>This register sets the weight value of the turning point of contrast gain cure. This function is able to use when CN_EN=1</p> <p>CN_00[5:0]: Adjust the weight of S curve ratio of turning point 1. CN_01[5:0]: Adjust the weight of S curve ratio of turning point 2. CN_02[5:0]: Adjust the weight of S curve ratio of turning point 3. CN_03[5:0]: Adjust the weight of S curve ratio of turning point 4. CN_04[5:0]: Adjust the weight of S curve ratio of turning point 5. CN_05[5:0]: Adjust the weight of S curve ratio of turning point 6. CN_06[5:0]: Adjust the weight of S curve ratio of turning point 7.</p> $Y_{enh} = Y_{org} + Y_{delta}$																		
	Restriction	None																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
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Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>0Eh_18h_24h_28h_24h_18h_0Eh</td> </tr> <tr> <td>S/W Reset</td> <td>0Eh_18h_24h_28h_24h_18h_0Eh</td> </tr> <tr> <td>H/W Reset</td> <td>0Eh_18h_24h_28h_24h_18h_0Eh</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	0Eh_18h_24h_28h_24h_18h_0Eh	S/W Reset	0Eh_18h_24h_28h_24h_18h_0Eh	H/W Reset	0Eh_18h_24h_28h_24h_18h_0Eh
Status	Default Value																		
Power On Sequence	0Eh_18h_24h_28h_24h_18h_0Eh																		
S/W Reset	0Eh_18h_24h_28h_24h_18h_0Eh																		
H/W Reset	0Eh_18h_24h_28h_24h_18h_0Eh																		

5.5.8. IIE Auto White Balance 1 (D0h)

Command Page			Page 2																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
D0h	1st	W/R	0	0	0	0	0	0	0	AWB_EN	00h								
Description		AWB_EN : Enable AWB function, active high.																	
Restriction		To enable this command, "EXTC Command Set enable register (FFh) "must set first.																	
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	00h	S/W Reset	00h	H/W Reset	00h
Status	Default Value																		
Power On Sequence	00h																		
S/W Reset	00h																		
H/W Reset	00h																		

5.5.9. IIE Auto White Balance 2 (D1h~D4h)

Command Page			Page 2																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
D1h	1st	W/R	0	0	R_AWB_1[9:8]		G_AWB_1[9:8]		B_AWB_1[9:8]		3Fh								
D2h	1st	W/R	R_AWB_1[7:0]									FFh							
D3h	1st	W/R	G_AWB_1[7:0]									FFh							
D4h	1st	W/R	B_AWB_1[7:0]									FFh							
Description		<p>R_AWB_1[9:0] : Adjust the drop level of red. $R = R \times (1 + R_AWB_1)/1024$</p> <p>G_AWB_1[9:0] : Adjust the drop level of green. $G = G \times (1 + G_AWB_1)/1024$</p> <p>B_AWB_1[9:0] : Adjust the drop level of blue. $B = B \times (1 + B_AWB_1)/1024$</p>																	
Restriction		To enable this command, "EXTC Command Set enable register (FFh) "must set first.																	
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>3Fh_FFh_FFh_FFh</td> </tr> <tr> <td>S/W Reset</td> <td>3Fh_FFh_FFh_FFh</td> </tr> <tr> <td>H/W Reset</td> <td>3Fh_FFh_FFh_FFh</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	3Fh_FFh_FFh_FFh	S/W Reset	3Fh_FFh_FFh_FFh	H/W Reset	3Fh_FFh_FFh_FFh
Status	Default Value																		
Power On Sequence	3Fh_FFh_FFh_FFh																		
S/W Reset	3Fh_FFh_FFh_FFh																		
H/W Reset	3Fh_FFh_FFh_FFh																		

5.5.10. IIE Auto White Balance 3 (D5~D8)

Command Page			Page 2																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
D5h	1st	W/R	0	0	R_AWB_2[9:8]		G_AWB_2[9:8]		B_AWB_2[9:8]		3Fh								
D6h	1st	W/R	R_AWB_2[7:0]								FFh								
D7h	1st	W/R	G_AWB_2[7:0]								FFh								
D8h	1st	W/R	B_AWB_2[7:0]								FFh								
Description		<p>R_AWB_2[9:0] : Adjust the drop level of red. $R = R \times (1 + R_AWB_2)/1024$</p> <p>G_AWB_2[9:0] : Adjust the drop level of green. $G = G \times (1 + G_AWB_2)/1024$</p> <p>B_AWB_2[9:0] : Adjust the drop level of blue. $B = B \times (1 + B_AWB_2)/1024$</p>																	
Restriction		To enable this command, "EXTC Command Set enable register (FFh) "must set first.																	
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>3Fh_FFh_FFh_FFh</td> </tr> <tr> <td>S/W Reset</td> <td>3Fh_FFh_FFh_FFh</td> </tr> <tr> <td>H/W Reset</td> <td>3Fh_FFh_FFh_FFh</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	3Fh_FFh_FFh_FFh	S/W Reset	3Fh_FFh_FFh_FFh	H/W Reset	3Fh_FFh_FFh_FFh
Status	Default Value																		
Power On Sequence	3Fh_FFh_FFh_FFh																		
S/W Reset	3Fh_FFh_FFh_FFh																		
H/W Reset	3Fh_FFh_FFh_FFh																		

5.5.11. IIE Auto White Balance 4 (D9h~DCh)

Command Page			Page 2																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
D9h	1st	W/R	0	0	R_AWB_3[9:8]		G_AWB_3[9:8]		B_AWB_3[9:8]		3Fh								
DAh	1st	W/R	R_AWB_3[7:0]									FFh							
DBh	1st	W/R	G_AWB_3[7:0]									FFh							
DCh	1st	W/R	B_AWB_3[7:0]									FFh							
Description		<p>R_AWB_3[9:0] : Adjust the drop level of red. $R = R \times (1 + R_AWB_3)/1024$</p> <p>G_AWB_3[9:0] : Adjust the drop level of green. $G = G \times (1 + G_AWB_3)/1024$</p> <p>B_AWB_3[9:0] : Adjust the drop level of blue. $B = B \times (1 + B_AWB_3)/1024$</p>																	
Restriction		To enable this command, "EXTC Command Set enable register (FFh) "must set first.																	
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
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Sleep In	Yes																		
Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>3Fh_FFh_FFh_FFh</td> </tr> <tr> <td>S/W Reset</td> <td>3Fh_FFh_FFh_FFh</td> </tr> <tr> <td>H/W Reset</td> <td>3Fh_FFh_FFh_FFh</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	3Fh_FFh_FFh_FFh	S/W Reset	3Fh_FFh_FFh_FFh	H/W Reset	3Fh_FFh_FFh_FFh
Status	Default Value																		
Power On Sequence	3Fh_FFh_FFh_FFh																		
S/W Reset	3Fh_FFh_FFh_FFh																		
H/W Reset	3Fh_FFh_FFh_FFh																		

5.5.12. IIE Auto White Balance 5 (DDh~E0h)

Command Page			Page 2																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
DDh	1st	W/R	0	0	R_AWB_4[9:8]		G_AWB_4[9:8]		B_AWB_4[9:8]		3Fh								
DEh	1st	W/R	R_AWB_4[7:0]									FFh							
DFh	1st	W/R	G_AWB_4[7:0]									FFh							
E0h	1st	W/R	B_AWB_4[7:0]									FFh							
Description		<p>R_AWB_4[9:0] : Adjust the drop level of red. $R = R \times (1 + R_AWB_4)/1024$</p> <p>G_AWB_4[9:0] : Adjust the drop level of green. $G = G \times (1 + G_AWB_4)/1024$</p> <p>B_AWB_4[9:0] : Adjust the drop level of blue. $B = B \times (1 + B_AWB_4)/1024$</p>																	
Restriction		To enable this command, "EXTC Command Set enable register (FFh) "must set first.																	
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
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Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>3Fh_FFh_FFh_FFh</td> </tr> <tr> <td>S/W Reset</td> <td>3Fh_FFh_FFh_FFh</td> </tr> <tr> <td>H/W Reset</td> <td>3Fh_FFh_FFh_FFh</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	3Fh_FFh_FFh_FFh	S/W Reset	3Fh_FFh_FFh_FFh	H/W Reset	3Fh_FFh_FFh_FFh
Status	Default Value																		
Power On Sequence	3Fh_FFh_FFh_FFh																		
S/W Reset	3Fh_FFh_FFh_FFh																		
H/W Reset	3Fh_FFh_FFh_FFh																		

5.5.13. IIE Auto White Balance 6 (E1h~E4h)

Command Page			Page 2																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
E1h	1st	W/R	0	0	R_AWB_5[9:8]		G_AWB_5[9:8]		B_AWB_5[9:8]		3Fh								
E2h	1st	W/R	R_AWB_5[7:0]								FFh								
E3h	1st	W/R	G_AWB_5[7:0]								FFh								
E4h	1st	W/R	B_AWB_5[7:0]								FFh								
Description		<p>R_AWB_5[9:0] : Adjust the drop level of red. $R = R \times (1 + R_AWB_5)/1024$</p> <p>G_AWB_5[9:0] : Adjust the drop level of green. $G = G \times (1 + G_AWB_5)/1024$</p> <p>B_AWB_5[9:0] : Adjust the drop level of blue. $B = B \times (1 + B_AWB_5)/1024$</p>																	
Restriction		To enable this command, "EXTC Command Set enable register (FFh) "must set first.																	
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>3Fh_FFh_FFh_FFh</td> </tr> <tr> <td>S/W Reset</td> <td>3Fh_FFh_FFh_FFh</td> </tr> <tr> <td>H/W Reset</td> <td>3Fh_FFh_FFh_FFh</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	3Fh_FFh_FFh_FFh	S/W Reset	3Fh_FFh_FFh_FFh	H/W Reset	3Fh_FFh_FFh_FFh
Status	Default Value																		
Power On Sequence	3Fh_FFh_FFh_FFh																		
S/W Reset	3Fh_FFh_FFh_FFh																		
H/W Reset	3Fh_FFh_FFh_FFh																		

5.5.14. IIE Auto White Balance 7 (E5h~E8h)

Command Page			Page 2																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
E5h	1st	W/R	0	0	R_AWB_6[9:8]		G_AWB_6[9:8]		B_AWB_6[9:8]		3Fh								
E6h	1st	W/R	R_AWB_6[7:0]								FFh								
E7h	1st	W/R	G_AWB_6[7:0]								FFh								
E8h	1st	W/R	B_AWB_6[7:0]								FFh								
Description		<p>R_AWB_6[9:0] : Adjust the drop level of red. $R = R \times (1 + R_AWB_6)/1024$</p> <p>G_AWB_6[9:0] : Adjust the drop level of green. $G = G \times (1 + G_AWB_6)/1024$</p> <p>B_AWB_6[9:0] : Adjust the drop level of blue. $B = B \times (1 + B_AWB_6)/1024$</p>																	
Restriction		To enable this command, "EXTC Command Set enable register (FFh) "must set first.																	
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>3Fh_FFh_FFh_FFh</td> </tr> <tr> <td>S/W Reset</td> <td>3Fh_FFh_FFh_FFh</td> </tr> <tr> <td>H/W Reset</td> <td>3Fh_FFh_FFh_FFh</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	3Fh_FFh_FFh_FFh	S/W Reset	3Fh_FFh_FFh_FFh	H/W Reset	3Fh_FFh_FFh_FFh
Status	Default Value																		
Power On Sequence	3Fh_FFh_FFh_FFh																		
S/W Reset	3Fh_FFh_FFh_FFh																		
H/W Reset	3Fh_FFh_FFh_FFh																		

5.5.15. IIE Auto White Balance 8 (E9h~ECh)

Command Page			Page 2																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
E9h	1st	W/R	0	0	R_AWB_7[9:8]		G_AWB_7[9:8]		B_AWB_7[9:8]		3Fh								
EAh	1st	W/R	R_AWB_7[7:0]								FFh								
EBh	1st	W/R	G_AWB_7[7:0]								FFh								
ECh	1st	W/R	B_AWB_7[7:0]								FFh								
Description		<p>R_AWB_7[9:0] : Adjust the drop level of red. $R = R \times (1 + R_AWB_7)/1024$</p> <p>G_AWB_7[9:0] : Adjust the drop level of green. $G = G \times (1 + G_AWB_7)/1024$</p> <p>B_AWB_7[9:0] : Adjust the drop level of blue. $B = B \times (1 + B_AWB_7)/1024$</p>																	
Restriction		To enable this command, "EXTC Command Set enable register (FFh) "must set first.																	
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>3Fh_FFh_FFh_FFh</td> </tr> <tr> <td>S/W Reset</td> <td>3Fh_FFh_FFh_FFh</td> </tr> <tr> <td>H/W Reset</td> <td>3Fh_FFh_FFh_FFh</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	3Fh_FFh_FFh_FFh	S/W Reset	3Fh_FFh_FFh_FFh	H/W Reset	3Fh_FFh_FFh_FFh
Status	Default Value																		
Power On Sequence	3Fh_FFh_FFh_FFh																		
S/W Reset	3Fh_FFh_FFh_FFh																		
H/W Reset	3Fh_FFh_FFh_FFh																		

5.5.16. IIE Auto White Balance 9 (EDh)

Command Page			Page 2																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
EDh	1st	W/R	Color_Temp_Adj[7:0]								60h								
Description	Color_Temp_Adj : Adjust color temperature.																		
	Color_Temp_Adj[7:0]					Adjust Value													
	7'h00	AWB_1																	
	7'h01	AWB_1 * (31/32) + AWB_2 * (1/32)																	
	7'h02	AWB_1 * (30/32) + AWB_2 * (2/32)																	
																	
	7'h1F	AWB_1 * (1/32) + AWB_2 * (31/32)																	
	7'h20	AWB_2																	
	7'h21	AWB_2 * (31/32) + AWB_3 * (1/32)																	
	7'h22	AWB_2 * (30/32) + AWB_3 * (2/32)																	
																	
	7'h3F	AWB_2 * (1/32) + AWB_3 * (31/32)																	
	7'h40	AWB_3																	
	7'h41	AWB_3 * (31/32) + AWB_4 * (1/32)																	
	7'h42	AWB_3 * (30/32) + AWB_4 * (2/32)																	
																	
	7'h5F	AWB_3 * (1/32) + AWB_4 * (31/32)																	
	7'h60	AWB_4																	
	7'h61	AWB_4 * (31/32) + AWB_5 * (1/32)																	
	7'h62	AWB_4 * (30/32) + AWB_5 * (2/32)																	
																	
	7'h7F	AWB_4 * (1/32) + AWB_5 * (31/32)																	
	7'h80	AWB_5																	
	7'h81	AWB_5 * (31/32) + AWB_6 * (1/32)																	
	7'h82	AWB_5 * (30/32) + AWB_6 * (2/32)																	
																	
	7'h9F	AWB_5 * (1/32) + AWB_6 * (31/32)																	
	7'hA0	AWB_6																	
	7'hA1	AWB_6 * (31/32) + AWB_7 * (1/32)																	
	7'hA2	AWB_6 * (30/32) + AWB_7 * (2/32)																	
																	
	7'hBF	AWB_6 * (1/32) + AWB_7 * (31/32)																	
7'hC0	AWB_7																		
7'hC1	Reserved																		
....																		
7'hFF	Reserved																		
Restriction	To enable this command, "EXTC Command Set enable register (FFh) "must set first.																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		

Default	

Status	Default Value
Power On Sequence	60h
S/W Reset	60h
H/W Reset	60h

5.5.17. EXTC Command Set Enable Register (FFh)

Command Page			Page 2																																		
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																										
FFh	1st	W	1	0	0	1	1	0	0	0	98h																										
	2nd	W	1	0	0	0	0	0	0	1	81h																										
	3rd	W	PAGE[7:0]								02h																										
Description	<p>PAGE[7:0]: Set the command page.</p> <table border="1"> <thead> <tr> <th>PAGE[7:0]</th> <th>Command Page</th> </tr> </thead> <tbody> <tr><td>00h</td><td>Page 0</td></tr> <tr><td>01h</td><td>Page 1</td></tr> <tr><td>02h</td><td>Page 2</td></tr> <tr><td>03h</td><td>Page 3</td></tr> <tr><td>04h</td><td>Page 4</td></tr> <tr><td>05h</td><td>Page 5</td></tr> <tr><td>06h</td><td>Page 6</td></tr> <tr><td>07h</td><td>Page 7</td></tr> <tr><td>08h</td><td>Page 8</td></tr> <tr><td>09h</td><td>Page 9</td></tr> <tr><td>0Ah</td><td>Page 10</td></tr> <tr><td>Others</td><td>Reserved</td></tr> </tbody> </table> <p>Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available</p> <p>See section "5.1 Command Flow".</p>											PAGE[7:0]	Command Page	00h	Page 0	01h	Page 1	02h	Page 2	03h	Page 3	04h	Page 4	05h	Page 5	06h	Page 6	07h	Page 7	08h	Page 8	09h	Page 9	0Ah	Page 10	Others	Reserved
	PAGE[7:0]	Command Page																																			
	00h	Page 0																																			
	01h	Page 1																																			
	02h	Page 2																																			
	03h	Page 3																																			
	04h	Page 4																																			
	05h	Page 5																																			
	06h	Page 6																																			
	07h	Page 7																																			
	08h	Page 8																																			
	09h	Page 9																																			
	0Ah	Page 10																																			
Others	Reserved																																				
Restriction	None																																				
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																		
Status	Availability																																				
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																				
Normal Mode On, Idle Mode On, Sleep Out	Yes																																				
Sleep In	Yes																																				
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>02h</td> </tr> <tr> <td>S/W Reset</td> <td>02h</td> </tr> <tr> <td>H/W Reset</td> <td>02h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	02h	S/W Reset	02h	H/W Reset	02h																		
Status	Default Value																																				
Power On Sequence	02h																																				
S/W Reset	02h																																				
H/W Reset	02h																																				

5.6. Page 3 Command Description

5.6.1. GIP Setting 1 (01h~44h)

Command Page			Page 3								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
01h	1st	W/R	Reserve for other setting								-
02h	1st	W/R	Reserve for other setting								-
03h	1st	W/R	STV_A_Rise[9:8]		Phase_STV_A[1:0]		Overlap_STV_A[2:0]			-	
04h	1st	W/R	STV_B_Rise[9:8]		Phase_STV_B[1:0]		Overlap_STV_B[2:0]			-	
05h	1st	W/R	STV_C_Rise[9:8]		Phase_STV_C[1:0]		Overlap_STV_C[2:0]			-	
06h	1st	W/R	STV_A_Rise[7:0]								-
07h	1st	W/R	STV_B_Rise[7:0]								-
08h	1st	W/R	STV_C_Rise[7:0]								-
09h	1st	W/R	FTI_1_Rise[7:0]								-
0Ah	1st	W/R	FTI_2_Rise[7:0]								-
0Bh	1st	W/R	FTI_3_Rise[7:0]								-
0Ch	1st	W/R	FTI_1_Fall[7:0]								-
0Dh	1st	W/R	FTI_2_Fall[7:0]								-
0Eh	1st	W/R	FTI_3_Fall[7:0]								-
0Fh	1st	W/R	CLW_1_Rise[7:0]								-
10h	1st	W/R	CLW_2_Rise[7:0]								-
11h	1st	W/R	Reserve for other setting								-
12h	1st	W/R	Reserve for other setting								-
13h	1st	W/R	CLW_X_Fall[7:0]								-
14h	1st	W/R	Reserve for other setting								-
15h	1st	W/R	GPM_R_Stage_i[7:0]								-
16h	1st	W/R	GPM_R_Stage_ii[7:0]								-
17h	1st	W/R	GPM_F_Stage_i[7:0]								-
18h	1st	W/R	GPM_F_Stage_ii[7:0]								-
19h	1st	W/R	Reserve for other setting								-
1Ah	1st	W/R	Reserve for other setting								-
1Bh	1st	W/R	Reserve for other setting								-
1Ch	1st	W/R	Reserve for other setting								-
1Dh	1st	W/R	Reserve for other setting								-
1Eh	1st	W/R	GS_ENA	CLK_A_Rise[10:8]			Reserve for other setting	CLK_A_Fall[10:8]			-
1Fh	1st	W/R	Reserve for other setting	CLK_B_Rise[10:8]			Reserve for other setting	CLK_B_Fall[10:8]			-
20h	1st	W/R	CLK_A_Rise[7:0]								-
21h	1st	W/R	CLK_A_Fall[7:0]								-
22h	1st	W/R	CLK_B_Rise[7:0]								-
23h	1st	W/R	Reserve for other setting								-
24h	1st	W/R	CLK_Keep_Pos1[7:0]								-
25h	1st	W/R	CLK_Keep_Pos2[7:0]								-
26h	1st	W/R	Reserve for other setting								-
27h	1st	W/R	Reserve for other setting								-
28h	1st	W/R	CLK_Disable	CLK_x_Numb[2:0]			CLK_Keep	Phase_CLK[2:0]			-
29h	1st	W/R	Reserve for other setting				Overlap_CLK[3:0]				-
2Ah	1st	W/R	Reserve for other setting								-
2Bh	1st	W/R	Reserve for other setting								-
2Ch	1st	W/R	Reserve for other setting								-
2Dh	1st	W/R	Reserve for other setting								-
2Eh	1st	W/R	Reserve for other setting								-

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2Fh	1st	W/R	Reserve for other setting	-
30h	1st	W/R	Reserve for other setting	-
31h	1st	W/R	Reserve for other setting	-
32h	1st	W/R	Reserve for other setting	-
33h	1st	W/R	Reserve for other setting	-
34h	1st	W/R	Reserve for other setting	-
35h	1st	W/R	Reserve for other setting	-
36h	1st	W/R	Reserve for other setting	-
37h	1st	W/R	Reserve for other setting	-
38h	1st	W/R	Reserve for other setting	-
39h	1st	W/R	Reserve for other setting	-
3Ah	1st	W/R	Reserve for other setting	-
3Bh	1st	W/R	Reserve for other setting	-
3Ch	1st	W/R	Reserve for other setting	-
3Dh	1st	W/R	Reserve for other setting	-
3Eh	1st	W/R	Reserve for other setting	-
3Fh	1st	W/R	Reserve for other setting	-
40h	1st	W/R	Reserve for other setting	-
41h	1st	W/R	Reserve for other setting	-
42h	1st	W/R	Reserve for other setting	-
43h	1st	W/R	Reserve for other setting	-
44h	1st	W/R	Reserve for other setting	-

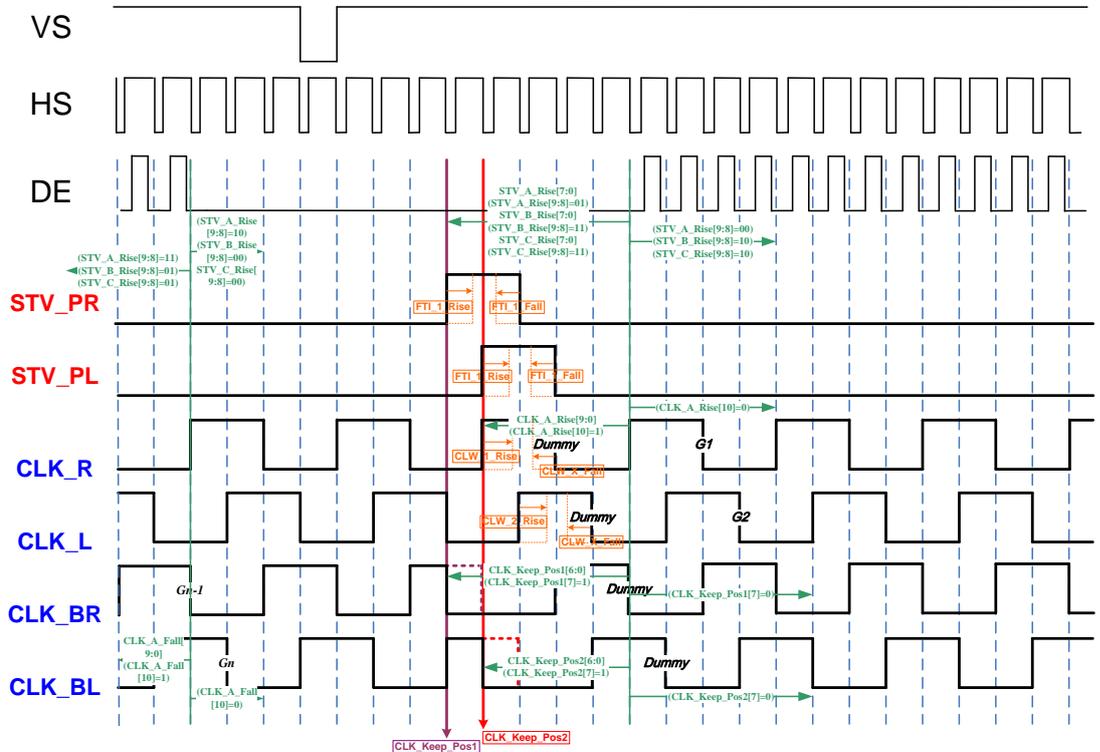
Description	<p>GS_ENA : Internal gate reverse function.</p> <table border="1"> <thead> <tr> <th>GS_ENA</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>On</td> </tr> <tr> <td>1</td> <td>Off</td> </tr> </tbody> </table>	GS_ENA	Description	0	On	1	Off												
	GS_ENA	Description																	
	0	On																	
	1	Off																	
	<p>CLK_X_Numb[2:0] : Number of CLK reverse.(internal gate reverse function)</p> <table border="1"> <thead> <tr> <th>CLK_X_Numb[2:0]</th> <th>Number of CLK</th> </tr> </thead> <tbody> <tr><td>000</td><td>2</td></tr> <tr><td>001</td><td>4</td></tr> <tr><td>010</td><td>6</td></tr> <tr><td>011</td><td>8</td></tr> <tr><td>100</td><td>10</td></tr> <tr><td>101</td><td>12</td></tr> <tr><td>110</td><td>14</td></tr> <tr><td>111</td><td>16</td></tr> </tbody> </table> <p><i>Note: Normally, set CLK_x_Numb[2:0] = Phase_CLK[2:0]</i></p>	CLK_X_Numb[2:0]	Number of CLK	000	2	001	4	010	6	011	8	100	10	101	12	110	14	111	16
	CLK_X_Numb[2:0]	Number of CLK																	
	000	2																	
	001	4																	
	010	6																	
	011	8																	
100	10																		
101	12																		
110	14																		
111	16																		
<p>CLK_Disable : reg_CLK_Keep_PosX setting.</p> <table border="1"> <thead> <tr> <th>CLK_Disable</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Enable</td> </tr> <tr> <td>1</td> <td>Disable</td> </tr> </tbody> </table>	CLK_Disable	Description	0	Enable	1	Disable													
CLK_Disable	Description																		
0	Enable																		
1	Disable																		
<p>CLK_Keep : CLK toggle continuously.</p> <table border="1"> <thead> <tr> <th>CLK_Keep</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Not Keep CLK</td> </tr> <tr> <td>1</td> <td>Keep CLK</td> </tr> </tbody> </table>	CLK_Keep	Description	0	Not Keep CLK	1	Keep CLK													
CLK_Keep	Description																		
0	Not Keep CLK																		
1	Keep CLK																		

FTI_n_Rise[7:0] / CLW_n_Rise[7:0] / CLW_x_Fall[7:0] / FTI_n_Fall[7:0], n = 1 ~ 3

GPM_R_Stage_i[7:0] / GPM_R_Stage_ii[7:0] / GPM_F_Stage_i[7:0] / GPM_F_Stage_ii[7:0] :

FTI_n_Rise[7:0] / CLW_n_Rise[7:0] / CLW_x_Fall[7:0] / FTI_n_Fall[7:0] / GPM_R_Stage_i[7:0] / GPM_R_Stage_ii[7:0] / GPM_F_Stage_i[7:0] / GPM_F_Stage_ii[7:0]	OP_CLK
8'h00	0 * T _{OP_CLK}
8'h01	2 * T _{OP_CLK}
8'h02	4 * T _{OP_CLK}
:	:
:	:
8'hFE	508 * T _{OP_CLK}
8'hFF	510 * T _{OP_CLK}

Note1 : T_{OP_CLK} : 62.5ns



Notes: CLK_R, CLK_BR will keep VGL between CLK_Keep_Pos1 and CLK_A_Rise setting point.

CLK_L, CLK_BL will keep VGL between CLK_Keep_Pos2 and CLK_B_Rise setting point.

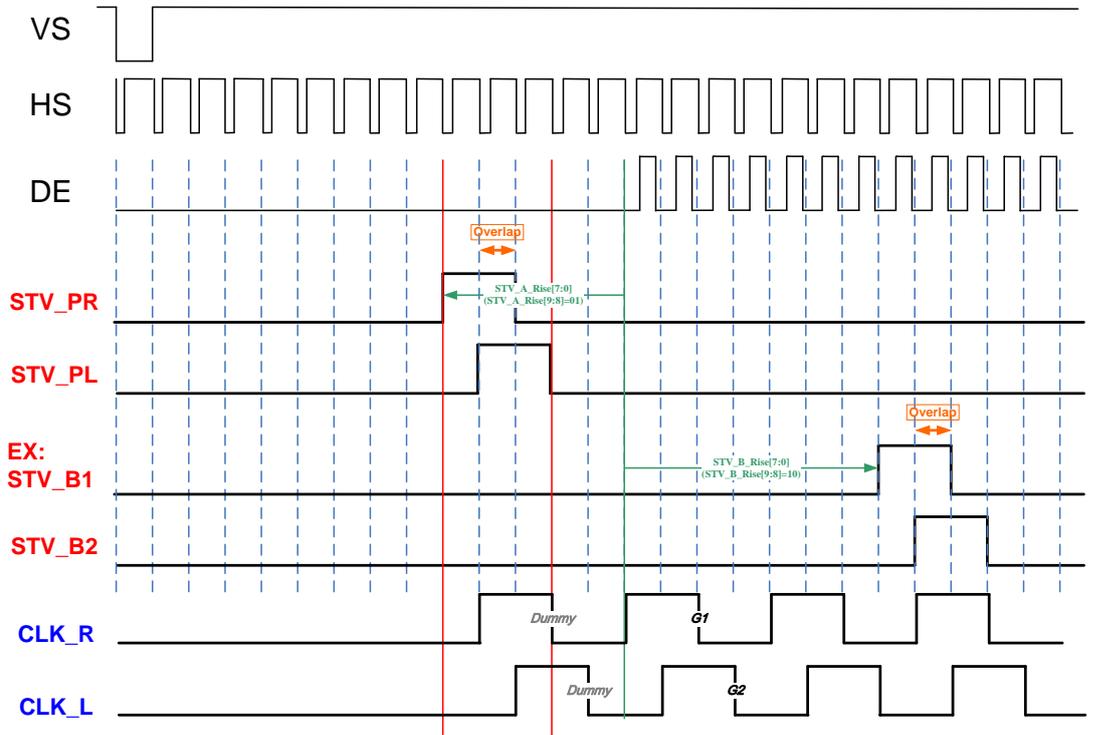
Phase_STV_A[1:0] / Phase_STV_B [1:0] / Phase_STV_C [1:0] :

Phase_STV_A[1:0] / Phase_STV_B [1:0] / Phase_STV_C[1:0]	Number of CLK
00	1
01	2
10	3
11	4

Overlap_STV_A[2:0] / Overlap_STV_B [2:0] / Overlap_STV_C [2:0]:

Overlap_STV_A[2:0] / Overlap_STV_B [2:0] / Overlap_STV_C [2:0]	Overlap of CLK
000	1H

001	2H
010	3H
011	4H
100	5H
101	6H
110	7H
111	8H

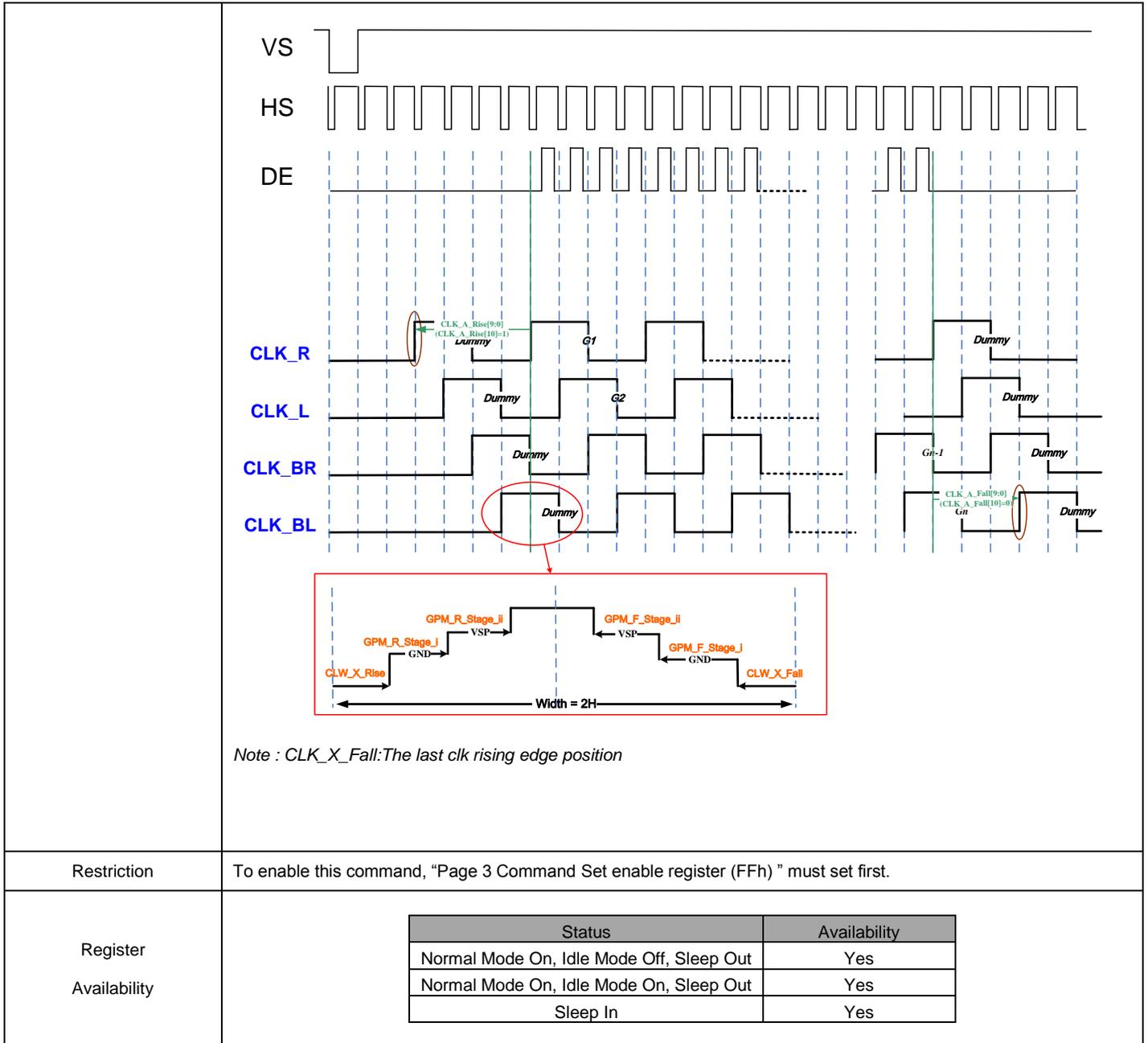


Phase_CLK[2:0] :

Phase_CLK [2:0]	Number of CLK
000	2
001	4
010	6
011	8
100	10
101	12
110	14
111	16

Overlap_CLK[1:0] :

Overlap_CLK [2:0]	Overlap of CLK
000	1H
001	2H
010	3H
011	4H
100	5H
101	6H
110	7H
111	8H



5.6.2. GIP Setting 2 (50h~5Dh)

Command Page			Page 3																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
50h	1st	W/R	STV_1_MUX[2:0]				STV_2_MUX[2:0]				-								
51h	1st	W/R	STV_3_MUX[2:0]				STV_4_MUX[2:0]				-								
52h	1st	W/R	STV_5_MUX[2:0]				STV_6_MUX[2:0]				-								
53h	1st	W/R	STV_7_MUX[2:0]				STV_8_MUX[2:0]				-								
54h	1st	W/R	STV_9_MUX[2:0]				STV_10_MUX[2:0]				-								
55h	1st	W/R	STV_11_MUX[2:0]				STV_12_MUX[2:0]				-								
56h	1st	W/R	CLK_1_MUX[2:0]				CLK_2_MUX[2:0]				-								
57h	1st	W/R	CLK_3_MUX[2:0]				CLK_4_MUX[2:0]				-								
58h	1st	W/R	CLK_5_MUX[2:0]				CLK_6_MUX[2:0]				-								
59h	1st	W/R	CLK_7_MUX[2:0]				CLK_8_MUX[2:0]				-								
5Ah	1st	W/R	CLK_9_MUX[2:0]				CLK_10_MUX[2:0]				-								
5Bh	1st	W/R	CLK_11_MUX[2:0]				CLK_12_MUX[2:0]				-								
5Ch	1st	W/R	CLK_13_MUX[2:0]				CLK_14_MUX[2:0]				-								
5Dh	1st	W/R	CLK_15_MUX[2:0]				CLK_16_MUX[2:0]				-								
Description		Change GIP signal timing output pin map.																	
Restriction		To enable this command, "Page 3 Command Set enable register (FFh) " must set first.																	
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		

5.6.3. GIP Setting 3 (5Eh~8Ah)

Command Page			Page 3														
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default						
5Eh	1st	W/R	Reserve for other setting			BACKWARDS	Reserve for other setting			FORWARDS	-						
5Fh	1st	W/R	0			GOUT_01_MUX_FW[4:0]					-						
60h	1st	W/R	0			GOUT_02_MUX_FW[4:0]					-						
61h	1st	W/R	0			GOUT_03_MUX_FW[4:0]					-						
62h	1st	W/R	0			GOUT_04_MUX_FW[4:0]					-						
63h	1st	W/R	0			GOUT_05_MUX_FW[4:0]					-						
64h	1st	W/R	0			GOUT_06_MUX_FW[4:0]					-						
65h	1st	W/R	0			GOUT_07_MUX_FW[4:0]					-						
66h	1st	W/R	0			GOUT_08_MUX_FW[4:0]					-						
67h	1st	W/R	0			GOUT_09_MUX_FW[4:0]					-						
68h	1st	W/R	0			GOUT_10_MUX_FW[4:0]					-						
69h	1st	W/R	0			GOUT_11_MUX_FW[4:0]					-						
6Ah	1st	W/R	0			GOUT_12_MUX_FW[4:0]					-						
6Bh	1st	W/R	0			GOUT_13_MUX_FW[4:0]					-						
6Ch	1st	W/R	0			GOUT_14_MUX_FW[4:0]					-						
6Dh	1st	W/R	0			GOUT_15_MUX_FW[4:0]					-						
6Eh	1st	W/R	0			GOUT_16_MUX_FW[4:0]					-						
6Fh	1st	W/R	0			GOUT_17_MUX_FW[4:0]					-						
70h	1st	W/R	0			GOUT_18_MUX_FW[4:0]					-						
71h	1st	W/R	0			GOUT_19_MUX_FW[4:0]					-						
72h	1st	W/R	0			GOUT_20_MUX_FW[4:0]					-						
73h	1st	W/R	0			GOUT_21_MUX_FW[4:0]					-						
74h	1st	W/R	0			GOUT_22_MUX_FW[4:0]					-						
75h	1st	W/R	0			GOUT_01_MUX_BW[4:0]					-						
76h	1st	W/R	0			GOUT_02_MUX_BW[4:0]					-						
77h	1st	W/R	0			GOUT_03_MUX_BW[4:0]					-						
78h	1st	W/R	0			GOUT_04_MUX_BW[4:0]					-						
79h	1st	W/R	0			GOUT_05_MUX_BW[4:0]					-						
7Ah	1st	W/R	0			GOUT_06_MUX_BW[4:0]					-						
7Bh	1st	W/R	0			GOUT_07_MUX_BW[4:0]					-						
7Ch	1st	W/R	0			GOUT_08_MUX_BW[4:0]					-						
7Dh	1st	W/R	0			GOUT_09_MUX_BW[4:0]					-						
7Eh	1st	W/R	0			GOUT_10_MUX_BW[4:0]					-						
7Fh	1st	W/R	0			GOUT_11_MUX_BW[4:0]					-						
80h	1st	W/R	0			GOUT_12_MUX_BW[4:0]					-						
81h	1st	W/R	0			GOUT_13_MUX_BW[4:0]					-						
82h	1st	W/R	0			GOUT_14_MUX_BW[4:0]					-						
83h	1st	W/R	0			GOUT_15_MUX_BW[4:0]					-						
84h	1st	W/R	0			GOUT_16_MUX_BW[4:0]					-						
85h	1st	W/R	0			GOUT_17_MUX_BW[4:0]					-						
86h	1st	W/R	0			GOUT_18_MUX_BW[4:0]					-						
87h	1st	W/R	0			GOUT_19_MUX_BW[4:0]					-						
88h	1st	W/R	0			GOUT_20_MUX_BW[4:0]					-						
89h	1st	W/R	0			GOUT_21_MUX_BW[4:0]					-						
8Ah	1st	W/R	0			GOUT_22_MUX_BW[4:0]					-						
Description		<p>BACKWARDS : Backward Scan Exchange Mode.</p> <table border="1"> <thead> <tr> <th>BACKWARDS</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Original</td> </tr> <tr> <td>1</td> <td>Exchange</td> </tr> </tbody> </table>										BACKWARDS	Description	0	Original	1	Exchange
BACKWARDS	Description																
0	Original																
1	Exchange																

FORWARDS : Forward Scan Exchange Mode.

FORWARDS	Description
0	Original
1	Exchange

GOUT_XX_MUX_FW[4:0] / GOUT_XX_MUX_BW[4:0] : These setting are the output status of GOUT[1:44].

GOUT_XX_MUX_FW[4:0] / GOUT_XX_MUX_BW[4:0]	Description
00h	If the GS=0, the setting is VGL, or if GS=1, the setting is VGH
01h	If the GS=0, the setting is VGH, or if GS=1, the setting is VGL
02h	VGL
03h	GND
04h	VSP
05h	VGH
06h	MUX2_STVA1_OUT
07h	MUX2_STVA3_OUT
08h	MUX2_STVB1_OUT
09h	MUX2_STVB3_OUT
0Ah	MUX2_STVC1_OUT
0Bh	MUX2_STVC3_OUT
0Ch	MUX2_CLKA1_OUT
0Dh	MUX2_CLKA3_OUT
0Eh	MUX2_CLKA5_OUT
0Fh	MUX2_CLKA7_OUT
10h	MUX2_CLKA9_OUT
11h	MUX2_CLKA11_OUT
12h	MUX2_CLKA13_OUT
13h	MUX2_CLKA15_OUT
14h	reserved
15h	reserved
16h	reserved
17h	reserved

Note : XX mean from 01 to 22.

Restriction

To enable this command, "Page 3 Command Set enable register (FFh)" must set first.

Register

Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

5.6.4. EXTC Command Set Enable Register (FFh)

Command Page			Page 3																																		
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																										
FFh	1st	W	1	0	0	1	1	0	0	0	98h																										
	2nd	W	1	0	0	0	0	0	0	1	81h																										
	3rd	W	PAGE[7:0]								03h																										
Description	<p>PAGE[7:0]: Set the command page.</p> <table border="1"> <thead> <tr> <th>PAGE[7:0]</th> <th>Command Page</th> </tr> </thead> <tbody> <tr><td>00h</td><td>Page 0</td></tr> <tr><td>01h</td><td>Page 1</td></tr> <tr><td>02h</td><td>Page 2</td></tr> <tr><td>03h</td><td>Page 3</td></tr> <tr><td>04h</td><td>Page 4</td></tr> <tr><td>05h</td><td>Page 5</td></tr> <tr><td>06h</td><td>Page 6</td></tr> <tr><td>07h</td><td>Page 7</td></tr> <tr><td>08h</td><td>Page 8</td></tr> <tr><td>09h</td><td>Page 9</td></tr> <tr><td>0Ah</td><td>Page 10</td></tr> <tr><td>Others</td><td>Reserved</td></tr> </tbody> </table> <p>Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available</p> <p>See section "5.1 Command Flow".</p>											PAGE[7:0]	Command Page	00h	Page 0	01h	Page 1	02h	Page 2	03h	Page 3	04h	Page 4	05h	Page 5	06h	Page 6	07h	Page 7	08h	Page 8	09h	Page 9	0Ah	Page 10	Others	Reserved
	PAGE[7:0]	Command Page																																			
	00h	Page 0																																			
	01h	Page 1																																			
	02h	Page 2																																			
	03h	Page 3																																			
	04h	Page 4																																			
	05h	Page 5																																			
	06h	Page 6																																			
	07h	Page 7																																			
	08h	Page 8																																			
	09h	Page 9																																			
	0Ah	Page 10																																			
Others	Reserved																																				
Restriction	None																																				
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																		
Status	Availability																																				
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																				
Normal Mode On, Idle Mode On, Sleep Out	Yes																																				
Sleep In	Yes																																				
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>03h</td> </tr> <tr> <td>S/W Reset</td> <td>03h</td> </tr> <tr> <td>H/W Reset</td> <td>03h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	03h	S/W Reset	03h	H/W Reset	03h																		
Status	Default Value																																				
Power On Sequence	03h																																				
S/W Reset	03h																																				
H/W Reset	03h																																				

5.7. Page 4 Command Description

5.7.1. DSI Lanes Control (00h)

Command Page			Page 4																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
00h	1st	W/R	MIPI_LANE_SEL	0	0	0	0	0	0	0	80h								
Description		MIPI_LANE_SEL : MIPI DSI lane number selection <i>Note: When use this setting, please reference to chapter 4.1 "DSI System Interface".</i>																	
Restriction		None																	
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>80h</td> </tr> <tr> <td>S/W Reset</td> <td>80h</td> </tr> <tr> <td>H/W Reset</td> <td>80h</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	80h	S/W Reset	80h	H/W Reset	80h
Status	Default Value																		
Power On Sequence	80h																		
S/W Reset	80h																		
H/W Reset	80h																		

5.7.2. SSC Function (0Bh,0Eh)

Command Page			Page 4																				
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
0Bh	1st	W/R	SSC_DIG_EN	SSC_DIG_STEP[2:0]			0	0	0	0	00h												
0Eh	1st	W/R	SSC_DIG_CNT[7:0]								00h												
Description	<p>SSC_DIG_EN : Enable/disable the SSC(Spread Spectrum Clock) function.</p> <p>SSC_DIG_STEP[2:0] : Set SSC parameter.</p> <p>SSC_DIG_CNT[7:0] : Set SSC parameter.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>SSC</th> <th>Address 0Bh</th> <th>Address 0Eh</th> </tr> </thead> <tbody> <tr> <td>±1%</td> <td>80h</td> <td>17h</td> </tr> <tr> <td>±2%</td> <td>90h</td> <td>0Bh</td> </tr> <tr> <td>Others</td> <td>Reserved</td> <td>Reserved</td> </tr> </tbody> </table>											SSC	Address 0Bh	Address 0Eh	±1%	80h	17h	±2%	90h	0Bh	Others	Reserved	Reserved
	SSC	Address 0Bh	Address 0Eh																				
	±1%	80h	17h																				
	±2%	90h	0Bh																				
Others	Reserved	Reserved																					
Restriction	None																						
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes				
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h_00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h_00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h_00h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h_00h	S/W Reset	00h_00h	H/W Reset	00h_00h				
Status	Default Value																						
Power On Sequence	00h_00h																						
S/W Reset	00h_00h																						
H/W Reset	00h_00h																						

5.7.3. Charge-Pump Setting (21h)

Command Page			Page 4																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
21h	1st	W/R	DMY_PU MP	0	1	1	0	0	0	0	B0h								
Description	<p>DMY_PUMP: Control the driver behavior when host stop transferring video data.</p> <table border="1"> <thead> <tr> <th>DMY_PUMP</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Charge-Pump VGH/VGL keep pumping and display shows smallest gamma voltage</td> </tr> <tr> <td>1</td> <td>Charge-Pump VGH/VGL keep pumping</td> </tr> </tbody> </table>											DMY_PUMP	Description	0	Charge-Pump VGH/VGL keep pumping and display shows smallest gamma voltage	1	Charge-Pump VGH/VGL keep pumping		
	DMY_PUMP	Description																	
0	Charge-Pump VGH/VGL keep pumping and display shows smallest gamma voltage																		
1	Charge-Pump VGH/VGL keep pumping																		
Restriction	None																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>B0h</td> </tr> <tr> <td>S/W Reset</td> <td>B0h</td> </tr> <tr> <td>H/W Reset</td> <td>B0h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	B0h	S/W Reset	B0h	H/W Reset	B0h
	Status	Default Value																	
Power On Sequence	B0h																		
S/W Reset	B0h																		
H/W Reset	B0h																		

5.7.4. Internal SD Timing Control (26h)

Command Page			Page 4								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
26h	1st	W/R	DET_TOLERANCE_OP[3:0]				0	1	1	0	76h
Description	DET_TOLERANCE_OP[3:0]: Control internal SD timing between latch1 load into latch2.										
	DET_TOLERANCE_OP[3:0]				Description						
	0000				62.5ns x 1						
	0001				62.5ns x 2						
						
1111				62.5ns x 16							
Restriction	None										
Register Availability	Status				Availability						
	Normal Mode On, Idle Mode Off, Sleep Out				Yes						
	Normal Mode On, Idle Mode On, Sleep Out				Yes						
	Sleep In				Yes						
Default	Status				Default Value						
	Power On Sequence				76h						
	S/W Reset				76h						
	H/W Reset				76h						

5.7.5. Touch Synchronization Timing Adjust (27h~2Ah)

Command Page			Page 4																								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																
27h	1st	W/R	TOUCH_OPT[1:0]		VSOD[1:0]		HSOM[1:0]		HFP_HB_P_OPT	VS_PW_OPT	00h																
28h	1st	W/R	HSOD[7:0]									05h															
29h	1st	W/R	HSOHW[7:0]									19h															
2Ah	1st	W/R	VS_OUT_EN	HS_OUT_EN	VS_OUT_POL	HS_OUT_POL	0	0	STB_EN	0	F0h																
Description			This command controls the synchronization output. This function is able to use when Page1_R29h=01h.																								
			TOUCH_OPT[1:0]: Select the Output Mode of synchronization (time scale: internal T _{OP_CLK})			<table border="1"> <thead> <tr> <th>TOUCH_OPT[1:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Off</td> </tr> <tr> <td>1h</td> <td>VFP+VBP</td> </tr> <tr> <td>2h</td> <td>Adjustable for VSOUT / HSOUT^(Note 2)</td> </tr> <tr> <td>3h</td> <td>VFP+VBP / HFP+HBP</td> </tr> </tbody> </table>									TOUCH_OPT[1:0]	Description	0h	Off	1h	VFP+VBP	2h	Adjustable for VSOUT / HSOUT ^(Note 2)	3h	VFP+VBP / HFP+HBP			
			TOUCH_OPT[1:0]	Description																							
			0h	Off																							
			1h	VFP+VBP																							
			2h	Adjustable for VSOUT / HSOUT ^(Note 2)																							
			3h	VFP+VBP / HFP+HBP																							
			VSOD[1:0]: Set the VSOUT delay timing (time scale: internal T _{OP_CLK})			<table border="1"> <thead> <tr> <th>VSOD[1:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>0 line (First line of back porch)</td> </tr> <tr> <td>1h</td> <td>1 line</td> </tr> <tr> <td>2h</td> <td>2 line</td> </tr> <tr> <td>3h</td> <td>3 line</td> </tr> </tbody> </table>									VSOD[1:0]	Description	0h	0 line (First line of back porch)	1h	1 line	2h	2 line	3h	3 line			
			VSOD[1:0]	Description																							
			0h	0 line (First line of back porch)																							
1h	1 line																										
2h	2 line																										
3h	3 line																										
HSOM[1:0]: Set the HSOUT active period (time scale: internal T _{OP_CLK})			<table border="1"> <thead> <tr> <th>HSOM[1:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>VACT Period + VFP + VBP</td> </tr> <tr> <td>1h</td> <td>VACT Period</td> </tr> <tr> <td>2h</td> <td>VFP+VBP</td> </tr> <tr> <td>3h</td> <td>Reserved</td> </tr> </tbody> </table>									HSOM[1:0]	Description	0h	VACT Period + VFP + VBP	1h	VACT Period	2h	VFP+VBP	3h	Reserved						
HSOM[1:0]	Description																										
0h	VACT Period + VFP + VBP																										
1h	VACT Period																										
2h	VFP+VBP																										
3h	Reserved																										
HFP_HBP_OPT: Select the output source for HSOUT			<table border="1"> <thead> <tr> <th>HFP_HBP_OPT</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Prebuf-Source</td> </tr> <tr> <td>1</td> <td>HSOUT^(Note 2)</td> </tr> </tbody> </table>									HFP_HBP_OPT	Description	0	Prebuf-Source	1	HSOUT ^(Note 2)										
HFP_HBP_OPT	Description																										
0	Prebuf-Source																										
1	HSOUT ^(Note 2)																										
VS_PW_OPT: Set the pulse width of VSOUT			<table border="1"> <thead> <tr> <th>VS_PW_OPT</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>pulse width = 1H</td> </tr> <tr> <td>1</td> <td>During transition from display off to display on : pulse width = 3H During transition from display on to display off : pulse width = 2H Otherwise : pulse width = 1H</td> </tr> </tbody> </table>									VS_PW_OPT	Description	0	pulse width = 1H	1	During transition from display off to display on : pulse width = 3H During transition from display on to display off : pulse width = 2H Otherwise : pulse width = 1H										
VS_PW_OPT	Description																										
0	pulse width = 1H																										
1	During transition from display off to display on : pulse width = 3H During transition from display on to display off : pulse width = 2H Otherwise : pulse width = 1H																										
HSOD[7:0]: Set HSOUT delay timing (time scale: internal T _{OP_CLK})			<table border="1"> <thead> <tr> <th>HSOD[1:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>0clk</td> </tr> <tr> <td>1h</td> <td>1clk</td> </tr> <tr> <td>2h</td> <td>2clk</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>FDh</td> <td>253clk</td> </tr> <tr> <td>FEh</td> <td>254clk</td> </tr> <tr> <td>FFh</td> <td>255clk</td> </tr> </tbody> </table>									HSOD[1:0]	Description	0h	0clk	1h	1clk	2h	2clk	:	:	FDh	253clk	FEh	254clk	FFh	255clk
HSOD[1:0]	Description																										
0h	0clk																										
1h	1clk																										
2h	2clk																										
:	:																										
FDh	253clk																										
FEh	254clk																										
FFh	255clk																										

	<p>HSOHW[7:0]: Set the high width of HSOUT (time scale: internal T_{OP_CLK})</p> <table border="1"> <thead> <tr> <th>HSOHW[1:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Reserved</td> </tr> <tr> <td>1h</td> <td>1clk</td> </tr> <tr> <td>2h</td> <td>2clk</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>FDh</td> <td>253clk</td> </tr> <tr> <td>FEh</td> <td>254clk</td> </tr> <tr> <td>FFh</td> <td>255clk</td> </tr> </tbody> </table> <p>VS_OUT_EN: VS signal output enable (1: enable, 0: disable)</p> <p>HS_OUT_EN: HS signal output enable (1: enable, 0: disable)</p> <p>VS_OUT_POL: VS signal polarity (1: non-inversion, 0: inversion)</p> <p>HS_OUT_POL: HS signal polarity (1: non-inversion, 0: inversion)</p> <p>STB_EN: touch option</p> <p><i>Note 1: T_{OP_CLK}: 32ns</i></p> <p><i>Note 2: When use this setting, please reference to chapter 16 "Touch Synchronization Signal".</i></p>	HSOHW[1:0]	Description	0h	Reserved	1h	1clk	2h	2clk	:	:	FDh	253clk	FEh	254clk	FFh	255clk
HSOHW[1:0]	Description																
0h	Reserved																
1h	1clk																
2h	2clk																
:	:																
FDh	253clk																
FEh	254clk																
FFh	255clk																
Restriction	None																
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes								
Status	Availability																
Normal Mode On, Idle Mode Off, Sleep Out	Yes																
Normal Mode On, Idle Mode On, Sleep Out	Yes																
Sleep In	Yes																
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h_05h_19h_F0h</td> </tr> <tr> <td>S/W Reset</td> <td>00h_05h_19h_F0h</td> </tr> <tr> <td>H/W Reset</td> <td>00h_05h_19h_F0h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h_05h_19h_F0h	S/W Reset	00h_05h_19h_F0h	H/W Reset	00h_05h_19h_F0h								
Status	Default Value																
Power On Sequence	00h_05h_19h_F0h																
S/W Reset	00h_05h_19h_F0h																
H/W Reset	00h_05h_19h_F0h																

5.7.6. BIST Mode Function (2Dh,2Fh)

Command Page			Page 4																																										
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																		
2Dh	1st	W/R	FRM_PT[7:0]								FFh																																		
2Fh	1st	W/R	0	0	FRM_CYC[1:0]		0	0	0	FRM_EN	00h																																		
Description	<p>FRM_PT[7:0]: Enable/disable the pattern</p> <table border="1"> <thead> <tr> <th>FRM_PT[7:0]</th> <th>Pattern</th> </tr> </thead> <tbody> <tr> <td>FRM_PT[0]</td> <td>White</td> </tr> <tr> <td>FRM_PT[1]</td> <td>Black</td> </tr> <tr> <td>FRM_PT[2]</td> <td>Red</td> </tr> <tr> <td>FRM_PT[3]</td> <td>Green</td> </tr> <tr> <td>FRM_PT[4]</td> <td>Blue</td> </tr> <tr> <td>FRM_PT[5]</td> <td>Gray128</td> </tr> <tr> <td>FRM_PT[6]</td> <td>Gray127</td> </tr> <tr> <td>FRM_PT[7]</td> <td>V-Color bar</td> </tr> </tbody> </table> <p>See also sections: "7 BIST Mode Function "</p> <p>FRM_CYC[1:0]: Set scan cycle of each pattern</p> <table border="1"> <thead> <tr> <th>FRM_CYC[1:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>64 frames</td> </tr> <tr> <td>1h</td> <td>128 frames</td> </tr> <tr> <td>2h</td> <td>256 frames</td> </tr> <tr> <td>3h</td> <td>512 frames</td> </tr> </tbody> </table> <p>FRM_EN: Enable/disable BIST mode function</p> <table border="1"> <thead> <tr> <th>FRM_EN</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Normal display</td> </tr> <tr> <td>1</td> <td>Enable BIST mode</td> </tr> </tbody> </table>											FRM_PT[7:0]	Pattern	FRM_PT[0]	White	FRM_PT[1]	Black	FRM_PT[2]	Red	FRM_PT[3]	Green	FRM_PT[4]	Blue	FRM_PT[5]	Gray128	FRM_PT[6]	Gray127	FRM_PT[7]	V-Color bar	FRM_CYC[1:0]	Description	0h	64 frames	1h	128 frames	2h	256 frames	3h	512 frames	FRM_EN	Description	0	Normal display	1	Enable BIST mode
	FRM_PT[7:0]	Pattern																																											
	FRM_PT[0]	White																																											
	FRM_PT[1]	Black																																											
FRM_PT[2]	Red																																												
FRM_PT[3]	Green																																												
FRM_PT[4]	Blue																																												
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FRM_PT[7]	V-Color bar																																												
FRM_CYC[1:0]	Description																																												
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FRM_EN	Description																																												
0	Normal display																																												
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Sleep In	Yes																																												
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Status	Default Value																																												
Power On Sequence	FFh_00h																																												
S/W Reset	FFh_00h																																												
H/W Reset	FFh_00h																																												

5.7.7. Source Timing Setting (35h)

Command Page			Page 4																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
35h	1st	W/R	0	0	0	1	HZ_OPT	1	1	1	17h								
Description	<p>HZ_OPT: Maximum source OP drive time.</p> <table border="1"> <thead> <tr> <th>HZ_OPT</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Disable</td> </tr> <tr> <td>1</td> <td>Enable (Before enable this function , set Page4_R3Ah_D[7]=0)</td> </tr> </tbody> </table>											HZ_OPT	Description	0	Disable	1	Enable (Before enable this function , set Page4_R3Ah_D[7]=0)		
	HZ_OPT	Description																	
0	Disable																		
1	Enable (Before enable this function , set Page4_R3Ah_D[7]=0)																		
Restriction	None																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
	Status	Availability																	
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Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>17h</td> </tr> <tr> <td>S/W Reset</td> <td>17h</td> </tr> <tr> <td>H/W Reset</td> <td>17h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	17h	S/W Reset	17h	H/W Reset	17h
	Status	Default Value																	
Power On Sequence	17h																		
S/W Reset	17h																		
H/W Reset	17h																		

5.7.8. Power Saving Control (3Ah)

Command Page		Page 4																													
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																				
3Ah	1st	W/R	PS_EN	PCST[6:0]								A4h																			
Description	<p>PS_EN: Source power saving enable</p> <table border="1"> <thead> <tr> <th>PS_EN</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Disable</td> </tr> <tr> <td>1</td> <td>Enable</td> </tr> </tbody> </table> <p>PCST[6:0]: Control power saving period</p> <table border="1"> <thead> <tr> <th>PCST[6:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0000000</td> <td>62.5ns x 1</td> </tr> <tr> <td>0000001</td> <td>62.5ns x 2</td> </tr> <tr> <td>0000010</td> <td>62.5ns x 3</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>0100100</td> <td>62.5ns x 37</td> </tr> <tr> <td>Others</td> <td>Inhibited</td> </tr> </tbody> </table>											PS_EN	Description	0	Disable	1	Enable	PCST[6:0]	Description	0000000	62.5ns x 1	0000001	62.5ns x 2	0000010	62.5ns x 3	0100100	62.5ns x 37	Others	Inhibited
	PS_EN	Description																													
0	Disable																														
1	Enable																														
PCST[6:0]	Description																														
0000000	62.5ns x 1																														
0000001	62.5ns x 2																														
0000010	62.5ns x 3																														
...	...																														
0100100	62.5ns x 37																														
Others	Inhibited																														
Restriction	None																														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes												
Status	Availability																														
Normal Mode On, Idle Mode Off, Sleep Out	Yes																														
Normal Mode On, Idle Mode On, Sleep Out	Yes																														
Sleep In	Yes																														
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>A4h</td> </tr> <tr> <td>S/W Reset</td> <td>A4h</td> </tr> <tr> <td>H/W Reset</td> <td>A4h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	A4h	S/W Reset	A4h	H/W Reset	A4h												
Status	Default Value																														
Power On Sequence	A4h																														
S/W Reset	A4h																														
H/W Reset	A4h																														

5.7.9. Power Control 1 (69h)

Command Page			Page 4																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
69h	1st	W/R	1	CP_VCL_CLP_OPTION_PRE[2:0]			0	1	1	1	D7h								
Description	CP_VCL_CLP_OPTION_PRE[2:0]: Set VCL clamp level.																		
	CP_VCL_CLP_OPTION_PRE[2:0]						VCL clamp level (V)												
	0h						-3.0V												
	1h						-2.9V												
	2h						-2.8V												
	3h						-2.7V												
	4h						-2.6V												
	5h						-2.5V												
	6h						-2.4V												
	7h						-2.3V												
Restriction	None																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>D7h</td> </tr> <tr> <td>S/W Reset</td> <td>D7h</td> </tr> <tr> <td>H/W Reset</td> <td>D7h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	D7h	S/W Reset	D7h	H/W Reset	D7h
Status	Default Value																		
Power On Sequence	D7h																		
S/W Reset	D7h																		
H/W Reset	D7h																		

5.7.10. Power Control 2 (6Eh)

Command Page		Page 4																																																																		
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																																									
6Eh	1st	W/R	0	DI_PWR_REG	REG1_VRH_CP[5:0]						6Ah																																																									
Description	<p>DI_PWR_REG: Select the input power mode.</p> <table border="1"> <thead> <tr> <th>DI_PWR_REG</th> <th>BOOSTM2</th> <th>BOOSTM1</th> <th>BOOSTM0</th> <th>Note</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>Power Mode 2A External VDDI, VSP and VSN (VCI=VSP) ^{Note 1}</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>1</td> <td>Power Mode 4 External VDDI, VCI, VSP and VSN</td> </tr> <tr> <td>X</td> <td>0</td> <td>1</td> <td>0</td> <td>Power Mode 3 External VDDI and VCI (ILI4003)</td> </tr> <tr> <td colspan="4">prohibited</td> <td>-</td> </tr> </tbody> </table> <p><i>Note 1: VCI and VSP pads must be connected by external metal path.</i></p> <p>REG1_VRH_CP[5:0]: Set VGH clamp level. (0.18V/step)</p> <table border="1"> <thead> <tr> <th>REG1_VRH_CP[5:0]</th> <th>VGH clamp level (V)</th> </tr> </thead> <tbody> <tr><td>03h</td><td>7.98</td></tr> <tr><td>04h</td><td>8.16</td></tr> <tr><td>05h</td><td>8.34</td></tr> <tr><td>06h</td><td>8.52</td></tr> <tr><td>07h</td><td>8.7</td></tr> <tr><td>08h</td><td>8.88</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>29h</td><td>14.82</td></tr> <tr><td>2Ah</td><td>15</td></tr> <tr><td>2Bh</td><td>15.18</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>39h</td><td>17.7</td></tr> <tr><td>3Ah</td><td>17.88</td></tr> <tr><td>3Bh</td><td>18.06</td></tr> <tr><td>Other</td><td>Reserved</td></tr> </tbody> </table>											DI_PWR_REG	BOOSTM2	BOOSTM1	BOOSTM0	Note	0	0	0	1	Power Mode 2A External VDDI, VSP and VSN (VCI=VSP) ^{Note 1}	1	0	0	1	Power Mode 4 External VDDI, VCI, VSP and VSN	X	0	1	0	Power Mode 3 External VDDI and VCI (ILI4003)	prohibited				-	REG1_VRH_CP[5:0]	VGH clamp level (V)	03h	7.98	04h	8.16	05h	8.34	06h	8.52	07h	8.7	08h	8.88	:	:	29h	14.82	2Ah	15	2Bh	15.18	:	:	39h	17.7	3Ah	17.88	3Bh	18.06	Other	Reserved
	DI_PWR_REG	BOOSTM2	BOOSTM1	BOOSTM0	Note																																																															
	0	0	0	1	Power Mode 2A External VDDI, VSP and VSN (VCI=VSP) ^{Note 1}																																																															
	1	0	0	1	Power Mode 4 External VDDI, VCI, VSP and VSN																																																															
	X	0	1	0	Power Mode 3 External VDDI and VCI (ILI4003)																																																															
	prohibited				-																																																															
	REG1_VRH_CP[5:0]	VGH clamp level (V)																																																																		
	03h	7.98																																																																		
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	05h	8.34																																																																		
06h	8.52																																																																			
07h	8.7																																																																			
08h	8.88																																																																			
:	:																																																																			
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Status	Default Value																																																																			
Power On Sequence	6Ah																																																																			
S/W Reset	6Ah																																																																			
H/W Reset	6Ah																																																																			

5.7.11. Power Control 3 (6Fh)

Command Page			Page 4																																																																																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																																																								
6Fh	1st	W/R	0	DI_CP_VGH_BH[2:0]			DI_CP_VGL_BL[2:0]			0	34h																																																																								
Description	<p>DI_CP_VGH_BH[2:0]: Set the factor used in the step-up circuits for VGH.</p> <p>Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.</p> <table border="1"> <thead> <tr> <th>DI_CP_VGH_BH[2:0]</th> <th>VGH Output (power mode 3, 4)</th> <th>VGH Output (power mode 2A)</th> <th>Flying Capacitor</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Reserved</td> <td>Reserved</td> <td>-</td> </tr> <tr> <td>1h</td> <td>2*VSP</td> <td>2*VSP</td> <td>C21P/N + C22P/N (option)</td> </tr> <tr> <td>2h</td> <td>2.5*VSP</td> <td>3*VSP</td> <td>C21P/N + C22P/N (option)</td> </tr> <tr> <td>3h</td> <td>3*VSP</td> <td>3*VSP</td> <td>C21P/N + C22P/N (option)</td> </tr> <tr> <td>4h</td> <td>3.5*VSP</td> <td>4*VSP</td> <td>C21P/N + C22P/N</td> </tr> <tr> <td>5h</td> <td>4*VSP</td> <td>4*VSP</td> <td>C21P/N + C22P/N</td> </tr> <tr> <td>6h</td> <td>4.5*VSP</td> <td>5*VSP</td> <td>C21P/N + C22P/N</td> </tr> <tr> <td>7h</td> <td>5*VSP</td> <td>5*VSP</td> <td>C21P/N + C22P/N</td> </tr> </tbody> </table> <p>DI_CP_VGL_BL[2:0]: Set the factor used in the step-up circuits for VGL. Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.</p> <table border="1"> <thead> <tr> <th>DI_CP_VGL_BL[2:0]</th> <th>VGL Output (power mode 3, 4)</th> <th>VGL Output (power mode 2A)</th> <th>Flying Capacitor</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>-1.5*VSP</td> <td>-2*VSP</td> <td>C23P/N + C24P/N (option)</td> </tr> <tr> <td>1h</td> <td>-2*VSP</td> <td>-2*VSP</td> <td>C23P/N + C24P/N (option)</td> </tr> <tr> <td>2h</td> <td>-2.5*VSP</td> <td>-3*VSP</td> <td>C23P/N + C24P/N (option)</td> </tr> <tr> <td>3h</td> <td>-3*VSP</td> <td>-3*VSP</td> <td>C23P/N + C24P/N (option)</td> </tr> <tr> <td>4h</td> <td>-3.5*VSP</td> <td>-4*VSP</td> <td>C23P/N + C24P/N</td> </tr> <tr> <td>5h</td> <td>-4*VSP</td> <td>-4*VSP</td> <td>C23P/N + C24P/N</td> </tr> <tr> <td>6h</td> <td>-4.5*VSP</td> <td>-5*VSP</td> <td>C23P/N + C24P/N</td> </tr> <tr> <td>7h</td> <td>-5*VSP</td> <td>-5*VSP</td> <td>C23P/N + C24P/N</td> </tr> </tbody> </table>											DI_CP_VGH_BH[2:0]	VGH Output (power mode 3, 4)	VGH Output (power mode 2A)	Flying Capacitor	0h	Reserved	Reserved	-	1h	2*VSP	2*VSP	C21P/N + C22P/N (option)	2h	2.5*VSP	3*VSP	C21P/N + C22P/N (option)	3h	3*VSP	3*VSP	C21P/N + C22P/N (option)	4h	3.5*VSP	4*VSP	C21P/N + C22P/N	5h	4*VSP	4*VSP	C21P/N + C22P/N	6h	4.5*VSP	5*VSP	C21P/N + C22P/N	7h	5*VSP	5*VSP	C21P/N + C22P/N	DI_CP_VGL_BL[2:0]	VGL Output (power mode 3, 4)	VGL Output (power mode 2A)	Flying Capacitor	0h	-1.5*VSP	-2*VSP	C23P/N + C24P/N (option)	1h	-2*VSP	-2*VSP	C23P/N + C24P/N (option)	2h	-2.5*VSP	-3*VSP	C23P/N + C24P/N (option)	3h	-3*VSP	-3*VSP	C23P/N + C24P/N (option)	4h	-3.5*VSP	-4*VSP	C23P/N + C24P/N	5h	-4*VSP	-4*VSP	C23P/N + C24P/N	6h	-4.5*VSP	-5*VSP	C23P/N + C24P/N	7h	-5*VSP	-5*VSP	C23P/N + C24P/N
	DI_CP_VGH_BH[2:0]	VGH Output (power mode 3, 4)	VGH Output (power mode 2A)	Flying Capacitor																																																																															
	0h	Reserved	Reserved	-																																																																															
	1h	2*VSP	2*VSP	C21P/N + C22P/N (option)																																																																															
2h	2.5*VSP	3*VSP	C21P/N + C22P/N (option)																																																																																
3h	3*VSP	3*VSP	C21P/N + C22P/N (option)																																																																																
4h	3.5*VSP	4*VSP	C21P/N + C22P/N																																																																																
5h	4*VSP	4*VSP	C21P/N + C22P/N																																																																																
6h	4.5*VSP	5*VSP	C21P/N + C22P/N																																																																																
7h	5*VSP	5*VSP	C21P/N + C22P/N																																																																																
DI_CP_VGL_BL[2:0]	VGL Output (power mode 3, 4)	VGL Output (power mode 2A)	Flying Capacitor																																																																																
0h	-1.5*VSP	-2*VSP	C23P/N + C24P/N (option)																																																																																
1h	-2*VSP	-2*VSP	C23P/N + C24P/N (option)																																																																																
2h	-2.5*VSP	-3*VSP	C23P/N + C24P/N (option)																																																																																
3h	-3*VSP	-3*VSP	C23P/N + C24P/N (option)																																																																																
4h	-3.5*VSP	-4*VSP	C23P/N + C24P/N																																																																																
5h	-4*VSP	-4*VSP	C23P/N + C24P/N																																																																																
6h	-4.5*VSP	-5*VSP	C23P/N + C24P/N																																																																																
7h	-5*VSP	-5*VSP	C23P/N + C24P/N																																																																																
Restriction	None																																																																																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																																																																
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Power On Sequence	34h																																																																																		
S/W Reset	34h																																																																																		
H/W Reset	34h																																																																																		

5.7.12. VREG1/2 Setting (7Ah)

Command Page			Page 4								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Ah	1st	W/R	0	0	0	DI_REG_ REG1_E N_CAP	0	0	0	0	00h
Description	DI_REG_REG1_EN_CAP: Using VREG1/2 external caps(1uF) enable										
	DI_REG_REG1_EN_CAP						Description				
	1						IC uses VREG1/2 caps(1uF) at FPC				
0						IC doesn't use VREG1/2 caps(1uF) at FPC					
Restriction	None										
Register Availability	Status						Availability				
	Normal Mode On, Idle Mode Off, Sleep Out						Yes				
	Normal Mode On, Idle Mode On, Sleep Out						Yes				
	Sleep In						Yes				
Default	Status						Default Value				
	Power On Sequence						00h				
	S/W Reset						00h				
	H/W Reset						00h				

5.7.13. LVD Function 1 (87h)

Command Page			Page 4																				
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
87h	1st	W/R	DI_LVD_CTL[3:0]				1	0	1	0	BAh												
Description	<p>DI_LVD_CTL[3:0]: The sensitivity adjustment of detecting when battery is removed and power voltage is low.</p> <table border="1"> <thead> <tr> <th>DI_LVD_CTL[3:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1111</td> <td>sensitivity high</td> </tr> <tr> <td>1011</td> <td>sensitivity medium</td> </tr> <tr> <td>0010</td> <td>sensitivity low</td> </tr> <tr> <td>0000</td> <td>disable detecting</td> </tr> <tr> <td>Others</td> <td>Inhibited</td> </tr> </tbody> </table>											DI_LVD_CTL[3:0]	Description	1111	sensitivity high	1011	sensitivity medium	0010	sensitivity low	0000	disable detecting	Others	Inhibited
	DI_LVD_CTL[3:0]	Description																					
1111	sensitivity high																						
1011	sensitivity medium																						
0010	sensitivity low																						
0000	disable detecting																						
Others	Inhibited																						
Restriction	None																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes				
	Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>BAh</td> </tr> <tr> <td>S/W Reset</td> <td>BAh</td> </tr> <tr> <td>H/W Reset</td> <td>BAh</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	BAh	S/W Reset	BAh	H/W Reset	BAh				
	Status	Default Value																					
Power On Sequence	BAh																						
S/W Reset	BAh																						
H/W Reset	BAh																						

5.7.14. LVD Function 2 (88h)

Command Page			Page 4																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
88h	1st	W/R	DIS_LVD_CHK	0	0	0	1	0	1	1	8Bh								
Description		<p>DIS_LVD_CHK: LVD check function control.</p> <table border="1"> <thead> <tr> <th>DIS_LVD_CHK</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>When LVD is detected, IC will directly turn off pump power and go into sleep in sequence</td> </tr> <tr> <td>1</td> <td>When LVD is detected, IC will go into normal power-off/sleep in sequence</td> </tr> </tbody> </table>										DIS_LVD_CHK	Description	0	When LVD is detected, IC will directly turn off pump power and go into sleep in sequence	1	When LVD is detected, IC will go into normal power-off/sleep in sequence		
DIS_LVD_CHK	Description																		
0	When LVD is detected, IC will directly turn off pump power and go into sleep in sequence																		
1	When LVD is detected, IC will go into normal power-off/sleep in sequence																		
Restriction		None																	
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default		<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8Bh</td> </tr> <tr> <td>S/W Reset</td> <td>8Bh</td> </tr> <tr> <td>H/W Reset</td> <td>8Bh</td> </tr> </tbody> </table>										Status	Default Value	Power On Sequence	8Bh	S/W Reset	8Bh	H/W Reset	8Bh
Status	Default Value																		
Power On Sequence	8Bh																		
S/W Reset	8Bh																		
H/W Reset	8Bh																		

5.7.15. VCOM Control (8Bh)

Command Page			Page 4																							
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default															
8Bh	1st	W/R	1	1	1	0	DI_VCM _SELO_E N	0	1	1	E3h															
Description		<p>DI_VCM_SELO_EN: Set the VCOM output mode.</p> <table border="1"> <thead> <tr> <th>DI_VCM_SELO_EN</th> <th>GS_PANEL ^{Note}</th> <th>VCOM output mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Set VCOM level by VCM1[8:0]</td> </tr> <tr> <td>0</td> <td>1</td> <td>Set VCOM level by VCM2[8:0]</td> </tr> <tr> <td>1</td> <td>0</td> <td>VCOM = 0V</td> </tr> <tr> <td>1</td> <td>1</td> <td>VCOM = 0V</td> </tr> </tbody> </table> <p><i>Note: Please reference "5.4.2 Set Panel Operation Mode and Data Complement Setting (22h)"</i></p>										DI_VCM_SELO_EN	GS_PANEL ^{Note}	VCOM output mode	0	0	Set VCOM level by VCM1[8:0]	0	1	Set VCOM level by VCM2[8:0]	1	0	VCOM = 0V	1	1	VCOM = 0V
DI_VCM_SELO_EN	GS_PANEL ^{Note}	VCOM output mode																								
0	0	Set VCOM level by VCM1[8:0]																								
0	1	Set VCOM level by VCM2[8:0]																								
1	0	VCOM = 0V																								
1	1	VCOM = 0V																								
Restriction		None																								
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																									
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Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In	Yes																									
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Status	Default Value																									
Power On Sequence	E3h																									
S/W Reset	E3h																									
H/W Reset	E3h																									

5.7.16. Power Control 4 (8Ch~8Dh)

Command Page		Page 4																	
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
8Dh	1st	W/R	0	DI_VCOM_CP_VGLCLP[6:0]								14h							
Description	DI_VCOM_CP_VGLCLP[6:0]: Set VGL clamp level. (0.18V/step)																		
							DI_VCOM_CP_VGLCLP[6:0]		VGL clamp level (V)										
							03h		-6.99										
							04h		-7.17										
							05h		-7.35										
							06h		-7.53										
							07h		-7.71										
							08h		-7.89										
							09h		-8.07										
							0Ah		-8.25										
							0Bh		-8.43										
							0Ch		-8.61										
							0Dh		-8.79										
							0Eh		-8.97										
							0Fh		-9.15										
							10h		-9.33										
							11h		-9.51										
							12h		-9.69										
							13h		-9.87										
							14h		-10.05										
							15h		-10.23										
							:		:										
							3Fh		-17.79										
						40h		-17.97											
						41h		-18.15											
						Others		Reserved											
Restriction	None																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>14h</td> </tr> <tr> <td>S/W Reset</td> <td>14h</td> </tr> <tr> <td>H/W Reset</td> <td>14h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	14h	S/W Reset	14h	H/W Reset	14h
Status	Default Value																		
Power On Sequence	14h																		
S/W Reset	14h																		
H/W Reset	14h																		

5.7.17. Reload Gamma Setting (B2h)

Command Page			Page 4																				
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default												
B2h	1st	W/R	RELOAD _GMA_E N	RELOAD _GMA_LI NE8_EN	0	1	0	0	0	1	D1h												
Description	<p>RELOAD_GMA_EN: Gamma setting reload enable when IC operates at sleep-out state.</p> <table border="1"> <thead> <tr> <th>RELOAD_GMA_EN</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Disable</td> </tr> <tr> <td>1</td> <td>Enable</td> </tr> </tbody> </table> <p>RELOAD_GMA_LINE8_EN: Gamma setting reload at the period of 8 line when IC operates at sleep-out state.</p> <table border="1"> <thead> <tr> <th>RELOAD_GMA_LINE8_EN</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Disable</td> </tr> <tr> <td>1</td> <td>Enable</td> </tr> </tbody> </table>											RELOAD_GMA_EN	Description	0	Disable	1	Enable	RELOAD_GMA_LINE8_EN	Description	0	Disable	1	Enable
RELOAD_GMA_EN	Description																						
0	Disable																						
1	Enable																						
RELOAD_GMA_LINE8_EN	Description																						
0	Disable																						
1	Enable																						
Restriction	None																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes				
Status	Availability																						
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Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Sleep In	Yes																						
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>D1h</td> </tr> <tr> <td>S/W Reset</td> <td>D1h</td> </tr> <tr> <td>H/W Reset</td> <td>D1h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	D1h	S/W Reset	D1h	H/W Reset	D1h				
Status	Default Value																						
Power On Sequence	D1h																						
S/W Reset	D1h																						
H/W Reset	D1h																						

5.7.18. Gamma Bias Level (B5h)

Command Page			Page 4																		
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default										
B5h	1st	W/R	0	0	0	0	0	DI_GMA_GAP[2:0]		02h											
Description	<p>DI_GMA_GAP[2:0]: Control the gamma bias level.</p> <table border="1"> <thead> <tr> <th>DI_GMA_GAP[2:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>111</td> <td>High</td> </tr> <tr> <td>110</td> <td>Medium High</td> </tr> <tr> <td>010</td> <td>Default value</td> </tr> <tr> <td>Others</td> <td>inhibited</td> </tr> </tbody> </table>											DI_GMA_GAP[2:0]	Description	111	High	110	Medium High	010	Default value	Others	inhibited
	DI_GMA_GAP[2:0]	Description																			
111	High																				
110	Medium High																				
010	Default value																				
Others	inhibited																				
Restriction	None																				
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes		
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	Status	Default Value																			
Power On Sequence	02h																				
S/W Reset	02h																				
H/W Reset	02h																				

5.7.19. Temperature Detecting Setting 1 (BBh~C2h)

Command Page			Page 4								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
BBh	1st	W/R	EN_TEM P_PROC ESS	0	CP_VGH_TAP_C[5:0]					1Eh	
BCh	1st	W/R	0	0	CP_VGH_TAP_L[5:0]					1Eh	
BDh	1st	W/R	0	0	CP_VGH_TAP_M[5:0]					1Eh	
BEh	1st	W/R	0	0	CP_VGH_TAP_H[5:0]					1Eh	
BFh	1st	W/R	VCOM_C[7:0]					4Ch			
C0h	1st	W/R	VCOM_L[7:0]					4Ch			
C1h	1st	W/R	VCOM_M[7:0]					4Ch			
C2h	1st	W/R	VCOM_H[7:0]					4Ch			

Description	EN_TEMP_PROCESS / EN_TS: Enable/Disable Temperature Detecting function.																																								
	<table border="1"> <thead> <tr> <th>EN_TEMP_PROCESS</th> <th>EN_TS</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Disable</td> </tr> <tr> <td>1</td> <td>1</td> <td>Enable</td> </tr> <tr> <td colspan="2">Other</td> <td>Reserved</td> </tr> </tbody> </table>		EN_TEMP_PROCESS	EN_TS	Function	0	0	Disable	1	1	Enable	Other		Reserved																											
	EN_TEMP_PROCESS	EN_TS	Function																																						
	0	0	Disable																																						
	1	1	Enable																																						
	Other		Reserved																																						
	CP_VGH_TAP_C[5:0]: Set VGH clamp level for Temp_Cold. (0.18V/step)																																								
	CP_VGH_TAP_L[5:0]: Set VGH clamp level for Temp_Low. (0.18V/step)																																								
	CP_VGH_TAP_M[5:0]: Set VGH clamp level for Temp_Middle. (0.18V/step)																																								
	CP_VGH_TAP_H[5:0]: Set VGH clamp level for Temp_High. (0.18V/step)																																								
<table border="1"> <thead> <tr> <th>CP_VGH_TAP_C[5:0] CP_VGH_TAP_L[5:0] CP_VGH_TAP_M[5:0] CP_VGH_TAP_H[5:0]</th> <th>VGH clamp level (V)</th> </tr> </thead> <tbody> <tr><td>03h</td><td>7.98</td></tr> <tr><td>04h</td><td>8.16</td></tr> <tr><td>05h</td><td>8.34</td></tr> <tr><td>06h</td><td>8.52</td></tr> <tr><td>07h</td><td>8.7</td></tr> <tr><td>08h</td><td>8.88</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>28h</td><td>14.64</td></tr> <tr><td>29h</td><td>14.82</td></tr> <tr><td>2Ah</td><td>15</td></tr> <tr><td>2Bh</td><td>15.18</td></tr> <tr><td>2Ch</td><td>15.36</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>37h</td><td>17.34</td></tr> <tr><td>38h</td><td>17.52</td></tr> <tr><td>39h</td><td>17.7</td></tr> <tr><td>3Ah</td><td>17.88</td></tr> <tr><td>3Bh</td><td>18.06</td></tr> <tr><td>Other</td><td>Reserved</td></tr> </tbody> </table>		CP_VGH_TAP_C[5:0] CP_VGH_TAP_L[5:0] CP_VGH_TAP_M[5:0] CP_VGH_TAP_H[5:0]	VGH clamp level (V)	03h	7.98	04h	8.16	05h	8.34	06h	8.52	07h	8.7	08h	8.88	:	:	28h	14.64	29h	14.82	2Ah	15	2Bh	15.18	2Ch	15.36	:	:	37h	17.34	38h	17.52	39h	17.7	3Ah	17.88	3Bh	18.06	Other	Reserved
CP_VGH_TAP_C[5:0] CP_VGH_TAP_L[5:0] CP_VGH_TAP_M[5:0] CP_VGH_TAP_H[5:0]	VGH clamp level (V)																																								
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VCOM_C[8:0]: Set the VCOM level for Temp_Cold.																																									
VCOM_L[8:0]: Set the VCOM level for Temp_Low.																																									

	<p>VCOM_M[8:0]: Set the VCOM level for Temp_Middle.</p> <p>VCOM_H[8:0]: Set the VCOM level for Temp_High.</p> <table border="1"> <thead> <tr> <th>VCOM_C[8:0] VCOM_L[8:0] VCOM_M[8:0] VCOM_H[8:0]</th> <th>VCOM voltage (V)</th> </tr> </thead> <tbody> <tr><td>010h</td><td>-0.204</td></tr> <tr><td>011h</td><td>-0.216</td></tr> <tr><td>012h</td><td>-0.228</td></tr> <tr><td>013h</td><td>-0.24</td></tr> <tr><td>014h</td><td>-0.252</td></tr> <tr><td>015h</td><td>-0.264</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>07Ah</td><td>-1.476</td></tr> <tr><td>07Bh</td><td>-1.488</td></tr> <tr><td>07Ch</td><td>-1.5</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>149h</td><td>-3.96</td></tr> <tr><td>14Ah</td><td>-3.972</td></tr> <tr><td>14Bh</td><td>-3.984</td></tr> <tr><td>14Ch</td><td>-3.996</td></tr> <tr><td>14Dh</td><td>-4.008</td></tr> <tr><td>Others</td><td>Reserved</td></tr> </tbody> </table>	VCOM_C[8:0] VCOM_L[8:0] VCOM_M[8:0] VCOM_H[8:0]	VCOM voltage (V)	010h	-0.204	011h	-0.216	012h	-0.228	013h	-0.24	014h	-0.252	015h	-0.264	:	:	07Ah	-1.476	07Bh	-1.488	07Ch	-1.5	:	:	149h	-3.96	14Ah	-3.972	14Bh	-3.984	14Ch	-3.996	14Dh	-4.008	Others	Reserved
VCOM_C[8:0] VCOM_L[8:0] VCOM_M[8:0] VCOM_H[8:0]	VCOM voltage (V)																																				
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Others	Reserved																																				
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Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>1Eh_1Eh_1Eh_1Eh_4Ch_4Ch_4Ch_4Ch</td> </tr> <tr> <td>S/W Reset</td> <td>1Eh_1Eh_1Eh_1Eh_4Ch_4Ch_4Ch_4Ch</td> </tr> <tr> <td>H/W Reset</td> <td>1Eh_1Eh_1Eh_1Eh_4Ch_4Ch_4Ch_4Ch</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	1Eh_1Eh_1Eh_1Eh_4Ch_4Ch_4Ch_4Ch	S/W Reset	1Eh_1Eh_1Eh_1Eh_4Ch_4Ch_4Ch_4Ch	H/W Reset	1Eh_1Eh_1Eh_1Eh_4Ch_4Ch_4Ch_4Ch																												
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H/W Reset	1Eh_1Eh_1Eh_1Eh_4Ch_4Ch_4Ch_4Ch																																				

5.7.20. Read VCOM OTP Data (C4h~C7h)

Command Page			Page 4																																												
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																																				
C4h	1st	R	0	0	0	0	0	0	0	OTP_VCM1[8]	00h																																				
C5h	1st	R	OTP_VCM1[7:0]								7Bh																																				
C6h	1st	R	0	0	0	0	0	0	0	OTP_VCM2[8]	00h																																				
C7h	1st	R	OTP_VCM2[7:0]								7Bh																																				
Description	<p>OTP_VCM1[8:0]: Read the VCOM1 OTP data used for vertical forward scan (GS_PANEL= 1'b0), when NV memory is programmed. (12mV/step)</p> <p>OTP_VCM2[8:0]: Read the VCOM2 OTP data used for vertical backward scan (GS_PANEL= 1'b1), when NV memory is programmed. (12mV/step)</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>OTP_VCM1[8:0] OTP_VCM2[8:0]</th> <th>VCOM voltage (V)</th> </tr> </thead> <tbody> <tr><td>010h</td><td>-0.204</td></tr> <tr><td>011h</td><td>-0.216</td></tr> <tr><td>012h</td><td>-0.228</td></tr> <tr><td>013h</td><td>-0.24</td></tr> <tr><td>014h</td><td>-0.252</td></tr> <tr><td>015h</td><td>-0.264</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>07Ah</td><td>-1.476</td></tr> <tr><td>07Bh</td><td>-1.488</td></tr> <tr><td>07Ch</td><td>-1.5</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>149h</td><td>-3.96</td></tr> <tr><td>14Ah</td><td>-3.972</td></tr> <tr><td>14Bh</td><td>-3.984</td></tr> <tr><td>14Ch</td><td>-3.996</td></tr> <tr><td>14Dh</td><td>-4.008</td></tr> <tr><td>Others</td><td>Reserved</td></tr> </tbody> </table> <p style="text-align: center;"><i>Note: VCOM ≥ VSN + 0.5V</i></p>											OTP_VCM1[8:0] OTP_VCM2[8:0]	VCOM voltage (V)	010h	-0.204	011h	-0.216	012h	-0.228	013h	-0.24	014h	-0.252	015h	-0.264	:	:	07Ah	-1.476	07Bh	-1.488	07Ch	-1.5	:	:	149h	-3.96	14Ah	-3.972	14Bh	-3.984	14Ch	-3.996	14Dh	-4.008	Others	Reserved
	OTP_VCM1[8:0] OTP_VCM2[8:0]	VCOM voltage (V)																																													
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Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h_7Bh_00h_7Bh</td> </tr> <tr> <td>S/W Res t</td> <td>00h_7Bh_00h_7Bh</td> </tr> <tr> <td>H/W Reset</td> <td>00h_7Bh_00h_7Bh</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	00h_7Bh_00h_7Bh	S/W Res t	00h_7Bh_00h_7Bh	H/W Reset	00h_7Bh_00h_7Bh																												
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Power On Sequence	00h_7Bh_00h_7Bh																																														
S/W Res t	00h_7Bh_00h_7Bh																																														
H/W Reset	00h_7Bh_00h_7Bh																																														

5.7.21. Temperature Detecting Setting 2 (C8h~CEh)

Command Page			Page 4																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
C8h	1st	W/R	TS_TH0[7:0]									00h							
C9h	1st	W/R	TS_TH1[7:0]									00h							
CAh	1st	W/R	TS_TH2[7:0]									00h							
CBh	1st	W/R	TS_TH3[7:0]									00h							
CCh	1st	W/R	TS_TH0[9:8]		TS_TH1[9:8]		TS_TH2[9:8]		TS_TH3[9:8]		00h								
CDh	1st	W/R	TS_DEBT_OPT[3:0]				TS_HYST_OPT[3:0]				02h								
CEh	1st	W/R	EN_TS	VCOM_C[8]	VCOM_L[8]	VCOM_M[8]	VCOM_H[8]	1	0	0	04h								
Description	<p>TS_TH0[9:0]: Set the temperature detecting range threshold for Temp_Cold.</p> <p>TS_TH1[9:0]: Set the temperature detecting range threshold for Temp_Low.</p> <p>TS_TH2[9:0]: Set the temperature detecting range threshold for Temp_Middle.</p> <p>TS_TH3[9:0]: Set the temperature detecting range threshold for Temp_High.</p> <p>TS_DEBT_OPT[3:0]: Set the de-bounce of temperature detecting range.</p> <p>TS_HYST_OPT[3:0]: Set the hysteresis of temperature detecting range.</p>																		
Restriction	None																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
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Status	Default Value																		
Power On Sequence	00h_00h_00h_00h_00h_02h_04h																		
S/W Reset	00h_00h_00h_00h_00h_02h_04h																		
H/W Reset	00h_00h_00h_00h_00h_02h_04h																		

5.7.22. OTP Control (D7h)

Command Page		Page 4																		
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default									
D7h	1st	W/R	0	0	0	OTP_PA TH	PROG_SEL[1:0]		0	0	1Ch									
Description	OTP_PATH: <table border="1" style="margin-left: 40px;"> <thead> <tr> <th>OTP_PATH</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Internal VGH Programming</td> </tr> <tr> <td>1</td> <td>External MTP_PWR Programming</td> </tr> </tbody> </table>											OTP_PATH	Description	0	Internal VGH Programming	1	External MTP_PWR Programming			
	OTP_PATH	Description																		
0	Internal VGH Programming																			
1	External MTP_PWR Programming																			
PROG_SEL[1:0]: <table border="1" style="margin-left: 40px;"> <thead> <tr> <th>PROG_SEL[1:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>Inhibited</td> </tr> <tr> <td>1h</td> <td>Internal Programming Setting (Best Setting)</td> </tr> <tr> <td>2h</td> <td>Inhibited</td> </tr> <tr> <td>3h</td> <td>Internal Programming Setting (Default)</td> </tr> </tbody> </table>											PROG_SEL[1:0]	Description	0h	Inhibited	1h	Internal Programming Setting (Best Setting)	2h	Inhibited	3h	Internal Programming Setting (Default)
PROG_SEL[1:0]	Description																			
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1h	Internal Programming Setting (Best Setting)																			
2h	Inhibited																			
3h	Internal Programming Setting (Default)																			
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Status	Availability																			
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Status	Default Value																			
Power On Sequence	1Ch																			
S/W Reset	1Ch																			
H/W Reset	1Ch																			

5.7.23. EXTC Command Set Enable Register (FFh)

Command Page			Page 4																																		
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																										
FFh	1st	W	1	0	0	1	1	0	0	0	98h																										
	2nd	W	1	0	0	0	0	0	0	1	81h																										
	3rd	W	PAGE[7:0]								04h																										
Description	<p>PAGE[7:0]: Set the command page.</p> <table border="1"> <thead> <tr> <th>PAGE[7:0]</th> <th>Command Page</th> </tr> </thead> <tbody> <tr><td>00h</td><td>Page 0</td></tr> <tr><td>01h</td><td>Page 1</td></tr> <tr><td>02h</td><td>Page 2</td></tr> <tr><td>03h</td><td>Page 3</td></tr> <tr><td>04h</td><td>Page 4</td></tr> <tr><td>05h</td><td>Page 5</td></tr> <tr><td>06h</td><td>Page 6</td></tr> <tr><td>07h</td><td>Page 7</td></tr> <tr><td>08h</td><td>Page 8</td></tr> <tr><td>09h</td><td>Page 9</td></tr> <tr><td>0Ah</td><td>Page 10</td></tr> <tr><td>Others</td><td>Reserved</td></tr> </tbody> </table> <p>Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available</p> <p>See section "5.1 Command Flow".</p>											PAGE[7:0]	Command Page	00h	Page 0	01h	Page 1	02h	Page 2	03h	Page 3	04h	Page 4	05h	Page 5	06h	Page 6	07h	Page 7	08h	Page 8	09h	Page 9	0Ah	Page 10	Others	Reserved
	PAGE[7:0]	Command Page																																			
	00h	Page 0																																			
	01h	Page 1																																			
	02h	Page 2																																			
	03h	Page 3																																			
	04h	Page 4																																			
	05h	Page 5																																			
	06h	Page 6																																			
	07h	Page 7																																			
	08h	Page 8																																			
	09h	Page 9																																			
	0Ah	Page 10																																			
Others	Reserved																																				
Restriction	None																																				
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																		
Status	Availability																																				
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Status	Default Value																																				
Power On Sequence	04h																																				
S/W Reset	04h																																				
H/W Reset	04h																																				

5.8. Page 5 Command Description

5.8.1. Fine Digital Gamma Control 1 (00h~5Bh)

Command Page			Page 5								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	1st	W/R	FineOffsetR00[5:0]						GRPR_OP0[9:8]		XX
01h	1st	W/R	GRPR_OP0[7:0]								XX
02h	1st	W/R	FineOffsetR01[5:0]						GRPR_OP1[9:8]		XX
03h	1st	W/R	GRPR_OP1[7:0]								XX
04h	1st	W/R	FineOffsetR02[5:0]						GRPR_OP2[9:8]		XX
05h	1st	W/R	GRPR_OP2[7:0]								XX
06h	1st	W/R	FineOffsetR03[5:0]						GRPR_OP3[9:8]		XX
07h	1st	W/R	GRPR_OP3[7:0]								XX
08h	1st	W/R	FineOffsetR04[5:0]						GRPR_OP4[9:8]		XX
09h	1st	W/R	GRPR_OP4[7:0]								XX
0Ah	1st	W/R	FineOffsetR05[5:0]						GRPR_OP5[9:8]		XX
0Bh	1st	W/R	GRPR_OP5[7:0]								XX
0Ch	1st	W/R	FineOffsetR06[5:0]						GRPR_OP6[9:8]		XX
0Dh	1st	W/R	GRPR_OP6[7:0]								XX
0Eh	1st	W/R	FineOffsetR07[5:0]						GRPR_OP7[9:8]		XX
0Fh	1st	W/R	GRPR_OP7[7:0]								XX
10h	1st	W/R	FineOffsetR08[5:0]						GRPR_OP8[9:8]		XX
11h	1st	W/R	GRPR_OP8[7:0]								XX
12h	1st	W/R	FineOffsetR09[5:0]						GRPR_OP9[9:8]		XX
13h	1st	W/R	GRPR_OP9[7:0]								XX
14h	1st	W/R	FineOffsetR10[5:0]						GRPR_OP10[9:8]		XX
15h	1st	W/R	GRPR_OP10[7:0]								XX
16h	1st	W/R	FineOffsetR11[5:0]						GRPR_OP11[9:8]		XX
17h	1st	W/R	GRPR_OP11[7:0]								XX
18h	1st	W/R	FineOffsetR12[5:0]						GRPR_OP12[9:8]		XX
19h	1st	W/R	GRPR_OP12[7:0]								XX
1Ah	1st	W/R	FineOffsetR13[5:0]						GRPR_OP13[9:8]		XX
1Bh	1st	W/R	GRPR_OP13[7:0]								XX
1Ch	1st	W/R	FineOffsetR14[5:0]						GRPR_OP14[9:8]		XX
1Dh	1st	W/R	GRPR_OP14[7:0]								XX
1Eh	1st	W/R	FineOffsetR15[5:0]						GRPR_OP15[9:8]		XX
1Fh	1st	W/R	GRPR_OP15[7:0]								XX
20h	1st	W/R	FineOffsetR16[5:0]						GRPR_OP16[9:8]		XX
21h	1st	W/R	GRPR_OP16[7:0]								XX
22h	1st	W/R	FineOffsetR17[5:0]						GRPR_OP17[9:8]		XX
23h	1st	W/R	GRPR_OP17[7:0]								XX
24h	1st	W/R	FineOffsetR18[5:0]						GRPR_OP18[9:8]		XX
25h	1st	W/R	GRPR_OP18[7:0]								XX
26h	1st	W/R	FineOffsetR19[5:0]						GRPR_OP19[9:8]		XX
27h	1st	W/R	GRPR_OP19[7:0]								XX
28h	1st	W/R	FineOffsetR20[5:0]						GRPR_OP20[9:8]		XX
29h	1st	W/R	GRPR_OP20[7:0]								XX
2Ah	1st	W/R	FineOffsetR21[5:0]						GRPR_OP21[9:8]		XX
2Bh	1st	W/R	GRPR_OP21[7:0]								XX
2Ch	1st	W/R	FineOffsetR22[5:0]						GRPR_OP22[9:8]		XX
2Dh	1st	W/R	GRPR_OP22[7:0]								XX
2Eh	1st	W/R	FineOffsetR23[5:0]						GRPR_OP23[9:8]		XX
2Fh	1st	W/R	GRPR_OP23[7:0]								XX
30h	1st	W/R	FineOffsetR24[5:0]						GRPR_OP24[9:8]		XX
31h	1st	W/R	GRPR_OP24[7:0]								XX
32h	1st	W/R	FineOffsetR25[5:0]						GRPR_OP25[9:8]		XX

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33h	1st	W/R	GRPR_OP25[7:0]							XX	
34h	1st	W/R	FineOffsetR26[5:0]					GRPR_OP26[9:8]		XX	
35h	1st	W/R	GRPR_OP26[7:0]							XX	
36h	1st	W/R	FineOffsetR27[5:0]					GRPR_OP27[9:8]		XX	
37h	1st	W/R	GRPR_OP27[7:0]							XX	
38h	1st	W/R	FineOffsetR28[5:0]					GRPR_OP28[9:8]		XX	
39h	1st	W/R	GRPR_OP28[7:0]							XX	
3Ah	1st	W/R	0	0	0	0	0	0	GRPR_OP29[9:8]	XX	
3Bh	1st	W/R	GRPR_OP29[7:0]							XX	
3Ch	1st	W/R	0	0	0	0	0	0	GRPR_OP30[9:8]	XX	
3Dh	1st	W/R	GRPR_OP30[7:0]							XX	
3Eh	1st	W/R	0	0	0	0	0	0	GRPR_OP31[9:8]	XX	
3Fh	1st	W/R	GRPR_OP31[7:0]							XX	
40h	1st	W/R	0	0	0	0	0	0	GRPR_OP32[9:8]	XX	
41h	1st	W/R	GRPR_OP32[7:0]							XX	
42h	1st	W/R	0	0	0	0	0	0	GRPR_OP33[9:8]	XX	
43h	1st		GRPR_OP33[7:0]							XX	
44h	1st	W/R	0	0	0	0	0	0	GRPR_OP34[9:8]	XX	
45h	1st		GRPR_OP34[7:0]							XX	
46h	1st	W/R	0	0	0	0	0	0	GRPR_OP35[9:8]	XX	
47h	1st	W/R	GRPR_OP35[7:0]							XX	
48h	1st	W/R	0	0	0	0	0	0	GRPR_OP36[9:8]	XX	
49h	1st	W/R	GRPR_OP36[7:0]							XX	
4Ah	1st	W/R	0	0	0	0	0	0	GRPR_OP37[9:8]	XX	
4Bh	1st	W/R	GRPR_OP37[7:0]							XX	
4Ch	1st	W/R	0	0	0	0	0	0	GRPR_OP38[9:8]	XX	
4Dh	1st	W/R	GRPR_OP38[7:0]							XX	
4Eh	1st	W/R	0	0	0	0	0	0	GRPR_OP39[9:8]	XX	
4Fh	1st	W/R	GRPR_OP39[7:0]							XX	
50h	1st	W/R	0	0	0	0	0	0	GRPR_OP40[9:8]	XX	
51h	1st	W/R	GRPR_OP40[7:0]							XX	
52h	1st	W/R	0	0	0	0	0	0	GRPR_OP41[9:8]	XX	
53h	1st	W/R	GRPR_OP41[7:0]							XX	
54h	1st	W/R	0	0	0	0	0	0	GRPR_OP42[9:8]	XX	
55h	1st	W/R	GRPR_OP42[7:0]							XX	
56h	1st	W/R	0	0	0	0	0	0	GRPR_OP43[9:8]	XX	
57h	1st	W/R	GRPR_OP43[7:0]							XX	
58h	1st	W/R	0	0	0	0	0	0	GRPR_OP44[9:8]	XX	
59h	1st	W/R	GRPR_OP44[7:0]							XX	
5Ah	1st	W/R	0	0	0	0	0	0	GRPR_OP45[9:8]	XX	
5Bh	1st	W/R	GRPR_OP45[7:0]							XX	
FFh	1st	W	1	0	0	1	1	0	0	0	98
	2nd	W	1	0	0	0	0	0	0	1	81
	3rd	W	Page[7:0]							05	
Description		GRPR_OP0[9:0]~GRPR_OP45[9:0]: Digital Gamma Macro-adjustment registers for red gamma curve.									

	<p style="text-align: center;">Setting Digital Gamma Control 1</p> <table border="1" style="margin: auto;"> <tr> <th style="background-color: #00FFFF;">Register Address</th> <th style="background-color: #FFFF00;">1st parameter Device code 1</th> <th style="background-color: #FFFF00;">2nd parameter Device code 2</th> <th style="background-color: #FFDAB9;">3rd parameter Page_select</th> </tr> <tr> <td style="background-color: #FFFF00;">FFh</td> <td style="background-color: #FFFF00;">98h</td> <td style="background-color: #FFFF00;">81h</td> <td style="background-color: #FFDAB9;">05h</td> </tr> </table> <p style="text-align: center;"> Case 1 (The first time to set Digital Gamma Control) </p> <p style="text-align: center;"> Command Sequence (by order) Set register 00h = XXh Set register 01h = XXh . . Set register 5Bh = XXh XXh = Digital Gamma adjustment </p> <p style="text-align: center;"> One pair of commands(even and odd) must be written for a revised digital gamma point Example: modify GRPR_OP26 = 123h 123h = Digital Gamma adjustment Step1: set register 34h(even) = 01h Step2: set register 35h(odd) = 23h (Other registers still keep original value) </p> <p style="text-align: center;"> Digital Gamma Control 1 Setting finished </p> <p style="text-align: center;"> Case 2 </p>	Register Address	1st parameter Device code 1	2nd parameter Device code 2	3rd parameter Page_select	FFh	98h	81h	05h
Register Address	1st parameter Device code 1	2nd parameter Device code 2	3rd parameter Page_select						
FFh	98h	81h	05h						
<p>Restriction</p>	<p>None</p>								
<p>Register Availability</p>	<table border="1" style="margin: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability								
Normal Mode On, Idle Mode Off, Sleep Out	Yes								
Normal Mode On, Idle Mode On, Sleep Out	Yes								
Sleep In	Yes								
<p>Default</p>	<table border="1" style="margin: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h_00h...00h_00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h_00h...00h_00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h_00h...00h_00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h_00h...00h_00h	S/W Reset	00h_00h...00h_00h	H/W Reset	00h_00h...00h_00h
Status	Default Value								
Power On Sequence	00h_00h...00h_00h								
S/W Reset	00h_00h...00h_00h								
H/W Reset	00h_00h...00h_00h								

5.8.2. Digital 3 Gamma Enable (85h)

Command Page			Page 5																
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default								
85h	1st	W/R	0	1	0	0	EN_3G	0	0	0	40h								
Description	En_3G: 0 : digital 3 gamma disable 1 : digital 3 gamma enable																		
Restriction	None																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In	Yes																		
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value (Before OTP program)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>40h</td> </tr> <tr> <td>S/W Reset</td> <td>40h</td> </tr> <tr> <td>H/W Reset</td> <td>40h</td> </tr> </tbody> </table>											Status	Default Value (Before OTP program)	Power On Sequence	40h	S/W Reset	40h	H/W Reset	40h
Status	Default Value (Before OTP program)																		
Power On Sequence	40h																		
S/W Reset	40h																		
H/W Reset	40h																		

5.8.3. EXTC Command Set Enable Register (FFh)

Command Page			Page 5																																		
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																										
FFh	1st	W	1	0	0	1	1	0	0	0	98h																										
	2nd	W	1	0	0	0	0	0	0	1	81h																										
	3rd	W	PAGE[7:0]								05h																										
Description	<p>PAGE[7:0]: Set the command page.</p> <table border="1"> <thead> <tr> <th>PAGE[7:0]</th> <th>Command Page</th> </tr> </thead> <tbody> <tr><td>00h</td><td>Page 0</td></tr> <tr><td>01h</td><td>Page 1</td></tr> <tr><td>02h</td><td>Page 2</td></tr> <tr><td>03h</td><td>Page 3</td></tr> <tr><td>04h</td><td>Page 4</td></tr> <tr><td>05h</td><td>Page 5</td></tr> <tr><td>06h</td><td>Page 6</td></tr> <tr><td>07h</td><td>Page 7</td></tr> <tr><td>08h</td><td>Page 8</td></tr> <tr><td>09h</td><td>Page 9</td></tr> <tr><td>0Ah</td><td>Page 10</td></tr> <tr><td>Others</td><td>Reserved</td></tr> </tbody> </table> <p>Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available</p> <p>See section "5.1 Command Flow".</p>											PAGE[7:0]	Command Page	00h	Page 0	01h	Page 1	02h	Page 2	03h	Page 3	04h	Page 4	05h	Page 5	06h	Page 6	07h	Page 7	08h	Page 8	09h	Page 9	0Ah	Page 10	Others	Reserved
	PAGE[7:0]	Command Page																																			
	00h	Page 0																																			
	01h	Page 1																																			
	02h	Page 2																																			
	03h	Page 3																																			
	04h	Page 4																																			
	05h	Page 5																																			
	06h	Page 6																																			
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	08h	Page 8																																			
	09h	Page 9																																			
	0Ah	Page 10																																			
Others	Reserved																																				
Restriction	None																																				
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Status	Availability																																				
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																				
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Status	Default Value																																				
Power On Sequence	05h																																				
S/W Reset	05h																																				
H/W Reset	05h																																				

5.9. Page 6 Command Description

5.9.1. Fine Digital Gamma Control 2 (00h~5Bh)

Command Page			Page 6								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	1st	W/R	FineOffsetG00[5:0]						GRPG_OP0[9:8]		XX
01h	1st	W/R	GRPG_OP0[7:0]								XX
02h	1st	W/R	FineOffsetG01[5:0]						GRPG_OP1[9:8]		XX
03h	1st	W/R	GRPG_OP1[7:0]								XX
04h	1st	W/R	FineOffsetG02[5:0]						GRPG_OP2[9:8]		XX
05h	1st	W/R	GRPG_OP2[7:0]								XX
06h	1st	W/R	FineOffsetG03[5:0]						GRPG_OP3[9:8]		XX
07h	1st	W/R	GRPG_OP3[7:0]								XX
08h	1st	W/R	FineOffsetG04[5:0]						GRPG_OP4[9:8]		XX
09h	1st	W/R	GRPG_OP4[7:0]								XX
0Ah	1st	W/R	FineOffsetG05[5:0]						GRPG_OP5[9:8]		XX
0Bh	1st	W/R	GRPG_OP5[7:0]								XX
0Ch	1st	W/R	FineOffsetG06[5:0]						GRPG_OP6[9:8]		XX
0Dh	1st	W/R	GRPG_OP6[7:0]								XX
0Eh	1st	W/R	FineOffsetG07[5:0]						GRPG_OP7[9:8]		XX
0Fh	1st	W/R	GRPG_OP7[7:0]								XX
10h	1st	W/R	FineOffsetG08[5:0]						GRPG_OP8[9:8]		XX
11h	1st	W/R	GRPG_OP8[7:0]								XX
12h	1st	W/R	FineOffsetG09[5:0]						GRPG_OP9[9:8]		XX
13h	1st	W/R	GRPG_OP9[7:0]								XX
14h	1st	W/R	FineOffsetG10[5:0]						GRPG_OP10[9:8]		XX
15h	1st	W/R	GRPG_OP10[7:0]								XX
16h	1st	W/R	FineOffsetG11[5:0]						GRPG_OP11[9:8]		XX
17h	1st	W/R	GRPG_OP11[7:0]								XX
18h	1st	W/R	FineOffsetG12[5:0]						GRPG_OP12[9:8]		XX
19h	1st	W/R	GRPG_OP12[7:0]								XX
1Ah	1st	W/R	FineOffsetG13[5:0]						GRPG_OP13[9:8]		XX
1Bh	1st	W/R	GRPG_OP13[7:0]								XX
1Ch	1st	W/R	FineOffsetG14[5:0]						GRPG_OP14[9:8]		XX
1Dh	1st	W/R	GRPG_OP14[7:0]								XX
1Eh	1st	W/R	FineOffsetG15[5:0]						GRPG_OP15[9:8]		XX
1Fh	1st	W/R	GRPG_OP15[7:0]								XX
20h	1st	W/R	FineOffsetG16[5:0]						GRPG_OP16[9:8]		XX
21h	1st	W/R	GRPG_OP16[7:0]								XX
22h	1st	W/R	FineOffsetG17[5:0]						GRPG_OP17[9:8]		XX
23h	1st	W/R	GRPG_OP17[7:0]								XX
24h	1st	W/R	FineOffsetG18[5:0]						GRPG_OP18[9:8]		XX
25h	1st	W/R	GRPG_OP18[7:0]								XX
26h	1st	W/R	FineOffsetG19[5:0]						GRPG_OP19[9:8]		XX
27h	1st	W/R	GRPG_OP19[7:0]								XX
28h	1st	W/R	FineOffsetG20[5:0]						GRPG_OP20[9:8]		XX
29h	1st	W/R	GRPG_OP20[7:0]								XX
2Ah	1st	W/R	FineOffsetG21[5:0]						GRPG_OP21[9:8]		XX
2Bh	1st	W/R	GRPG_OP21[7:0]								XX
2Ch	1st	W/R	FineOffsetG22[5:0]						GRPG_OP22[9:8]		XX
2Dh	1st	W/R	GRPG_OP22[7:0]								XX
2Eh	1st	W/R	FineOffsetG23[5:0]						GRPG_OP23[9:8]		XX
2Fh	1st	W/R	GRPG_OP23[7:0]								XX
30h	1st	W/R	FineOffsetG24[5:0]						GRPG_OP24[9:8]		XX
31h	1st	W/R	GRPG_OP24[7:0]								XX
32h	1st	W/R	FineOffsetG25[5:0]						GRPG_OP25[9:8]		XX

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33h	1st	W/R	GRPG_OP25[7:0]							XX	
34h	1st	W/R	FineOffsetG26[5:0]				GRPG_OP26[9:8]			XX	
35h	1st	W/R	GRPG_OP26[7:0]							XX	
36h	1st	W/R	FineOffsetG27[5:0]				GRPG_OP27[9:8]			XX	
37h	1st	W/R	GRPG_OP27[7:0]							XX	
38h	1st	W/R	FineOffsetG28[5:0]				GRPG_OP28[9:8]			XX	
39h	1st	W/R	GRPG_OP28[7:0]							XX	
3Ah	1st	W/R	0	0	0	0	0	0	GRPG_OP29[9:8]	XX	
3Bh	1st	W/R	GRPG_OP29[7:0]							XX	
3Ch	1st	W/R	0	0	0	0	0	0	GRPG_OP30[9:8]	XX	
3Dh	1st	W/R	GRPG_OP30[7:0]							XX	
3Eh	1st	W/R	0	0	0	0	0	0	GRPG_OP31[9:8]	XX	
3Fh	1st	W/R	GRPG_OP31[7:0]							XX	
40h	1st	W/R	0	0	0	0	0	0	GRPG_OP32[9:8]	XX	
41h	1st	W/R	GRPG_OP32[7:0]							XX	
42h	1st	W/R	0	0	0	0	0	0	GRPG_OP33[9:8]	XX	
43h	1st		GRPG_OP33[7:0]							XX	
44h	1st	W/R	0	0	0	0	0	0	GRPG_OP34[9:8]	XX	
45h	1st		GRPG_OP34[7:0]							XX	
46h	1st	W/R	0	0	0	0	0	0	GRPG_OP35[9:8]	XX	
47h	1st	W/R	GRPG_OP35[7:0]							XX	
48h	1st	W/R	0	0	0	0	0	0	GRPG_OP36[9:8]	XX	
49h	1st	W/R	GRPG_OP36[7:0]							XX	
4Ah	1st	W/R	0	0	0	0	0	0	GRPG_OP37[9:8]	XX	
4Bh	1st	W/R	GRPG_OP37[7:0]							XX	
4Ch	1st	W/R	0	0	0	0	0	0	GRPG_OP38[9:8]	XX	
4Dh	1st	W/R	GRPG_OP38[7:0]							XX	
4Eh	1st	W/R	0	0	0	0	0	0	GRPG_OP39[9:8]	XX	
4Fh	1st	W/R	GRPG_OP39[7:0]							XX	
50h	1st	W/R	0	0	0	0	0	0	GRPG_OP40[9:8]	XX	
51h	1st	W/R	GRPG_OP40[7:0]							XX	
52h	1st	W/R	0	0	0	0	0	0	GRPG_OP41[9:8]	XX	
53h	1st	W/R	GRPG_OP41[7:0]							XX	
54h	1st	W/R	0	0	0	0	0	0	GRPG_OP42[9:8]	XX	
55h	1st	W/R	GRPG_OP42[7:0]							XX	
56h	1st	W/R	0	0	0	0	0	0	GRPG_OP43[9:8]	XX	
57h	1st	W/R	GRPG_OP43[7:0]							XX	
58h	1st	W/R	0	0	0	0	0	0	GRPG_OP44[9:8]	XX	
59h	1st	W/R	GRPG_OP44[7:0]							XX	
5Ah	1st	W/R	0	0	0	0	0	0	GRPG_OP45[9:8]	XX	
5Bh	1st	W/R	GRPG_OP45[7:0]							XX	
FFh	1st	W	1	0	0	1	1	0	0	0	98
	2nd	W	1	0	0	0	0	0	0	1	81
	3rd	W	Page[7:0]							06	
Description		GRPG_OP0[9:0]~GRPG_OP45[9:0]: Digital Gamma Macro-adjustment registers for green gamma curve.									

	<div style="text-align: center;"> <p>Setting Digital Gamma Control 2</p> <table border="1" style="margin: 0 auto;"> <tr> <th style="background-color: #00FFFF;">Register Address</th> <th style="background-color: #FFFF00;">1st parameter Device code 1</th> <th style="background-color: #FFFF00;">2nd parameter Device code 2</th> <th style="background-color: #FFDAB9;">3rd parameter Page_select</th> </tr> <tr> <td style="background-color: #FFFF00;">FFh</td> <td style="background-color: #FFFF00;">98h</td> <td style="background-color: #FFFF00;">81h</td> <td style="background-color: #FFDAB9;">06h</td> </tr> </table> <p>Case 2</p> <p style="color: red;">Case 1 (The first time to set Digital Gamma Control)</p> <div style="border: 1px solid black; padding: 5px; margin: 5px auto; width: 80%;"> <p>Command Sequence (by order)</p> <p>Set register 00h = XXh</p> <p>Set register 01h = XXh</p> <p style="text-align: center;">.</p> <p>Set register 5Bh = XXh</p> <p>XXh = Digital Gamma adjustment</p> </div> <div style="border: 1px solid black; padding: 5px; margin: 5px auto; width: 80%;"> <p>One pair of commands(even and odd) must be written for a revised digital gamma point</p> <p>Example: modify GRPG_OP26 = 123h</p> <p>123h = Digital Gamma adjustment</p> <p>Step1: set register 34h(even) = 01h</p> <p>Step2: set register 35h(odd) = 23h</p> <p style="color: red;">(Other registers still keep original value)</p> </div> <p>Digital Gamma Control 2 Setting finished</p> </div>	Register Address	1st parameter Device code 1	2nd parameter Device code 2	3rd parameter Page_select	FFh	98h	81h	06h
Register Address	1st parameter Device code 1	2nd parameter Device code 2	3rd parameter Page_select						
FFh	98h	81h	06h						
<p>Restriction</p>	<p>None</p>								
<p>Register Availability</p>	<table border="1" style="margin: 0 auto;"> <thead> <tr> <th style="background-color: #A9A9A9;">Status</th> <th style="background-color: #A9A9A9;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability								
Normal Mode On, Idle Mode Off, Sleep Out	Yes								
Normal Mode On, Idle Mode On, Sleep Out	Yes								
Sleep In	Yes								
<p>Default</p>	<table border="1" style="margin: 0 auto;"> <thead> <tr> <th style="background-color: #A9A9A9;">Status</th> <th style="background-color: #A9A9A9;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h_00h...00h_00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h_00h...00h_00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h_00h...00h_00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h_00h...00h_00h	S/W Reset	00h_00h...00h_00h	H/W Reset	00h_00h...00h_00h
Status	Default Value								
Power On Sequence	00h_00h...00h_00h								
S/W Reset	00h_00h...00h_00h								
H/W Reset	00h_00h...00h_00h								

5.9.2. EXTC Command Set Enable Register (FFh)

Command Page			Page 6																																		
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																										
FFh	1st	W	1	0	0	1	1	0	0	0	98h																										
	2nd	W	1	0	0	0	0	0	0	1	81h																										
	3rd	W	PAGE[7:0]								06h																										
Description	<p>PAGE[7:0]: Set the command page.</p> <table border="1"> <thead> <tr> <th>PAGE[7:0]</th> <th>Command Page</th> </tr> </thead> <tbody> <tr><td>00h</td><td>Page 0</td></tr> <tr><td>01h</td><td>Page 1</td></tr> <tr><td>02h</td><td>Page 2</td></tr> <tr><td>03h</td><td>Page 3</td></tr> <tr><td>04h</td><td>Page 4</td></tr> <tr><td>05h</td><td>Page 5</td></tr> <tr><td>06h</td><td>Page 6</td></tr> <tr><td>07h</td><td>Page 7</td></tr> <tr><td>08h</td><td>Page 8</td></tr> <tr><td>09h</td><td>Page 9</td></tr> <tr><td>0Ah</td><td>Page 10</td></tr> <tr><td>Others</td><td>Reserved</td></tr> </tbody> </table> <p>Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available</p> <p>See section "5.1 Command Flow".</p>											PAGE[7:0]	Command Page	00h	Page 0	01h	Page 1	02h	Page 2	03h	Page 3	04h	Page 4	05h	Page 5	06h	Page 6	07h	Page 7	08h	Page 8	09h	Page 9	0Ah	Page 10	Others	Reserved
	PAGE[7:0]	Command Page																																			
	00h	Page 0																																			
	01h	Page 1																																			
	02h	Page 2																																			
	03h	Page 3																																			
	04h	Page 4																																			
	05h	Page 5																																			
	06h	Page 6																																			
	07h	Page 7																																			
	08h	Page 8																																			
	09h	Page 9																																			
	0Ah	Page 10																																			
Others	Reserved																																				
Restriction	None																																				
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																		
Status	Availability																																				
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																				
Normal Mode On, Idle Mode On, Sleep Out	Yes																																				
Sleep In	Yes																																				
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>06h</td> </tr> <tr> <td>S/W Reset</td> <td>06h</td> </tr> <tr> <td>H/W Reset</td> <td>06h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	06h	S/W Reset	06h	H/W Reset	06h																		
Status	Default Value																																				
Power On Sequence	06h																																				
S/W Reset	06h																																				
H/W Reset	06h																																				

5.10. Page 7 Command Description

5.10.1. Fine Digital Gamma Control 3 (00h~5Bh)

Command Page			Page 7								
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	1st	W/R	FineOffsetB00[5:0]						GRPB_OP0[9:8]		XX
01h	1st	W/R	GRPB_OP0[7:0]								XX
02h	1st	W/R	FineOffsetB01[5:0]						GRPB_OP1[9:8]		XX
03h	1st	W/R	GRPB_OP1[7:0]								XX
04h	1st	W/R	FineOffsetB02[5:0]						GRPB_OP2[9:8]		XX
05h	1st	W/R	GRPB_OP2[7:0]								XX
06h	1st	W/R	FineOffsetB03[5:0]						GRPB_OP3[9:8]		XX
07h	1st	W/R	GRPB_OP3[7:0]								XX
08h	1st	W/R	FineOffsetB04[5:0]						GRPB_OP4[9:8]		XX
09h	1st	W/R	GRPB_OP4[7:0]								XX
0Ah	1st	W/R	FineOffsetB05[5:0]						GRPB_OP5[9:8]		XX
0Bh	1st	W/R	GRPB_OP5[7:0]								XX
0Ch	1st	W/R	FineOffsetB06[5:0]						GRPB_OP6[9:8]		XX
0Dh	1st	W/R	GRPB_OP6[7:0]								XX
0Eh	1st	W/R	FineOffsetB07[5:0]						GRPB_OP7[9:8]		XX
0Fh	1st	W/R	GRPB_OP7[7:0]								XX
10h	1st	W/R	FineOffsetB08[5:0]						GRPB_OP8[9:8]		XX
11h	1st	W/R	GRPB_OP8[7:0]								XX
12h	1st	W/R	FineOffsetB09[5:0]						GRPB_OP9[9:8]		XX
13h	1st	W/R	GRPB_OP9[7:0]								XX
14h	1st	W/R	FineOffsetB10[5:0]						GRPB_OP10[9:8]		XX
15h	1st	W/R	GRPB_OP10[7:0]								XX
16h	1st	W/R	FineOffsetB11[5:0]						GRPB_OP11[9:8]		XX
17h	1st	W/R	GRPB_OP11[7:0]								XX
18h	1st	W/R	FineOffsetB12[5:0]						GRPB_OP12[9:8]		XX
19h	1st	W/R	GRPB_OP12[7:0]								XX
1Ah	1st	W/R	FineOffsetB13[5:0]						GRPB_OP13[9:8]		XX
1Bh	1st	W/R	GRPB_OP13[7:0]								XX
1Ch	1st	W/R	FineOffsetB14[5:0]						GRPB_OP14[9:8]		XX
1Dh	1st	W/R	GRPB_OP14[7:0]								XX
1Eh	1st	W/R	FineOffsetB15[5:0]						GRPB_OP15[9:8]		XX
1Fh	1st	W/R	GRPB_OP15[7:0]								XX
20h	1st	W/R	FineOffsetB16[5:0]						GRPB_OP16[9:8]		XX
21h	1st	W/R	GRPB_OP16[7:0]								XX
22h	1st	W/R	FineOffsetB17[5:0]						GRPB_OP17[9:8]		XX
23h	1st	W/R	GRPB_OP17[7:0]								XX
24h	1st	W/R	FineOffsetB18[5:0]						GRPB_OP18[9:8]		XX
25h	1st	W/R	GRPB_OP18[7:0]								XX
26h	1st	W/R	FineOffsetB19[5:0]						GRPB_OP19[9:8]		XX
27h	1st	W/R	GRPB_OP19[7:0]								XX
28h	1st	W/R	FineOffsetB20[5:0]						GRPB_OP20[9:8]		XX
29h	1st	W/R	GRPB_OP20[7:0]								XX
2Ah	1st	W/R	FineOffsetB21[5:0]						GRPB_OP21[9:8]		XX
2Bh	1st	W/R	GRPB_OP21[7:0]								XX
2Ch	1st	W/R	FineOffsetB22[5:0]						GRPB_OP22[9:8]		XX
2Dh	1st	W/R	GRPB_OP22[7:0]								XX
2Eh	1st	W/R	FineOffsetB23[5:0]						GRPB_OP23[9:8]		XX
2Fh	1st	W/R	GRPB_OP23[7:0]								XX
30h	1st	W/R	FineOffsetB24[5:0]						GRPB_OP24[9:8]		XX
31h	1st	W/R	GRPB_OP24[7:0]								XX
32h	1st	W/R	FineOffsetB25[5:0]						GRPB_OP25[9:8]		XX

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33h	1st	W/R	GRP_B_OP25[7:0]							XX	
34h	1st	W/R	FineOffsetB26[5:0]				GRP_B_OP26[9:8]			XX	
35h	1st	W/R	GRP_B_OP26[7:0]							XX	
36h	1st	W/R	FineOffsetB27[5:0]				GRP_B_OP27[9:8]			XX	
37h	1st	W/R	GRP_B_OP27[7:0]							XX	
38h	1st	W/R	FineOffsetB28[5:0]				GRP_B_OP28[9:8]			XX	
39h	1st	W/R	GRP_B_OP28[7:0]							XX	
3Ah	1st	W/R	0	0	0	0	0	0	GRP_B_OP29[9:8]	XX	
3Bh	1st	W/R	GRP_B_OP29[7:0]							XX	
3Ch	1st	W/R	0	0	0	0	0	0	GRP_B_OP30[9:8]	XX	
3Dh	1st	W/R	GRP_B_OP30[7:0]							XX	
3Eh	1st	W/R	0	0	0	0	0	0	GRP_B_OP31[9:8]	XX	
3Fh	1st	W/R	GRP_B_OP31[7:0]							XX	
40h	1st	W/R	0	0	0	0	0	0	GRP_B_OP32[9:8]	XX	
41h	1st	W/R	GRP_B_OP32[7:0]							XX	
42h	1st	W/R	0	0	0	0	0	0	GRP_B_OP33[9:8]	XX	
43h	1st		GRP_B_OP33[7:0]							XX	
44h	1st	W/R	0	0	0	0	0	0	GRP_B_OP34[9:8]	XX	
45h	1st		GRP_B_OP34[7:0]							XX	
46h	1st	W/R	0	0	0	0	0	0	GRP_B_OP35[9:8]	XX	
47h	1st	W/R	GRP_B_OP35[7:0]							XX	
48h	1st	W/R	0	0	0	0	0	0	GRP_B_OP36[9:8]	XX	
49h	1st	W/R	GRP_B_OP36[7:0]							XX	
4Ah	1st	W/R	0	0	0	0	0	0	GRP_B_OP37[9:8]	XX	
4Bh	1st	W/R	GRP_B_OP37[7:0]							XX	
4Ch	1st	W/R	0	0	0	0	0	0	GRP_B_OP38[9:8]	XX	
4Dh	1st	W/R	GRP_B_OP38[7:0]							XX	
4Eh	1st	W/R	0	0	0	0	0	0	GRP_B_OP39[9:8]	XX	
4Fh	1st	W/R	GRP_B_OP39[7:0]							XX	
50h	1st	W/R	0	0	0	0	0	0	GRP_B_OP40[9:8]	XX	
51h	1st	W/R	GRP_B_OP40[7:0]							XX	
52h	1st	W/R	0	0	0	0	0	0	GRP_B_OP41[9:8]	XX	
53h	1st	W/R	GRP_B_OP41[7:0]							XX	
54h	1st	W/R	0	0	0	0	0	0	GRP_B_OP42[9:8]	XX	
55h	1st	W/R	GRP_B_OP42[7:0]							XX	
56h	1st	W/R	0	0	0	0	0	0	GRP_B_OP43[9:8]	XX	
57h	1st	W/R	GRP_B_OP43[7:0]							XX	
58h	1st	W/R	0	0	0	0	0	0	GRP_B_OP44[9:8]	XX	
59h	1st	W/R	GRP_B_OP44[7:0]							XX	
5Ah	1st	W/R	0	0	0	0	0	0	GRP_B_OP45[9:8]	XX	
5Bh	1st	W/R	GRP_B_OP45[7:0]							XX	
FFh	1st	W	1	0	0	1	1	0	0	0	98
	2nd	W	1	0	0	0	0	0	0	1	81
	3rd	W	Page[7:0]							07	
Description		GRP_B_OP0[9:0]~GRP_B_OP45[9:0]: Digital Gamma Macro-adjustment registers for blue gamma curve.									

	<div style="text-align: center;"> <p>Setting Digital Gamma Control 3</p> <table border="1" style="margin: 10px auto;"> <thead> <tr> <th style="background-color: #00FFFF;">Register Address</th> <th style="background-color: #FFFF00;">1st parameter Device code 1</th> <th style="background-color: #FFFF00;">2nd parameter Device code 2</th> <th style="background-color: #FFDAB9;">3rd parameter Page_select</th> </tr> </thead> <tbody> <tr> <td style="background-color: #FFFF00;">FFh</td> <td style="background-color: #FFFF00;">98h</td> <td style="background-color: #FFFF00;">81h</td> <td style="background-color: #FFDAB9;">07h</td> </tr> </tbody> </table> <p>Case 2</p> <p style="text-align: center;">Case 1 (The first time to set Digital Gamma Control)</p> <div style="border: 1px solid black; padding: 5px; margin: 5px auto; width: 80%;"> <p>Command Sequence (by order)</p> <p>Set register 00h = XXh</p> <p>Set register 01h = XXh</p> <p style="text-align: center;">.</p> <p>Set register 5Bh = XXh</p> <p>XXh = Digital Gamma adjustment</p> </div> <div style="border: 1px solid black; padding: 5px; margin: 5px auto; width: 80%;"> <p>One pair of commands(even and odd) must be written for a revised digital gamma point</p> <p>Example: modify GRPB_OP26 = 123h</p> <p>123h = Digital Gamma adjustment</p> <p>Step1: set register 34h(even) = 01h</p> <p>Step2: set register 35h(odd) = 23h</p> <p style="color: red;">(Other registers still keep original value)</p> </div> <p>Digital Gamma Control 3 Setting finished</p> </div>	Register Address	1st parameter Device code 1	2nd parameter Device code 2	3rd parameter Page_select	FFh	98h	81h	07h
Register Address	1st parameter Device code 1	2nd parameter Device code 2	3rd parameter Page_select						
FFh	98h	81h	07h						
<p>Restriction</p>	<p>None</p>								
<p>Register Availability</p>	<table border="1" style="margin: 10px auto;"> <thead> <tr> <th style="background-color: #A9A9A9;">Status</th> <th style="background-color: #A9A9A9;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability								
Normal Mode On, Idle Mode Off, Sleep Out	Yes								
Normal Mode On, Idle Mode On, Sleep Out	Yes								
Sleep In	Yes								
<p>Default</p>	<table border="1" style="margin: 10px auto;"> <thead> <tr> <th style="background-color: #A9A9A9;">Status</th> <th style="background-color: #A9A9A9;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>00h_00h...00h_00h</td> </tr> <tr> <td>S/W Reset</td> <td>00h_00h...00h_00h</td> </tr> <tr> <td>H/W Reset</td> <td>00h_00h...00h_00h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	00h_00h...00h_00h	S/W Reset	00h_00h...00h_00h	H/W Reset	00h_00h...00h_00h
Status	Default Value								
Power On Sequence	00h_00h...00h_00h								
S/W Reset	00h_00h...00h_00h								
H/W Reset	00h_00h...00h_00h								

5.10.2. EXTC Command Set Enable Register (FFh)

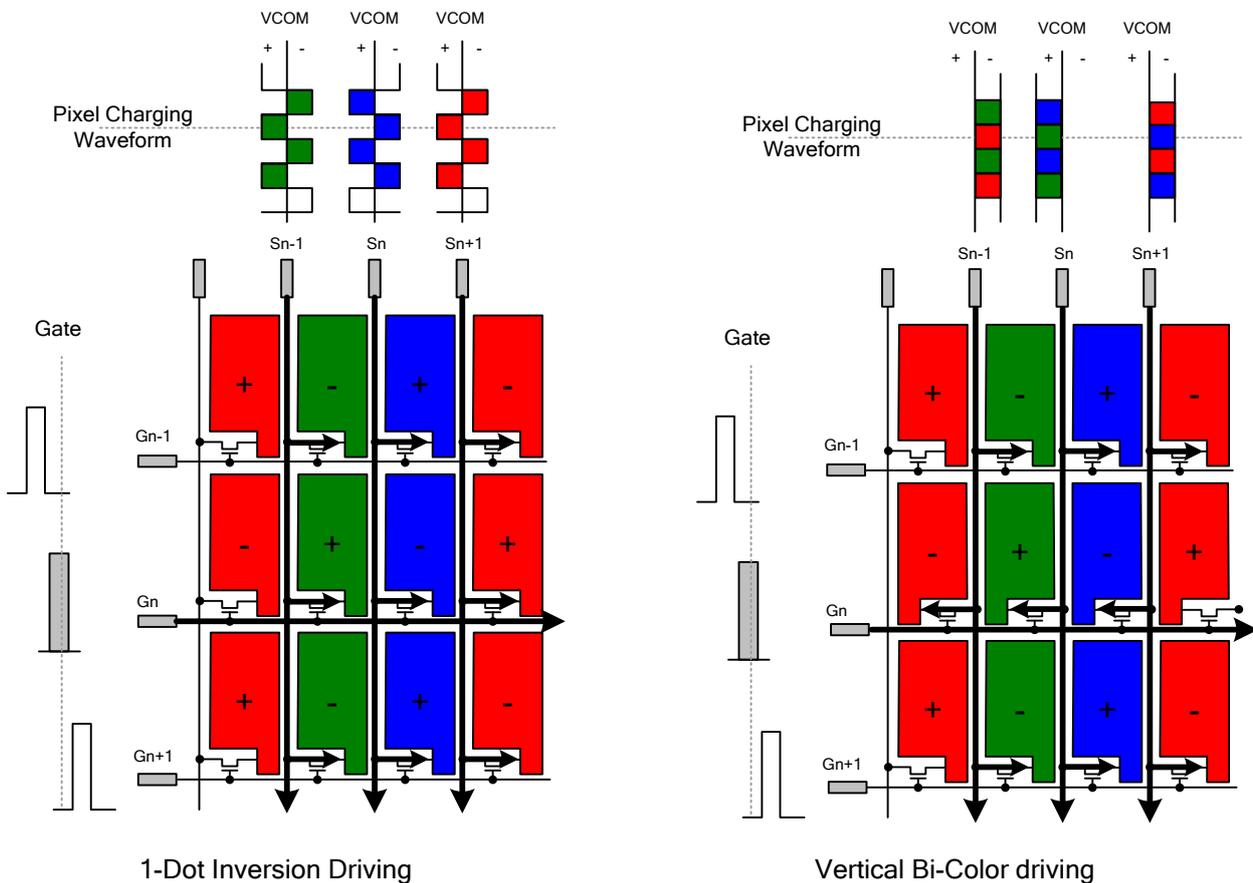
Command Page			Page 7																																		
Address	Parameter	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Default																										
FFh	1st	W	1	0	0	1	1	0	0	0	98h																										
	2nd	W	1	0	0	0	0	0	0	1	81h																										
	3rd	W	PAGE[7:0]								07h																										
Description	<p>PAGE[7:0]: Set the command page.</p> <table border="1"> <thead> <tr> <th>PAGE[7:0]</th> <th>Command Page</th> </tr> </thead> <tbody> <tr><td>00h</td><td>Page 0</td></tr> <tr><td>01h</td><td>Page 1</td></tr> <tr><td>02h</td><td>Page 2</td></tr> <tr><td>03h</td><td>Page 3</td></tr> <tr><td>04h</td><td>Page 4</td></tr> <tr><td>05h</td><td>Page 5</td></tr> <tr><td>06h</td><td>Page 6</td></tr> <tr><td>07h</td><td>Page 7</td></tr> <tr><td>08h</td><td>Page 8</td></tr> <tr><td>09h</td><td>Page 9</td></tr> <tr><td>0Ah</td><td>Page 10</td></tr> <tr><td>Others</td><td>Reserved</td></tr> </tbody> </table> <p>Set the register, 1st Parameter = 98h, 2nd Parameter = 81h, 3rd Parameter = Page value to enable "Page command set" available</p> <p>See section "5.1 Command Flow".</p>											PAGE[7:0]	Command Page	00h	Page 0	01h	Page 1	02h	Page 2	03h	Page 3	04h	Page 4	05h	Page 5	06h	Page 6	07h	Page 7	08h	Page 8	09h	Page 9	0Ah	Page 10	Others	Reserved
	PAGE[7:0]	Command Page																																			
	00h	Page 0																																			
	01h	Page 1																																			
	02h	Page 2																																			
	03h	Page 3																																			
	04h	Page 4																																			
	05h	Page 5																																			
	06h	Page 6																																			
	07h	Page 7																																			
	08h	Page 8																																			
	09h	Page 9																																			
	0Ah	Page 10																																			
Others	Reserved																																				
Restriction	None																																				
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																		
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Sleep In	Yes																																				
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>07h</td> </tr> <tr> <td>S/W Reset</td> <td>07h</td> </tr> <tr> <td>H/W Reset</td> <td>07h</td> </tr> </tbody> </table>											Status	Default Value	Power On Sequence	07h	S/W Reset	07h	H/W Reset	07h																		
Status	Default Value																																				
Power On Sequence	07h																																				
S/W Reset	07h																																				
H/W Reset	07h																																				

6. Source Driver

The source driver uses 2402 channels (S1~S2400 and SDUM[2:1] channels) for the Zig-zag function used for driving the source line of the TFT LCD panel. The source driver converts the digital data into the analog voltage and generates corresponding gray scale voltage output, enabling up to 16.7M colors to be displayed simultaneously. The output circuit of this source driver incorporates an operational amplifier, so that a positive and a negative voltage can be alternately outputted from each channel.

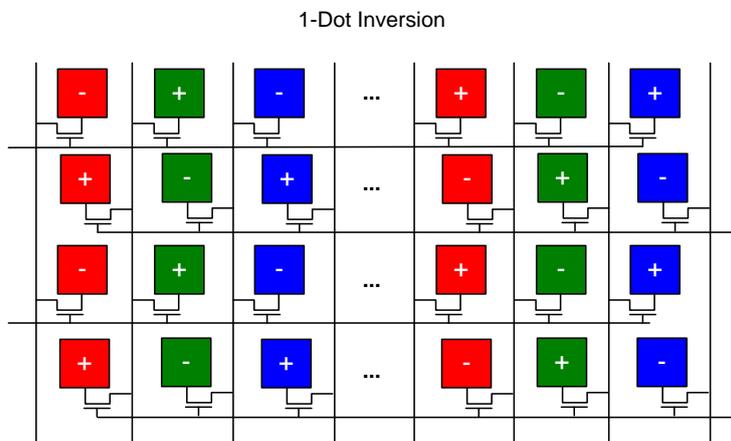
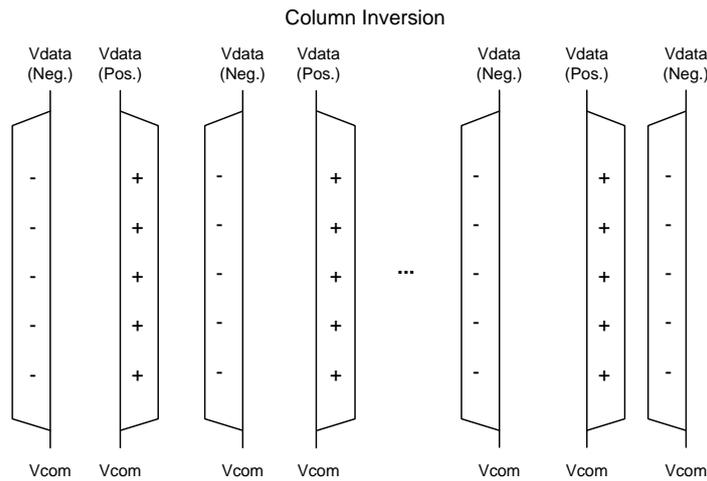
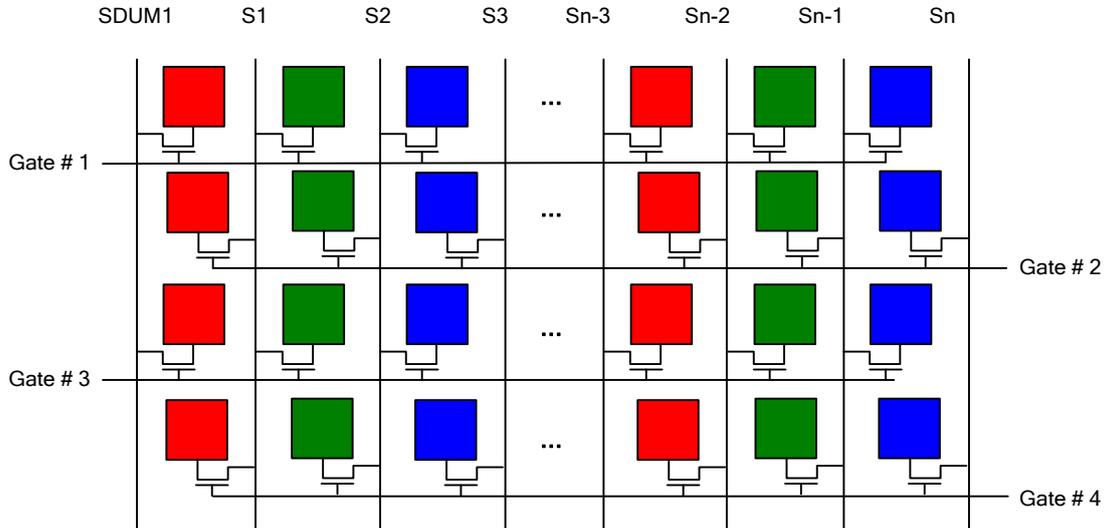
6.1. Zig-zag Inversion

Zig-zag Inversion is used to reduce the power consumption. The Zig-zag inversion decreases the switching frequency of the source related to the magnitude of power consumption. This method will have an addendum data line, SDUM.



6.2. Zig-zag Inversion Concept

The Zig-zag method uses the same polarity of data line of the column inversion to show the 1-dot inversion.



6.3. Zig-zag Inversion Source Output Method

The driving panel display method adds one sub-pixel at the Gate_Even to shift the data output.

(At the Gate_Even line, an additional data line is utilized.)

Red Pattern

	SDUM1	S1	S2	S3	S4	S5
Gate_Odd	R1	G1	B1	R2	G2	B2
Gate_Even		R1	G1	B1	R2	G2
Gate_Odd	R1	G1	B1	R2	G2	B2
Gate_Even		R1	G1	B1	R2	G2
Gate_Odd	R1	G1	B1	R2	G2	B2
Gate_Even		R1	G1	B1	R2	G2

	Sn-5	Sn-4	Sn-3	Sn-2	Sn-1	Sn
Gx-1	Bx-1	Rx	Gx	Bx		
Rx-1	Gx-1	Bx-1	Rx	Gx	Bx	
Gx-1	Bx-1	Rx	Gx	Bx		
Rx-1	Gx-1	Bx-1	Rx	Gx	Bx	
Gx-1	Bx-1	Rx	Gx	Bx		
Rx-1	Gx-1	Bx-1	Rx	Gx	Bx	

Green Pattern

	SDUM1	S1	S2	S3	S4	S5
Gate_Odd	R1	G1	B1	R2	G2	B2
Gate_Even		R1	G1	B1	R2	G2
Gate_Odd	R1	G1	B1	R2	G2	B2
Gate_Even		R1	G1	B1	R2	G2
Gate_Odd	R1	G1	B1	R2	G2	B2
Gate_Even		R1	G1	B1	R2	G2

	Sn-5	Sn-4	Sn-3	Sn-2	Sn-1	Sn
Gx-1	Bx-1	Rx	Gx	Bx		
Rx-1	Gx-1	Bx-1	Rx	Gx	Bx	
Gx-1	Bx-1	Rx	Gx	Bx		
Rx-1	Gx-1	Bx-1	Rx	Gx	Bx	
Gx-1	Bx-1	Rx	Gx	Bx		
Rx-1	Gx-1	Bx-1	Rx	Gx	Bx	

Blue Pattern

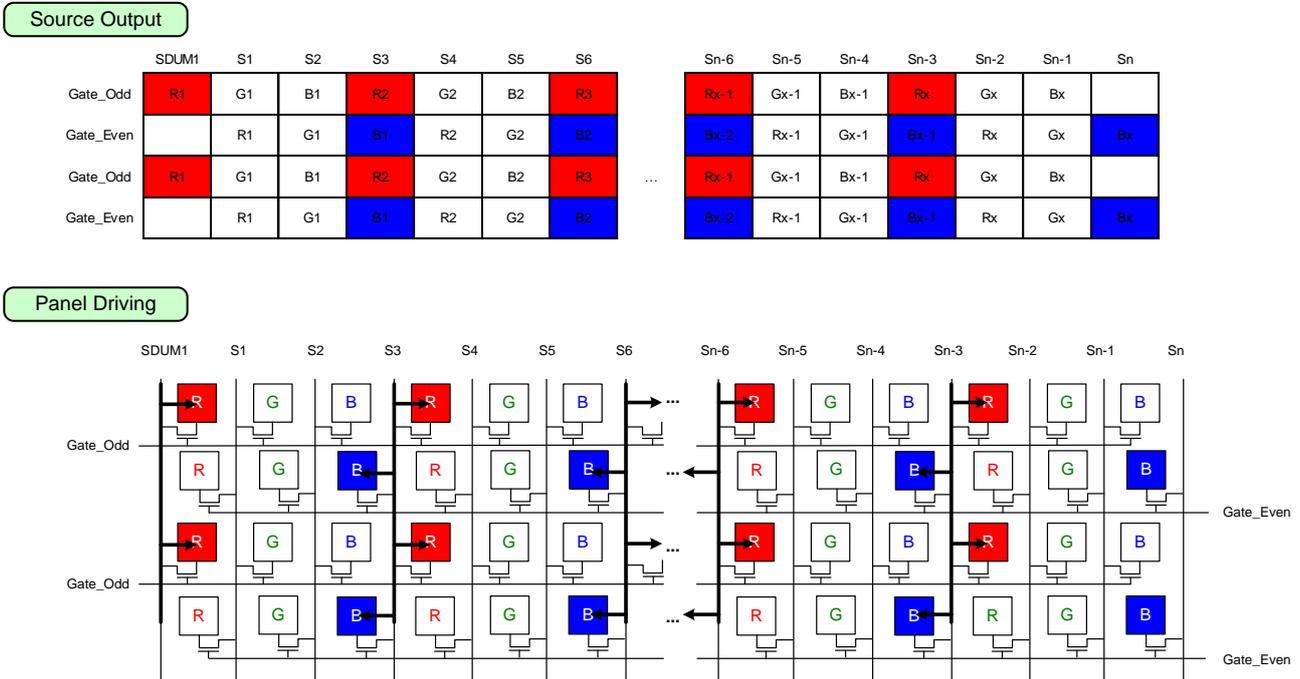
	SDUM1	S1	S2	S3	S4	S5
Gate_Odd	R1	G1	B1	R2	G2	B2
Gate_Even		R1	G1	B1	R2	G2
Gate_Odd	R1	G1	B1	R2	G2	B2
Gate_Even		R1	G1	B1	R2	G2
Gate_Odd	R1	G1	B1	R2	G2	B2
Gate_Even		R1	G1	B1	R2	G2

	Sn-5	Sn-4	Sn-3	Sn-2	Sn-1	Sn
Gx-1	Bx-1	Rx	Gx	Bx		
Rx-1	Gx-1	Bx-1	Rx	Gx	Bx	
Gx-1	Bx-1	Rx	Gx	Bx		
Rx-1	Gx-1	Bx-1	Rx	Gx	Bx	
Gx-1	Bx-1	Rx	Gx	Bx		
Rx-1	Gx-1	Bx-1	Rx	Gx	Bx	

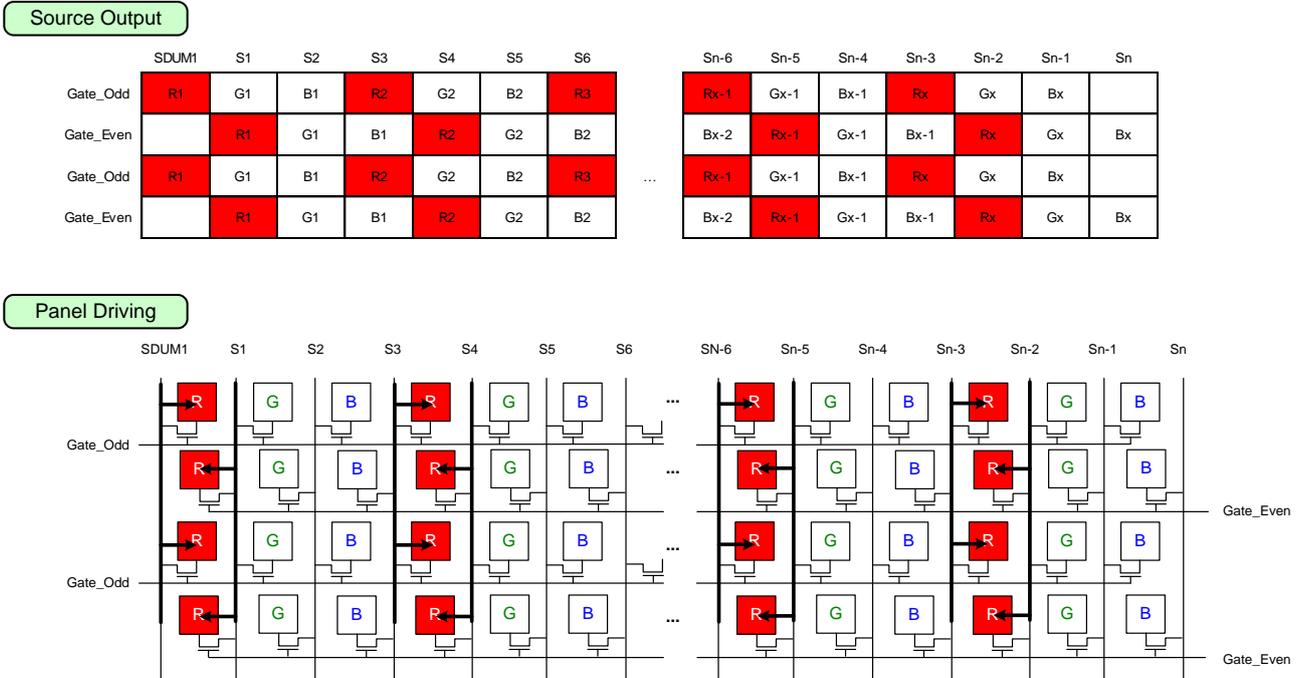
6.4. Zig-zag Inversion RED Data Display

The figure below illustrates the Zig-zag inversion panel driving method for Red data input.

When driving a Red pattern, the Red and Blue sub-pixels will light up line by line according to the data signal input.



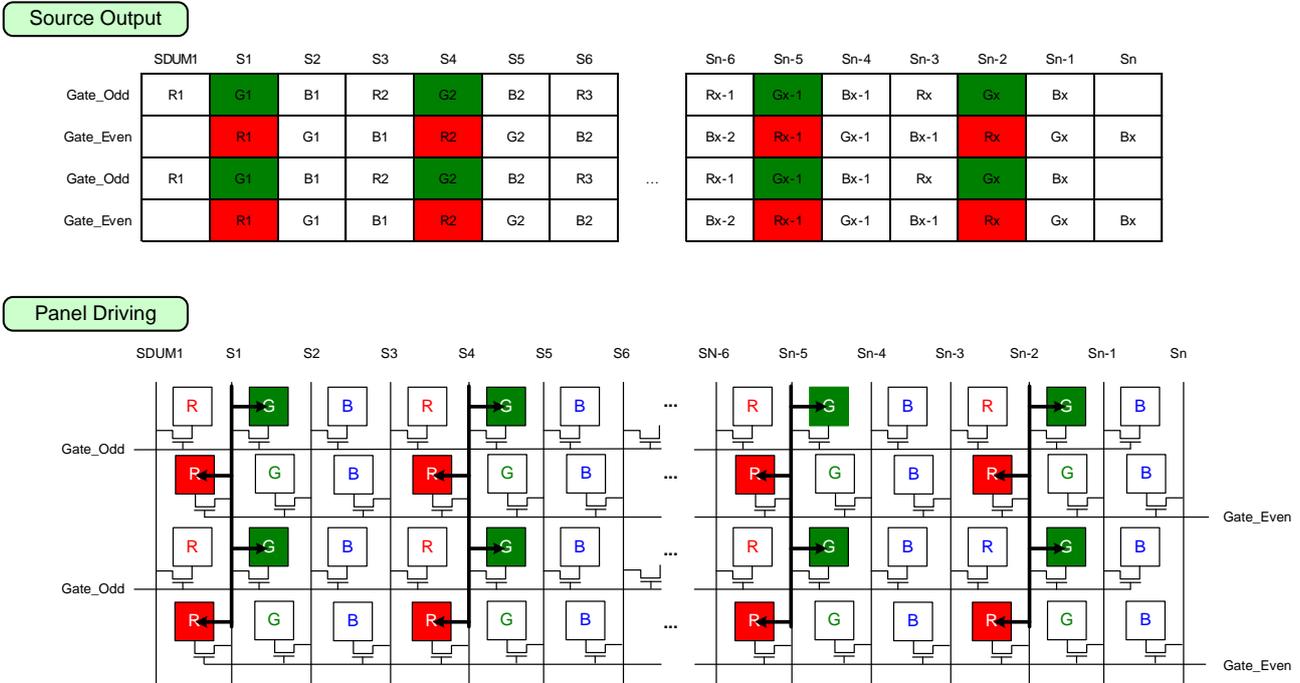
The figure below is the Zig-zag inversion panel driving method. The panel will be driven by the Red data input of the Gate_Odd and the Green data input of the Gate_Even.



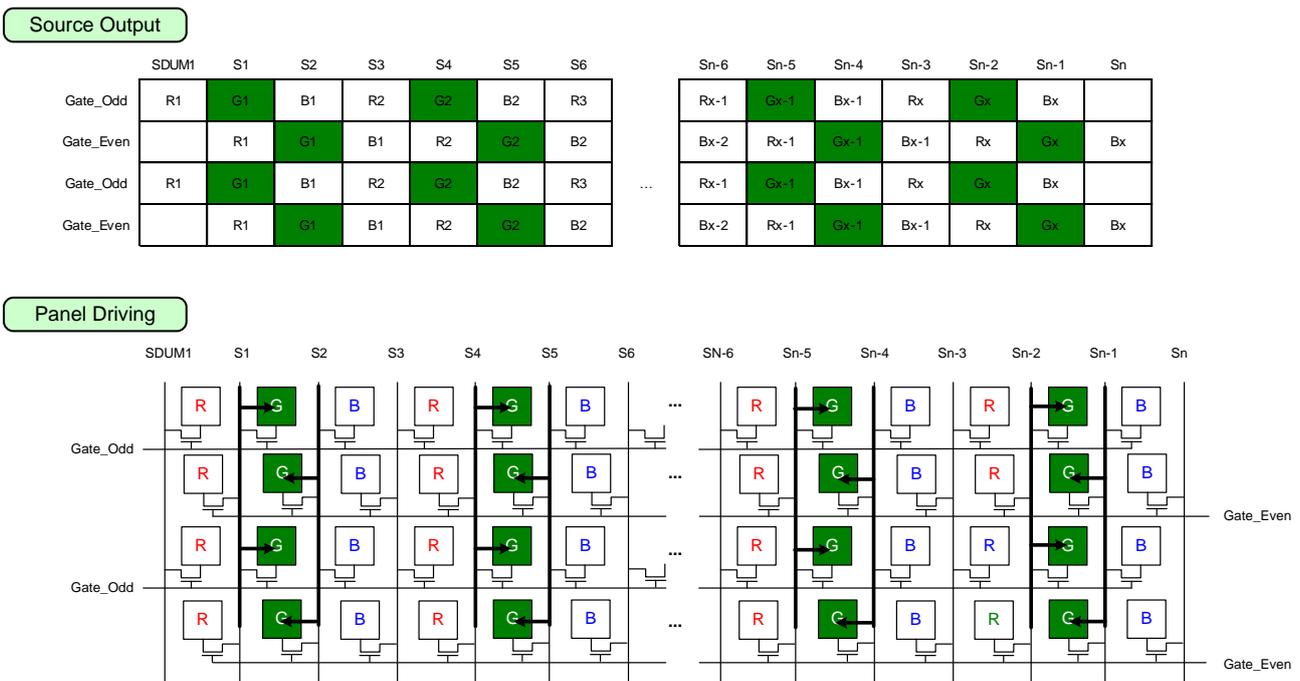
6.5. Zig-zag Inversion GREEN Data Display

The figure below illustrates the Zig-zag inversion panel driving method for Green data input.

When driving a Green pattern, the Green and Red sub-pixels will light up line by line according to the data signal input.



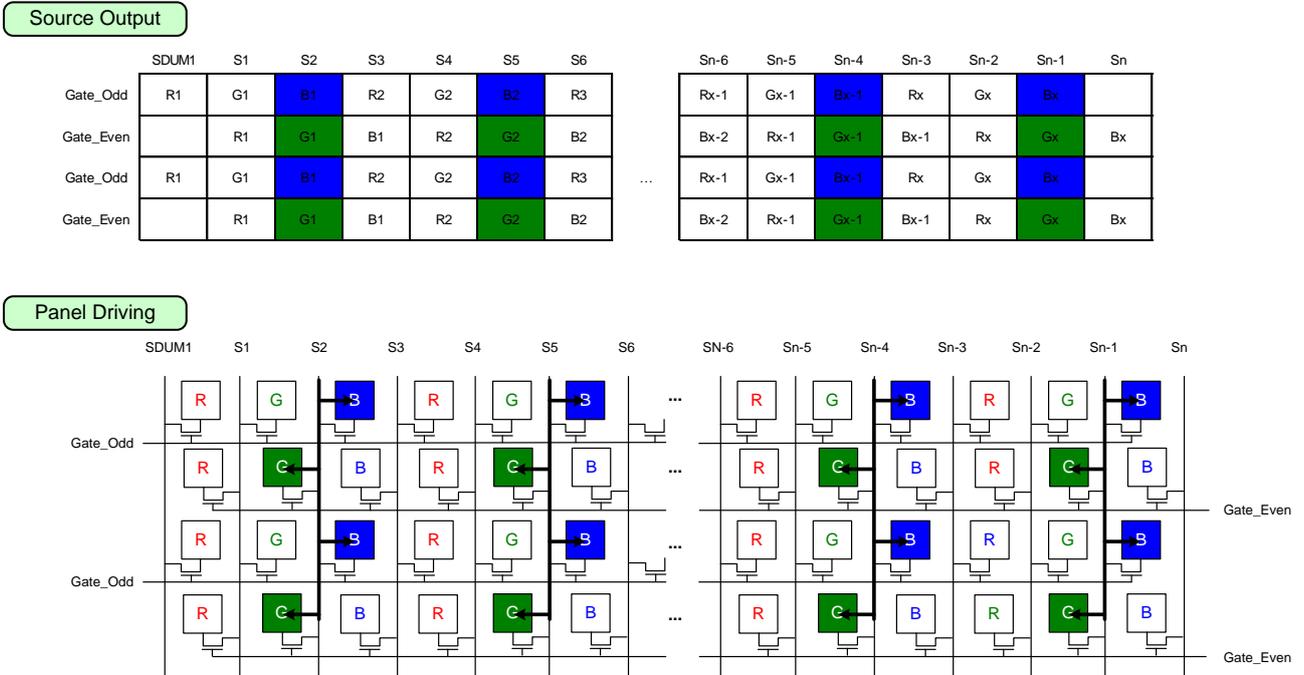
The figure below is the Zig-zag inversion panel driving method. The panel will be driven by the Green data input of the Gate_Odd and the Blue data input of the Gate_Even.



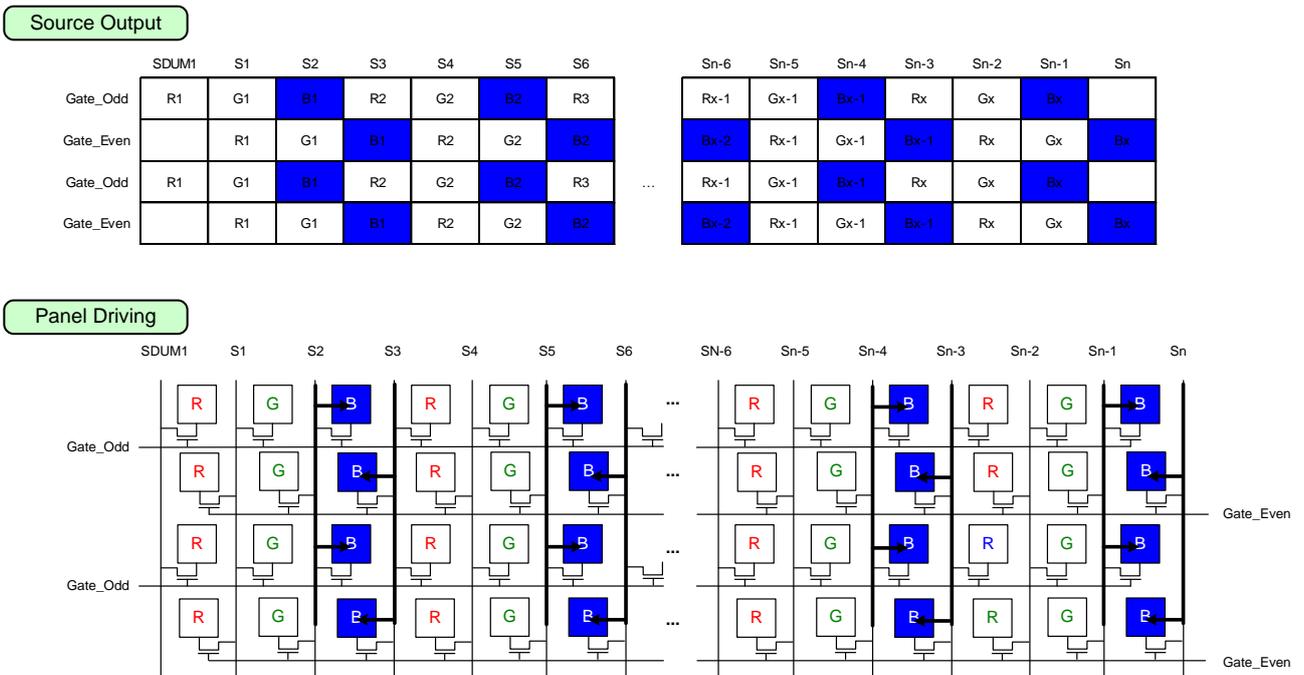
6.6. Zig-zag Inversion BLUE Data Display

The figure below illustrates the Zig-zag inversion panel driving method for Blue data input.

When driving a Blue pattern, the Blue and Green sub-pixels will light up line by line according to the data signal input.

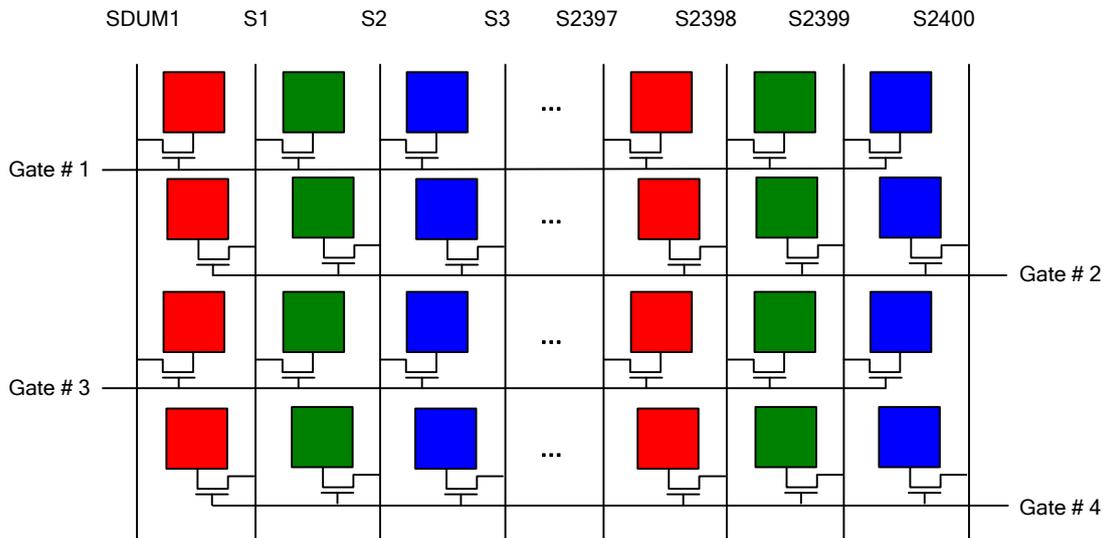


The figure below is the Zig-zag inversion panel driving method. The panel will be driven by the Blue data input of the Gate_Odd and the Red data input of the Gate_Even.

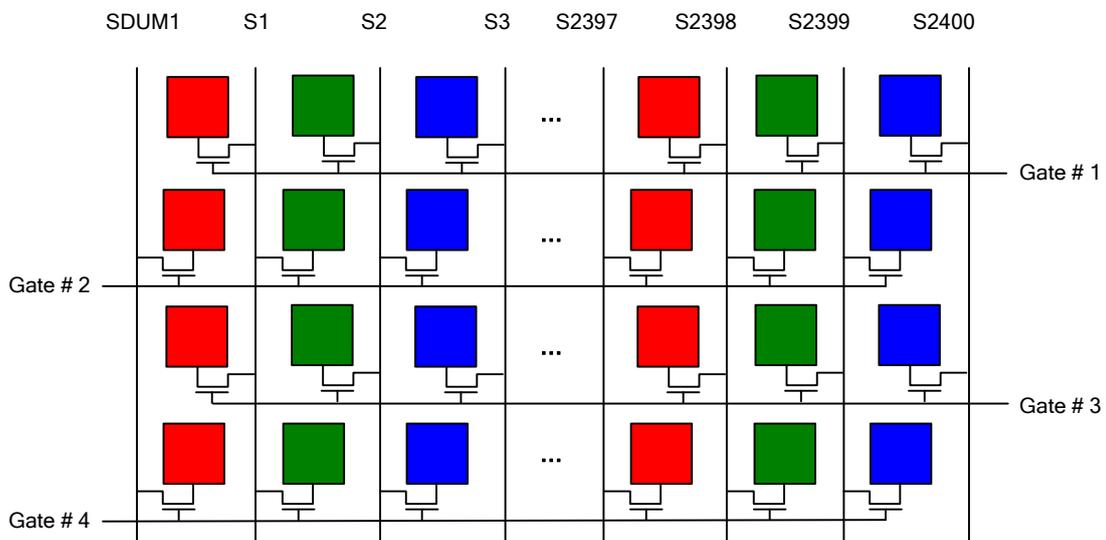


6.7. Different Zig-zag Type Panel

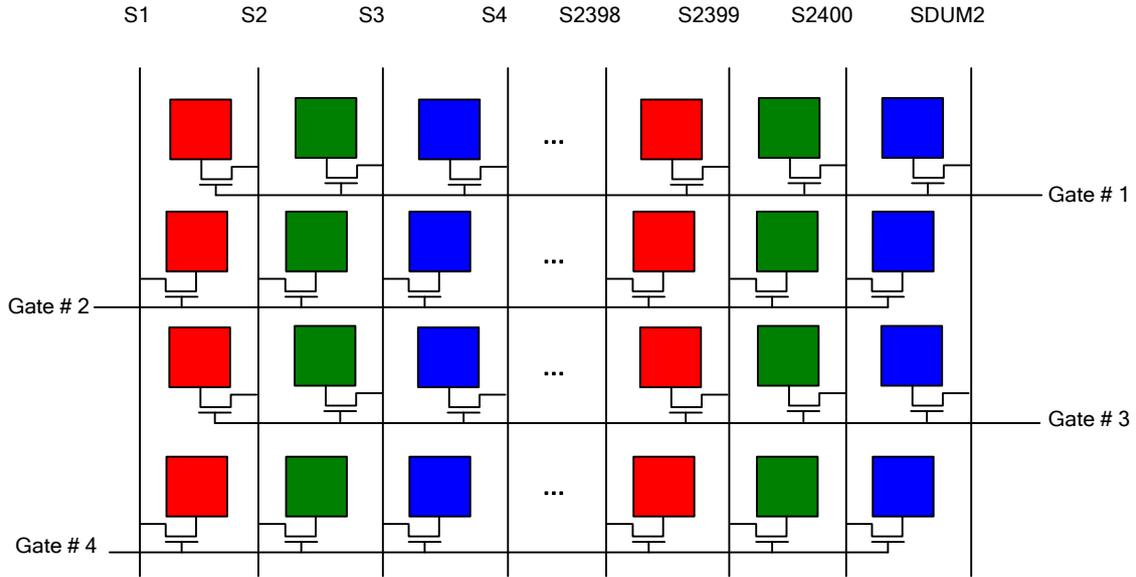
Zig-zag Type 1 (DINV[3:0] = 9h)



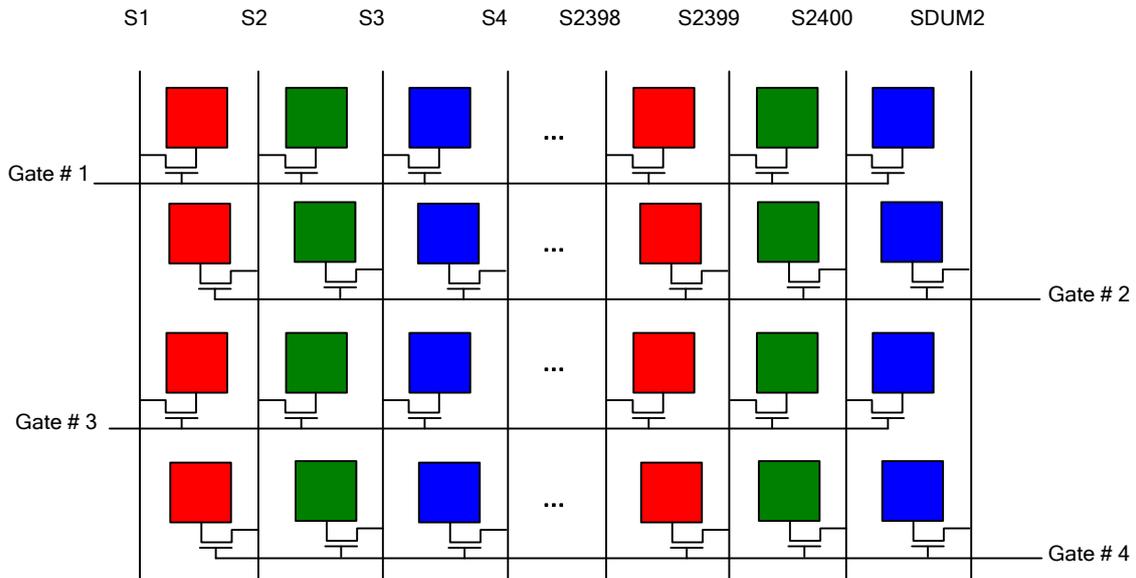
Zig-zag Type 2 (DINV[3:0] = Ah)



Zig-zag Type 3 (DINV[3:0] = Bh)



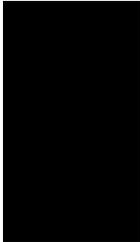
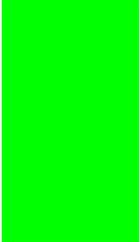
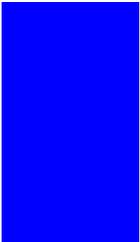
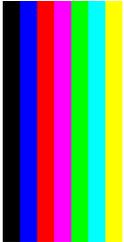
Zig-zag Type 4 (DINV[3:0] = Ch)



7. BIST Mode Function

7.1. BIST Mode Pattern

Table 33: BIST Mode Pattern

FRM_PT[0] White	FRM_PT[1]  Black	FRM_PT[2]  Red	FRM_PT[3]  Green
FRM_PT[4]  Blue	FRM_PT[5]  Gray128	FRM_PT[6]  Gray127	FRM_PT[7]  V-Color bar

8. Content Adaptive Brightness Control (CABC) Function

The CABC, a dynamic backlight control function, drastically reduces the power consumption of the luminance source. The ILI9881C-04 will refer the gray scale content of the display image to output in PWM waveform then to the LED driver for backlight brightness control. The content of gray scale can be increased while simultaneously lowering the brightness of the backlight to achieve the same perceived brightness. The adjusted gray level scale and the power consumption reduction depend on the content of the image.

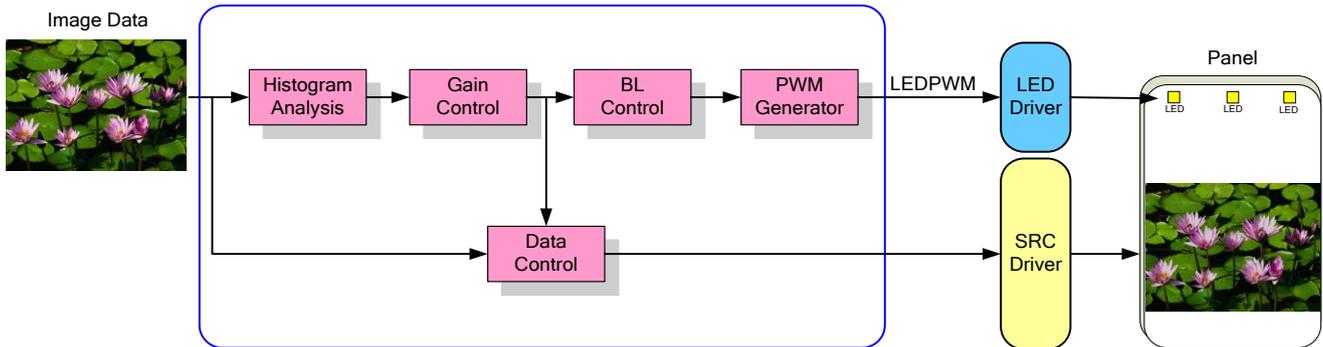


Figure 83: CABC Block Diagram

The ILI9881C-04 can calculate the backlight brightness level and send a PWM_OUT pulse to the LED driver via LEDPWM pin for backlight brightness control purposes. The PWM frequency can be adjusted by PWM_DIV parameters, and the calculating equation is shown below:

$$f_{LEDPWM} = \frac{32 \text{ MHz}}{(\text{PWM_DIV}[7:0] + 1) \times \text{PWM_DUTY_PRECISION}}$$

Figure 84 is the basic timing diagram which is applied from the ILI9881C-04 in order to control the LED driver.

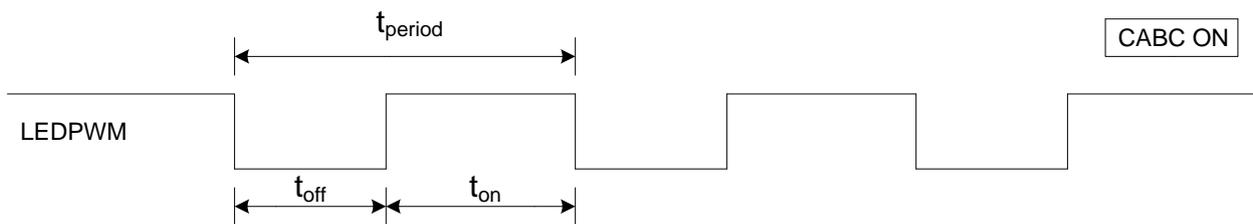


Figure 84: PWM OUT On/Off Period

9. Color Enhancement Function

9.1. Saturation Enhancement

The ILI9881C-04 provides the saturation enhancement to make the image content more vivid. The main concept in this feature is to enhance the color information on HSL domain, which includes the saturation information of each different color, show as Figure 85.

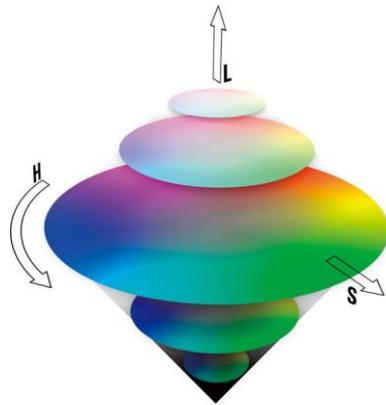


Figure 85: Saturation Enhancement : HSL model

In Figure 86, there is an example for saturation enhancement. Different enhancement levels being applied in this example.



Figure 86: Saturation Enhancement Image (a) Original, (b) Low Level, (c) Medium Level, (d) High Level.

9.2. Contrast Enhancement

The contrast between the dark and light, indicate the clarity of the image content. In this design, it provides contrast enhancement to increase the difference between dark and light to achieve the high contrast image. The user can select the enhancement level by setting command, the example shows below.

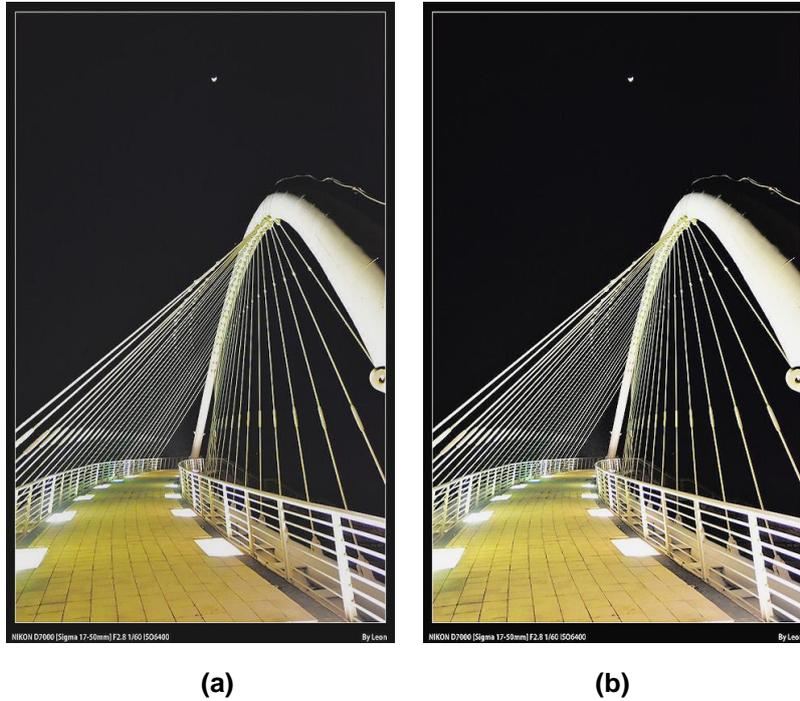


Figure 87: Contrast Enhancement Image (a) Original, (b) After enhancement

9.3. Sharpness Enhancement

Sharpness enhancement is provided to enhance the image visibility. Unlike contrast enhancement, sharpness enhancement is to strengthen the object's edge to make the object more clearly. The user can select the enhancement level by setting command, the example shows below.



Figure 88: Sharpness Enhancement Image (a) Original, (b) After enhancement

9.4. Sunlight Readability

The sunlight readability is in order to achieve high visibility in daylight or other bright light condition. Figure 89 shows the main concept of the influence of ambient light to the LCD displayer and the solution in the high ambient light condition. In this design, it changes the image content to achieve the high visibility in the ambient light condition as shows in Figure 89(b).

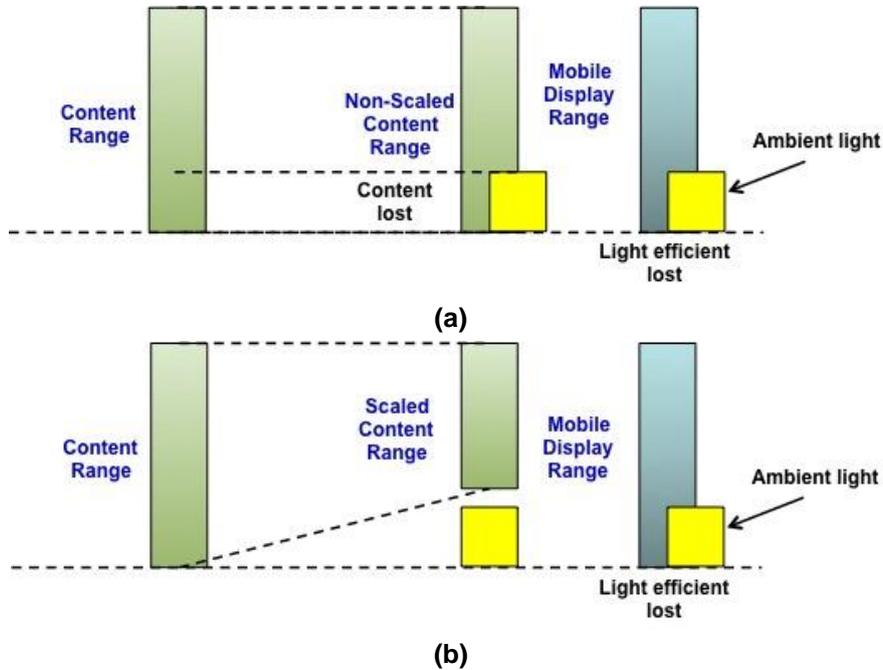


Figure 89: Sunlight Readability Concept (a) Backlight efficiency is consumed by ambient light, (b) Enhance the image content to avoid the influence.

10. Sleep Out Command and Self-Diagnostic Functions

10.1. Register Loading Detection

Sleep Out command (See Sleep Out (11h)) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EEPROM (or similar device) to registers of the display controller works properly.

The display controller will compare factory values of the EEPROM and register values of the display controller (1st step: compare register and EEPROM values; 2nd step: load EEPROM value to the register). If those two values (EEPROM and register values) are the same, a bit is inverted (= increased by 1), which is defined in command Read Display Self-Diagnostic Result (0Fh) (= RDDSDR) (The used bit of this command is D7). If those values are not the same, this bit (D7) is not inverted (= not increased by 1). The flow chart for this internal function is as follows:

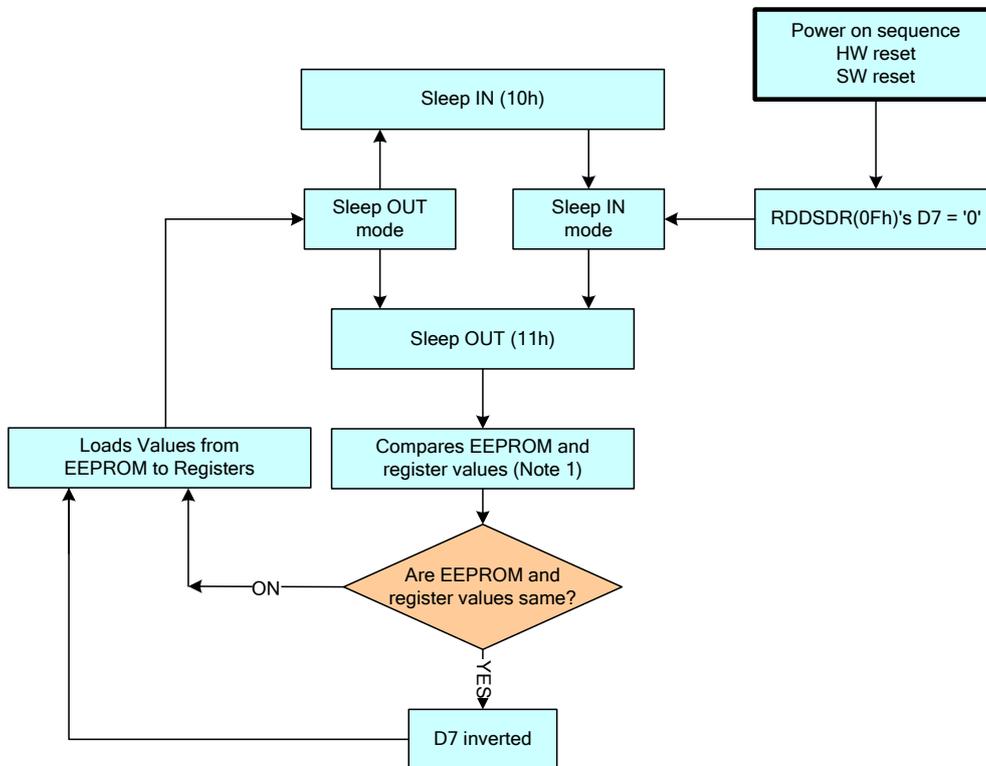


Figure 90: Register Loading Detection

Notes: If the EEPROM and loaded register values are not compared, then they can be changed by 00h to AFh and DAh to DDh commands.

10.2. Functionality Detection

The Sleep Out command (See Sleep Out (11h)) is a trigger for an internal function of the display module. It indicates if the display module is still running and meets functionality requirements. The internal function (the display controller) is compared to check if the display module still meets functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirements are met, a bit is inverted (= increased by 1), defined in the command Read Display Self-Diagnostic Result (0Fh) (RDDSDR) (The used bit of this command is D6). If functionality requirement is not the same, this bit (D6) is not inverted (= not increased by 1). The flow chart for this internal function is as follows:

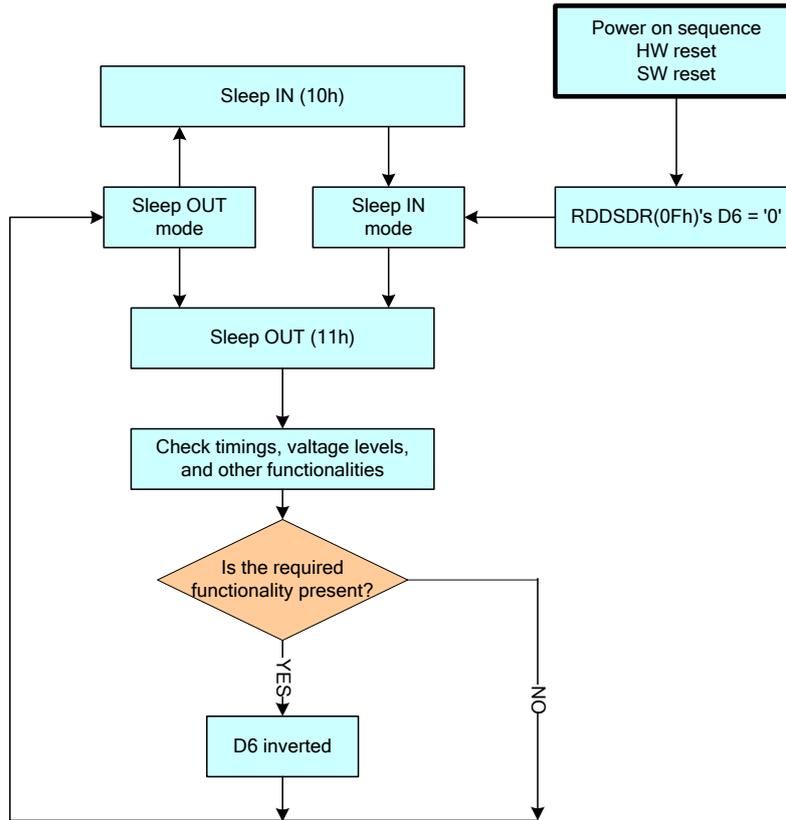


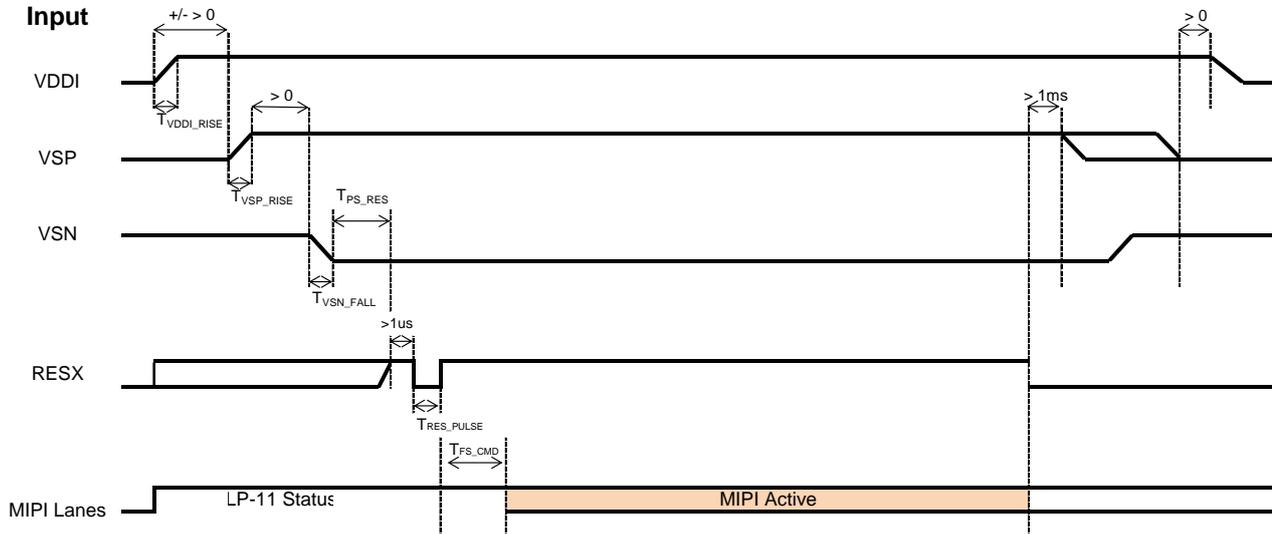
Figure 91: Functionality Detection

Notes: When changing from the Sleep In mode to Sleep Out mode, 120msec are needed after the Sleep Out command before it is able to check if functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there will be 5msec delay for the D6's value to be valid when the Sleep Out command is sent in the Sleep Out mode.

11. Power on/off Sequence

11.1. Power on/off sequence

11.1.1. Power Mode 2A

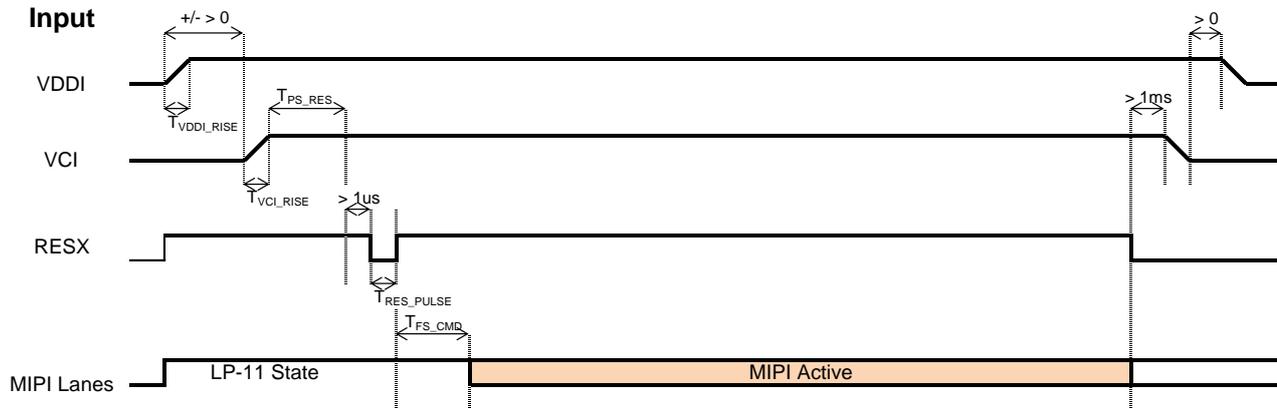


Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VSP_RISE}	VSP Rise time	130	-	-	us
T_{VSN_FALL}	VSN Fall time	200	-	-	us
T_{PS_RES}	VDDI/VSP on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

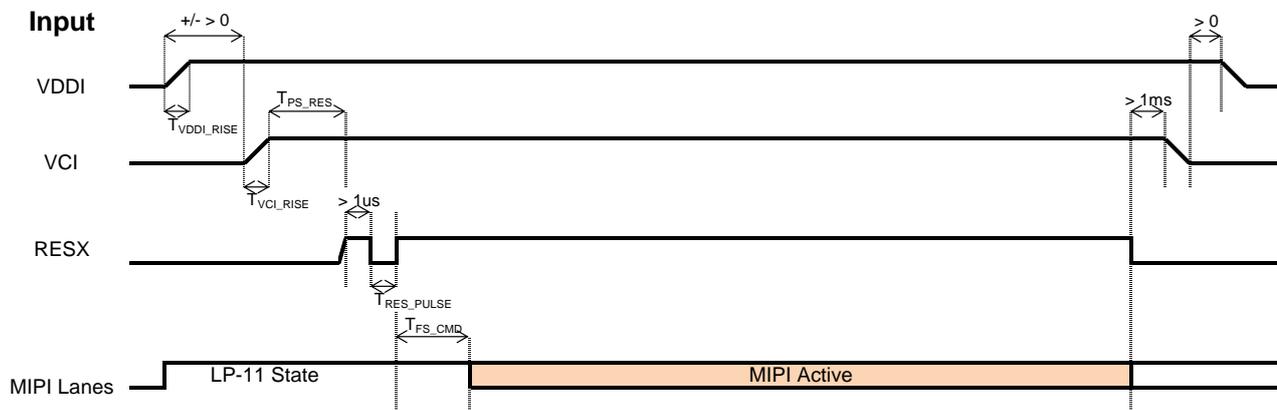
Figure 92: Power on/off sequence with Power Mode 2A

11.1.2. Power Mode 3

Case A:



Case B:

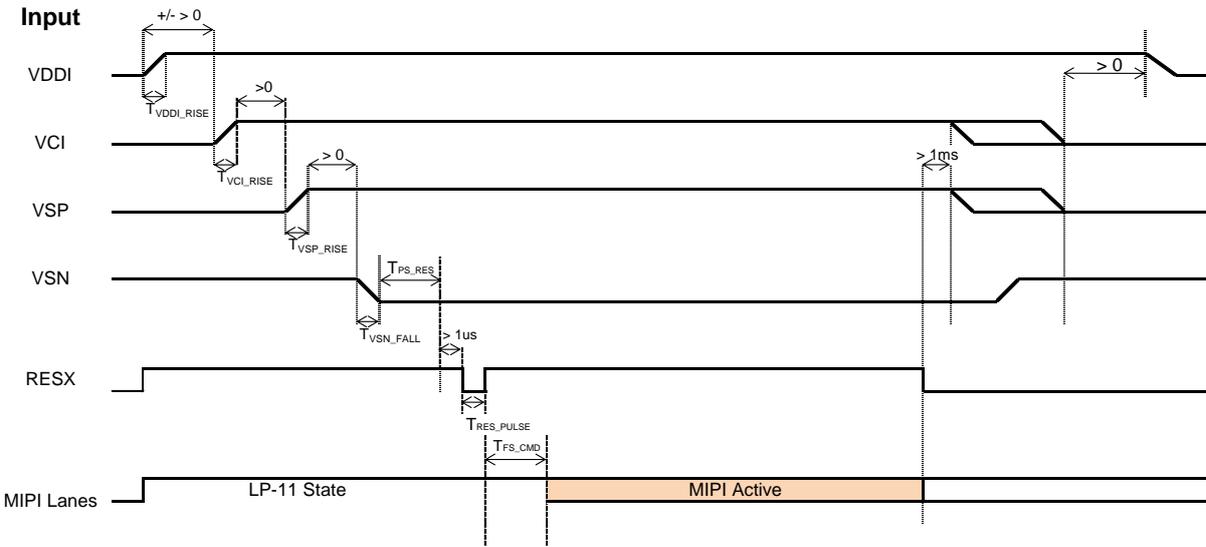


Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VCI_RISE}	Case A: VCI Rise time	130	-	-	us
	Case B: VCI Rise time	40	-	-	us
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

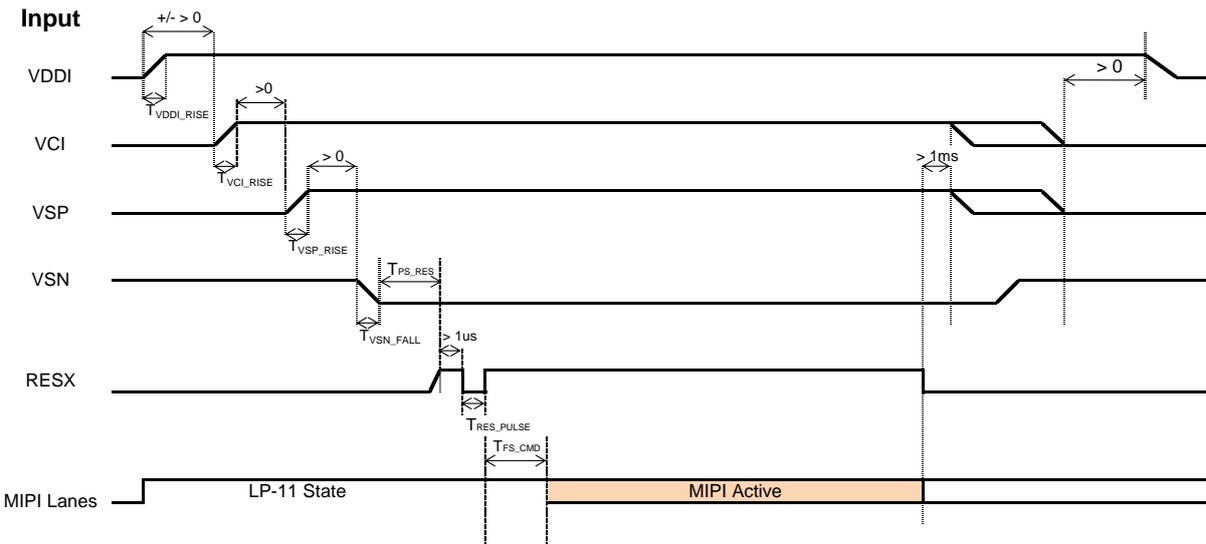
Figure 93: Power on/off sequence with Power Mode 3

11.1.3. Power Mode 4

Case A



Case B



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	10	-	-	us
T_{VCI_RISE}	Case A: VCI Rise time	130	-	-	us
	Case B: VCI Rise time	40	-	-	us
T_{VSP_RISE}	VSP Rise time	130	-	-	us
T_{VSN_FALL}	VSN Fall time	200	-	-	us
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

Figure 94: Power on/off sequence with Power Mode 4

11.2. Uncontrolled Power Off

The uncontrolled power off means a situation when a battery is removed without the controlled power off sequence. There will not be any damages for the display module, or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off event, the ILI9881C-04 will force the display to become blank and will not have any abnormal visible effects within 1 second on the display and remains blank until the Power On Sequence powers it up.

12. Power Level Definition

12.1. Power Levels

4 level modes are defined in order from Maximum to Minimum Power consumption:

1. Normal Mode On (full display), Sleep Out, Idle Mode Off.
In this mode, the display is able to show a maximum of 16.7M colors.
2. Normal Mode On (full display), Sleep Out, Idle Mode On.
In this mode, the display is able to show a maximum of 2 colors.
3. Sleep In Mode.
In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped.
4. Power Off Mode.
In this mode, all input powers are removed.

Transition between modes 1-3 is controllable by MCU commands. Mode 4 is entered only when both Power supplies are removed.

12.2. Power Flow Chart

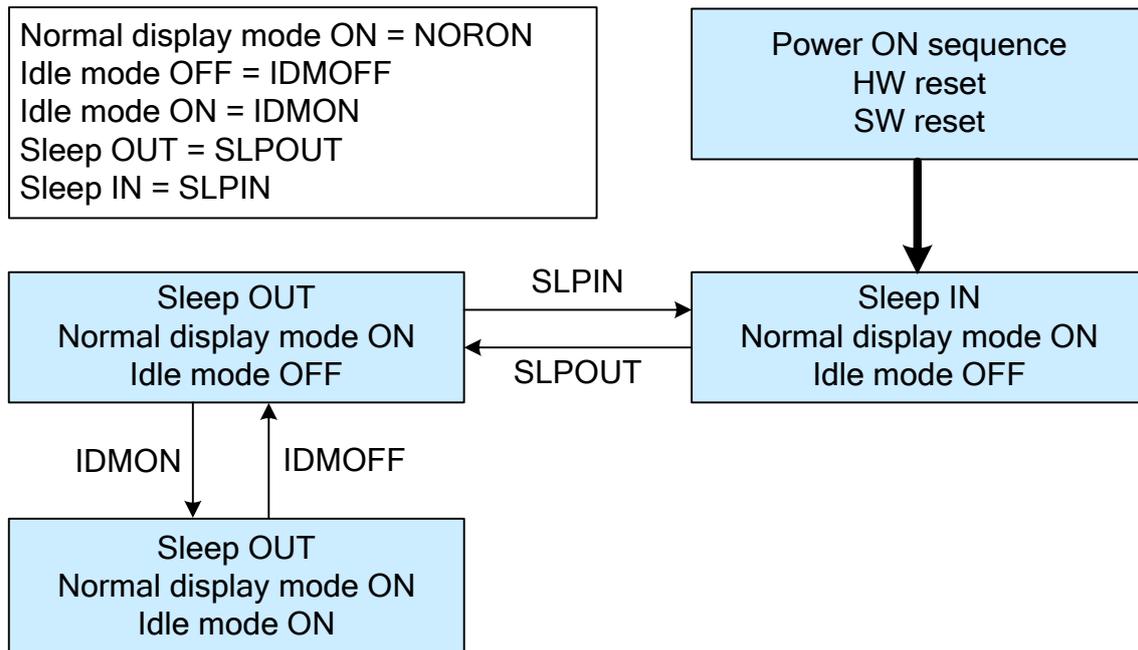


Figure 95: Power Mode Flow Chart

Notes:

1. There is not any abnormal visual effect when one power mode changes to another power mode.
2. There is not any limitation, which is not specified by User, when one power mode changes to another power mode.

13. Characteristics of I/O

13.1. Output or Bi-directional (I/O) Pins

Table 34: Characteristics of Output or Bi-directional (I/O) Pins

Pin/Line	After Power ON	After Hardware Reset	After Software Reset
D0P	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
D0N	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
VS	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
HS	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)
LEDPWM	Low	Low	Low
TE	Low	Low	Low

Note: There will be no output from D0P, D0N, VS, HS, LEDPWM and TE during Power ON/OFF sequence, hardware reset, and software reset.

13.2. Input Pins

Table 35: Input Pins

Pin/Line	During Power ON Process	After Power ON	After Hardware Reset	After Software Reset	During Power OFF Process
RESX	See chapter 11	Input valid	Input valid	Input valid	See chapter 11
IM[2:0]	Input invalid	Input valid	Input valid	Input valid	Input invalid
LANSEL	Input invalid	Input valid	Input valid	Input valid	Input invalid
RS[1:0]	Input invalid	Input valid	Input valid	Input valid	Input invalid
BOOSTM[2:0]	Input invalid	Input valid	Input valid	Input valid	Input invalid
CLKP	Input invalid	Input valid	Input valid	Input valid	Input invalid
CLKN	Input invalid	Input valid	Input valid	Input valid	Input invalid
D0P	Input invalid	Input valid	Input valid	Input valid	Input invalid
D0N	Input invalid	Input valid	Input valid	Input valid	Input invalid
D1P	Input invalid	Input valid	Input valid	Input valid	Input invalid
D1N	Input invalid	Input valid	Input valid	Input valid	Input invalid
D2P	Input invalid	Input valid	Input valid	Input valid	Input invalid
D2N	Input invalid	Input valid	Input valid	Input valid	Input invalid
D3P	Input invalid	Input valid	Input valid	Input valid	Input invalid
D3N	Input invalid	Input valid	Input valid	Input valid	Input invalid

14. NV Memory Programming Flow

14.1. External MTP_PWR 1-Byte Programming Flow

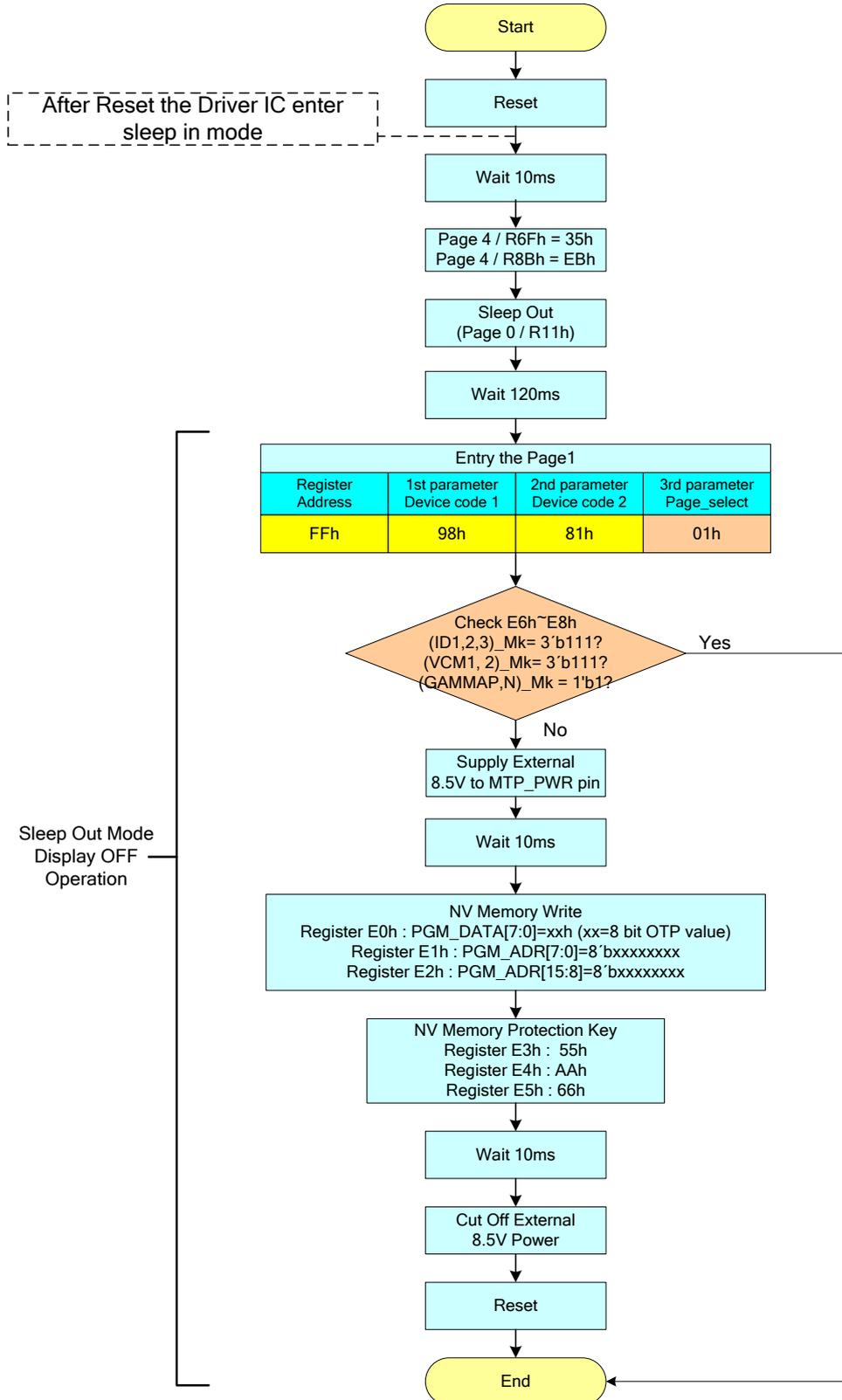
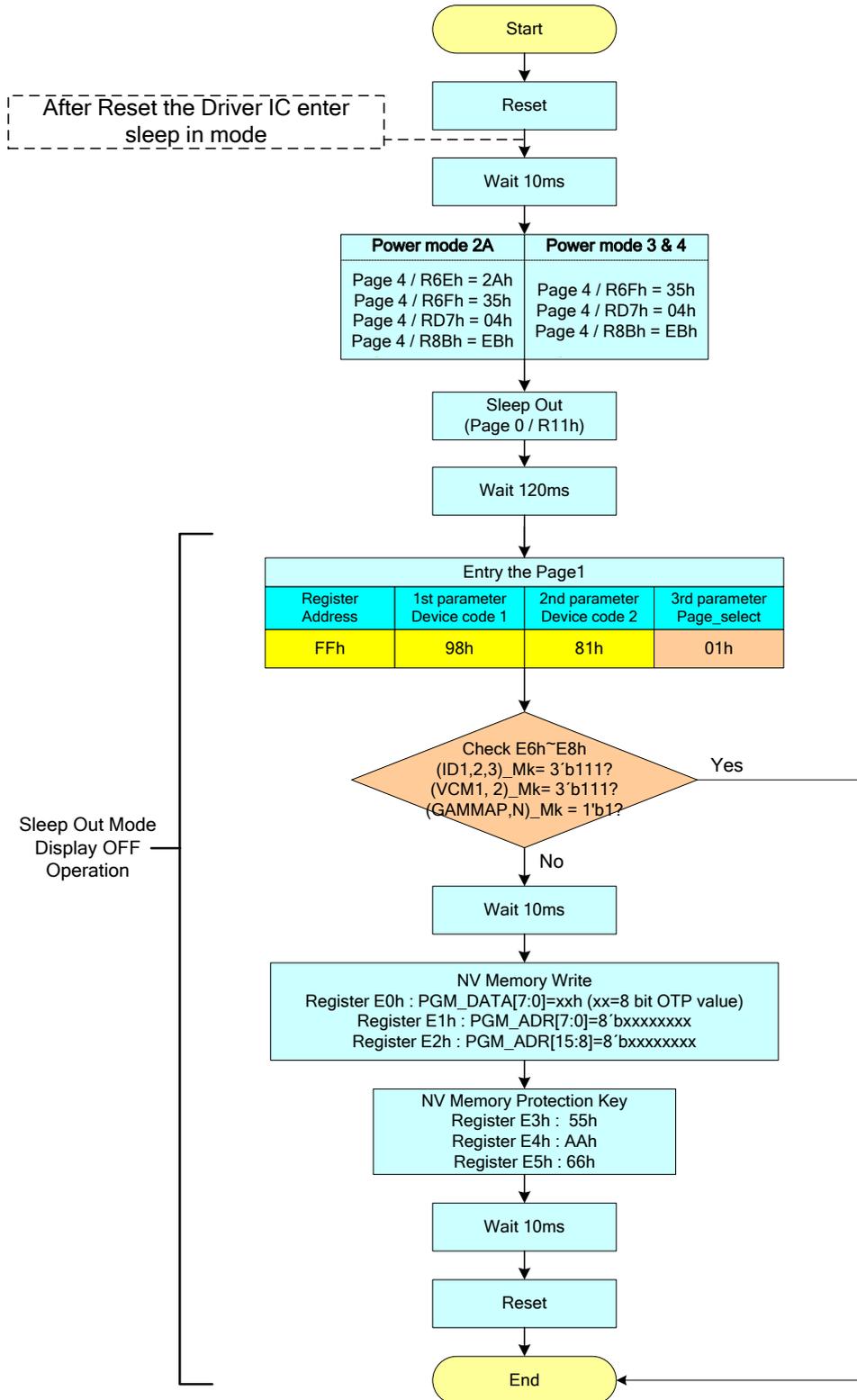


Figure 96: External MTP_PWR 1-Byte Programming Flow

14.2. Internal VGH 1-Byte Programming Flow



Note: Internal VGH Programming must operate in the Low Power mode.

Figure 97: Internal VGH 1-Byte Programming Flow

14.3. Group Programming Flow

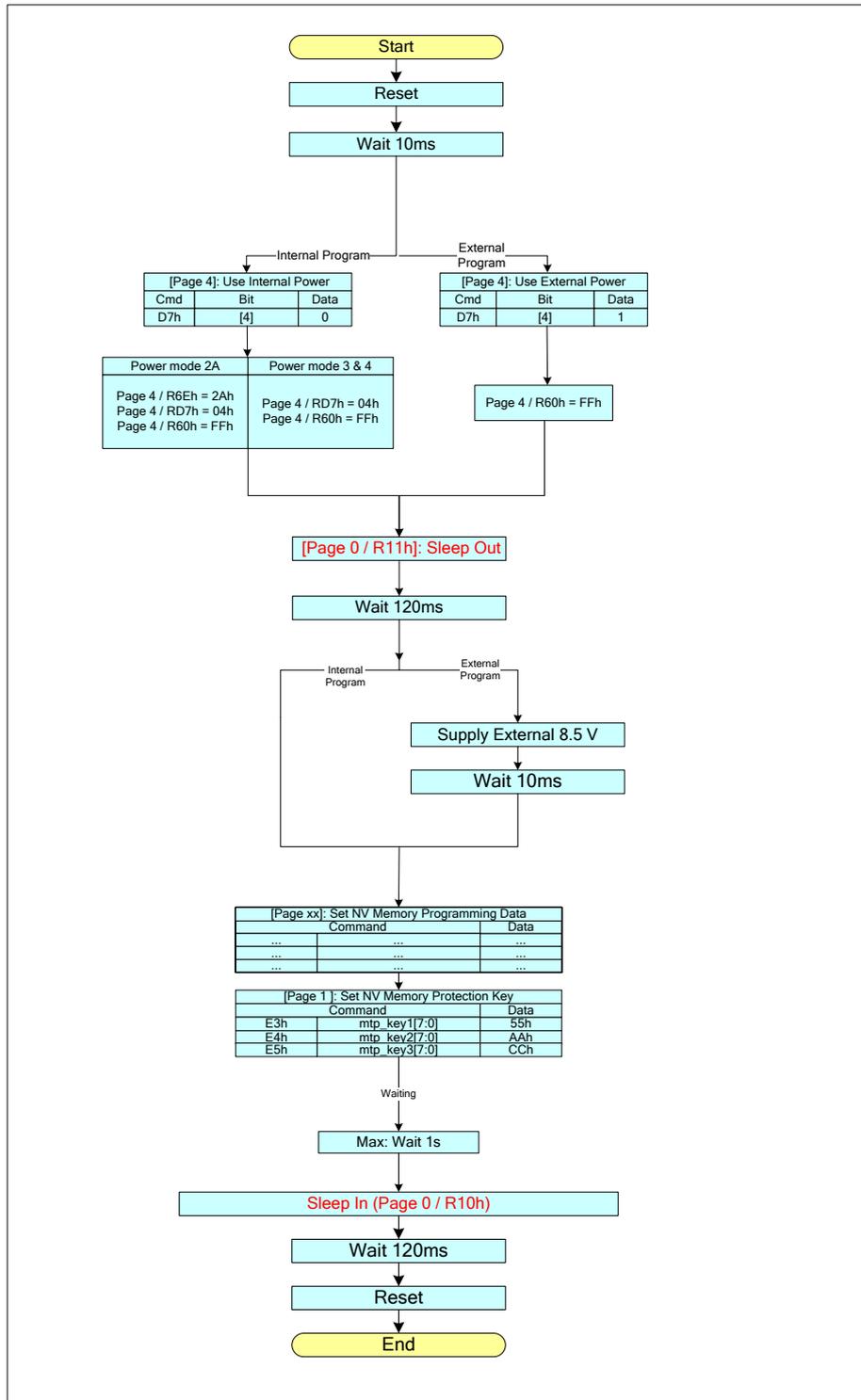


Figure 98: Group Programming Flow

*Note : If 1-byte program , VCOM OTP program address is register pg1_cmd_52h~55h,
If auto program, VCOM OTP program address is register pg4_cmd_C4h~C7h*

15. Gamma Correction

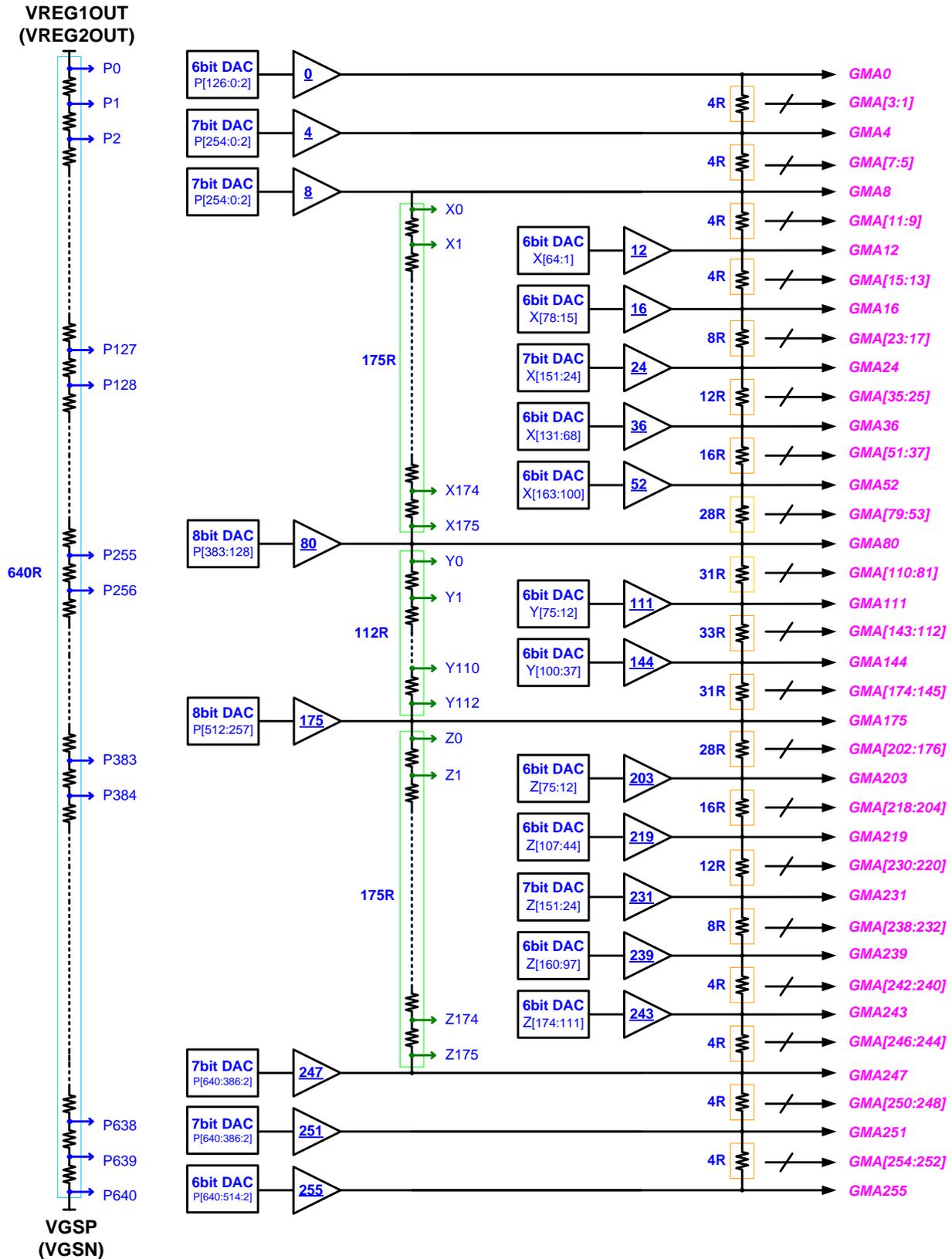


Figure 99: Gamma Architecture

16. Touch Synchronization Signal

The VS and HS pad of ILI9881C-04 can output the synchronization signals to touch sensing signal for touch panel controller. To use these signals, touch panel controller can receive touch sensing signal while avoiding display changing noise.

These signals are consist of vertical synchronization signal: VSOUT and horizontal synchronization signal: HSOUT. The level of output voltage is VDDI to GND. Each signal can adjust output timing for internal synchronization signal. The high level width of VSOUT is 1 line, and it is adjustable. VSOUT is outputted always, but HSOUT is outputted during displaying only.

(1) VSOUT output Timing

VSOUT output means internal VSYNC is starting point. VSOUT output timing can be adjusted by VSOD register. Unit is 1H.

(2) HSOUT output Timing

HSOUT output means internal source output timing is starting point. HSOUT output timing can be adjusted by HSOD register. And HSOUT high level width can be adjusted by HSOHW register.

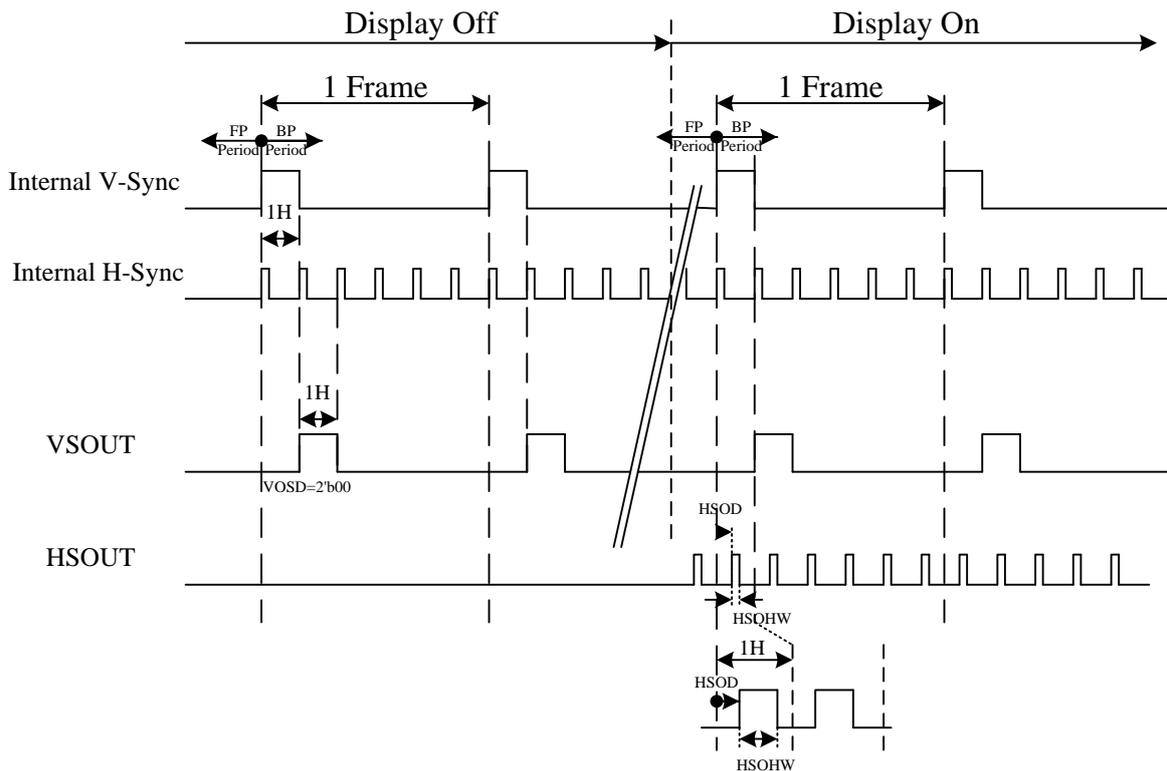


Figure 100: Touch Synchronization Signal

17. Electrical Characteristics

17.1. Absolute Maximum Ratings

The absolute maximum rating is listed in Table 36. When the ILI9881C-04 is used out of the absolute maximum ratings, it may be permanently damaged. To use the ILI9881C-04 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the ILI9881C-04 will malfunction and cause poor reliability.

Table 36: Absolute Maximum Ratings

Item	Symbol	Unit	Value
Analog Operating Voltage	VCI ~ GND	V	-0.3 ~ +7.0
Analog Operating Voltage	VCIREF ~ GND	V	-0.3 ~ +7.0
Digital Operating Voltage	VDDI ~ GND	V	-0.3 ~ +3.8
Digital Operating Voltage	VCC1 ~ GND	V	-0.3 ~ +7.0
Digital Operating Voltage	VCC2 ~ GND	V	-0.3 ~ +7.0
DSI Operating Voltage	VDDAM ~ GND	V	-0.3 ~ +3.8
OTP Supply Voltage	MTP_PWR ~ GND	V	-0.3 ~ +9.0
Supply Voltage	VSP ~ GND	V	-0.3 ~ +7.0
Supply Voltage	VSN ~ GND	V	0.3 ~ -7.0
Gate Driver High Voltage	VGH ~ GND	V	-0.3 ~ +18
Gate Driver Low Voltage	VGL ~ GND	V	0.3 ~ -18
Driver Supply Voltage	VDDI - VCL	V	≤ 6.6V
Driver Supply Voltage	VGH - VGL	V	≤ 32.0V
Input Voltage	VIN	V	-0.3 ~ VDDI + 0.3
HS Input Voltage	VHSIN	V	-0.3 ~ + 1.65
Operating Temperature	Topr	°C	-30 ~ +70
Storage Temperature	Tstg	°C	-55 ~ +110

Note: Even if the absolute maximum rating of one of the above parameters is exceeded only for a short while, the quality of the product may be degraded. Therefore, be sure to use the product within the range of the absolute maximum ratings.

17.2. DC Characteristics for Panel Driving

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power & Operation Voltage							
Analog operating voltage	VCI	-	2.5	2.8	6.6	V	
Analog operating voltage	VCIREF		2.5	2.8	6.6	V	
Digital operating voltage	VDDI	-	1.65	2.8	3.6	V	
Digital operating voltage	VCC1		1.65	2.8	6.6	V	
Digital operating voltage	VCC2		1.65	2.8	6.6	V	
DSI operating voltage	VDDAM	-	1.65	1.8	3.6	V	
OTP Supply voltage	MTP_PWR	-	8.4	8.5	8.6	V	
Analog operating voltage	VSP	-	4.5		6.6	V	
Analog operating voltage	VSN	-	-6.6		-4.5	V	
Logic High level input voltage	VIH	-	0.7*VDDI		VDDI	V	Note1
Logic Low level input voltage	VIL	-	-0.3		0.3*VDDI	V	Note1
Logic High level output voltage TE , LEDPWM	VOH	IOH = -1.0mA	0.8*VDDI		VDDI	V	Note1
Logic Low level output voltage TE , LEDPWM	VOL	IOL = +1.0mA	0		0.2*VDDI	V	Note1
Gate Driver High Voltage	VGH	-	8.0	-	18	V	
Gate Driver Low Voltage	VGL	-	-18.0	-	-7.0	V	
Driver Supply Voltage	-	VGH-VGL	15	-	32	V	
VCOM Operation							
DC VCOM Amplitude Voltage	VCOM	-	-4.0	-	0	V	Note3
Source Driver							
Source Output Range	VSOUT(+)	-	0.3	-	VREG1OUT-0.1	V	Note4
	VSOUT(-)	-	VREG2OUT +0.1	-	-0.3	V	Note4
Positive Gamma Reference Voltage	VREG1OUT	-	3.5	-	VSP-0.5 (VSP<=6.1) 5.6 (VSP>6.1)	V	
Negative Gamma Reference Voltage	VREG2OUT	-	VSN+0.5 (VSN>=-6.1) -5.6 (VSN<-6.1)	-	-3.5	V	
Source Output Setting Time	Tr	Below with 99% precision	-	10	-	uS	Note3.4
Output Deviation Voltage (Source Output channel)	Vdev	Sout>=4.2V Sout<=0.8V	-	-	20	mV	Note3
		4.2V>Sout>0.8V	-	-	15	mV	
Output Offset Voltage	VOFFSET	-	-	-	35	mV	Note3
Standby mode current consumption							
Sleep In mode	I(VDDI SLP IN)	Ta = 25 °C VCI=2.8V VDDI=1.8V	-	35	-	uA	
	I(VCI SLP IN)		-	25	-	uA	

Notes:

1. Ta = -30 to 70 °C (to 85 °C no damage) , VCI = 2.5V to 6.6V, VDDI = 1.65V to 3.6V
2. Supply digital VDDI voltage equal or less than analog VCI voltage.
3. Source channel loading = 9KΩ, 70pF/channel
4. The maximum value is between with Note 3 and Gamma setting value

17.3. DSI DC Characteristics

The DSI uses different state codes which depend on DC voltage levels of the clock and data lanes. The meaning of the state codes is defined in the following table.

State Code	Line DC Voltage Levels	
	CLOCK_P or DATA_P	CLOCK_N or DATA_N
HS-0	Low (HS)	High (HS)
HS-1	High (HS)	Low (HS)
LP-00	Low (LP)	Low (LP)
LP-01	Low (LP)	High (LP)
LP-10	High (LP)	Low (LP)
LP-11	High (LP)	High (LP)

Note: $T_a = -30^{\circ}\text{C}$ to 70°C (to $+85^{\circ}\text{C}$ no damage)

17.3.1. DC Characteristics for DSI LP Mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined in the table below: DC Characteristics for the DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned in the condition column. Other logical levels in the table are for MCU interface.

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Logic 1 input voltage	V_{IHLPD}	LP-CD	450	-	1350	mV
Logic 0 input voltage	V_{ILLPCD}	LP-CD	0.0	-	200	mV
Logic 1 input voltage	V_{IHLPRX}	LP-RX (CLK, D0, D1, D2, D3)	880	-	1350	mV
Logic 0 input voltage	V_{ILLPRX}	LP-RX (CLK, D0, D1, D2, D3)	0.0	-	550	mV
Logic 0 input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0.0	-	300	mV
Logic 1 output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic 0 output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic 1 input current	I_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic 0 input current	I_{IL}	LP-CD, LP-RX	-10	-	-	uA

Notes:

- $T_a = -30^{\circ}\text{C}$ to 70°C (to $+85^{\circ}\text{C}$ no damage)
- DSI High Speed mode is off.

17.3.2. Spike/Glitch Rejection

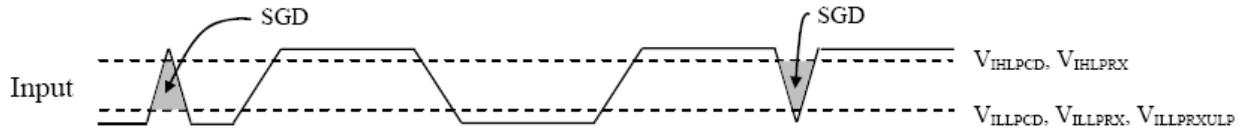


Figure 101: Spike/Glitch Rejection

Notes:

1. A spike/glitch can be rejected when the Peak Interference Amplitude is 200mV (at maximum) and Interference Frequency is 450MHz (at the very least).
2. $n = 0, 1, 2$ and 3.

Table 37: Spike/Glitch Rejection

Spike/Glitch Rejection – DSI					
Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N, DnP/N	SGD	Input pulse rejection for DSI	-	300	Vps

17.3.3. DC Characteristics for DSI HS mode

Parameter	Symbol	Condition	Specification			Unit
Input Common Mode Voltage for Clock	V_{CMCLK}	CLKP/N Note 2, Note 3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DnP/N Note 2, Note 3, Note 5	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	CLKP/N Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DnP/N Note 4, Note 5	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	CLKP/N	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DnP/N Note 5	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	CLKP/N	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DnP/N Note 5	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	CLKP/N	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DnP/N Note 5	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	CLKP/N, DnP/N Note 3, Note 5	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	CLKP/N, DnP/N Note 3, Note 5	-	-	460	mV
Differential Termination Resistor	R_{TERM}	CLKP/N, DnP/N Note 5	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	CLKP/N, DnP/N Note 5	-	-	450	mV
Termination Capacitor	C_{TERM}	CLKP/N, DnP/N Note 5, Note 6	-	-	60	pF

Notes:

1. $T_a = -30^{\circ}C$ to $70^{\circ}C$ (to $+85^{\circ}C$ no damage), $V_{CI} = 2.5V$ to $6.6V$, $V_{DDI} = 1.65V$ to $3.6V$
2. Includes $50mV$ ($-50mV$ to $50mV$) ground difference
3. Without $V_{CMRCLKM450}/V_{CMRDATAM450}$
4. Without $50mV$ ($-50mV$ to $50mV$) ground difference
5. $n = 0$ and 1
6. For higher bit rates, a $14pF$ capacitor will be needed to meet the common-mode return loss specification.

The DSI receiver (HS mode) understands that there is logical 1 (= HS-1) when a differential voltage is more than V_{THH} (CLKP/DnP). The DSI receiver (HS mode) understands that there is logical 0 (= HS-0) when a differential voltage is more than V_{THL} (CLKN/DnN). There is undefined state if the differential voltage is less than V_{THH} (CLKP/DnP) and less than V_{THL} (CLKN/DnN). A reference figure is below.

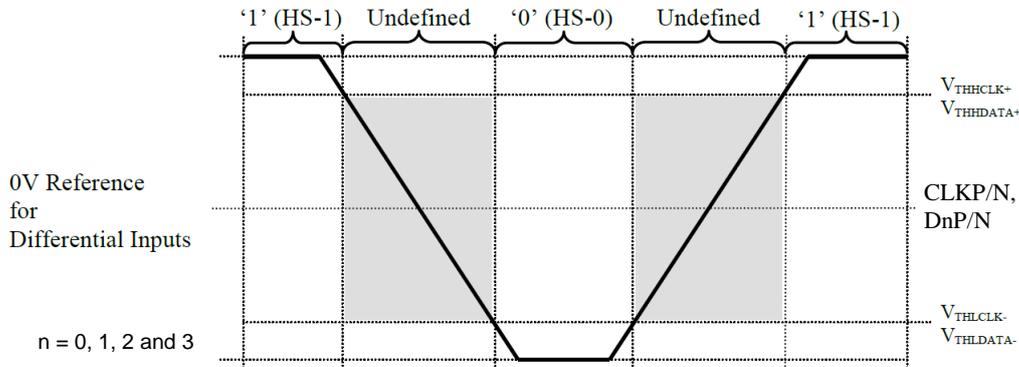
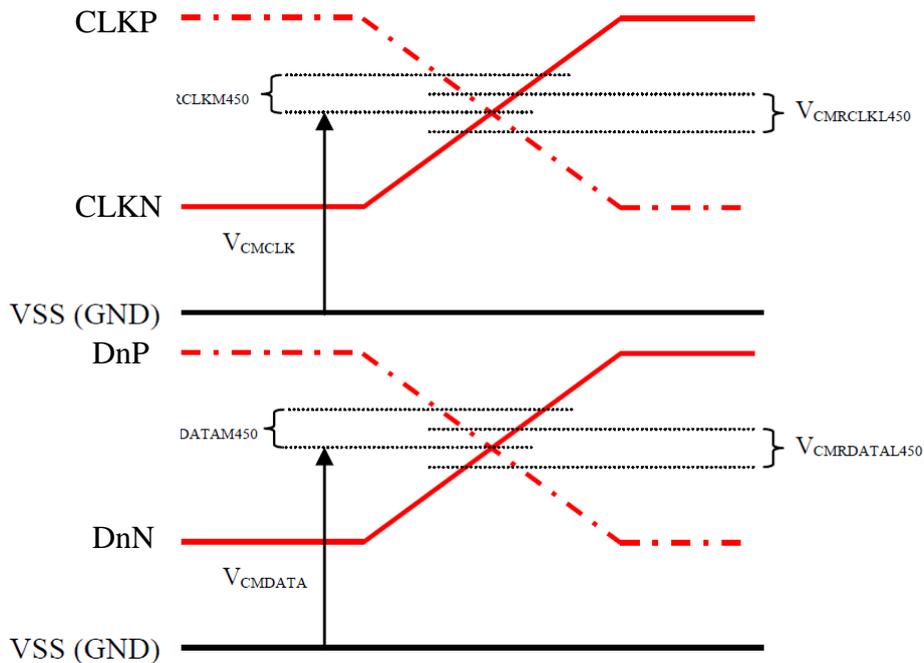


Figure 102: Differential Inputs Logical 0 and 1, Threshold High/Low, Differential Voltage Range



Note: $n = 0, 1, 2$ and 3

Figure 103: Common Mode Voltage on Clock and Data Channels

The termination resistor (R_{TERM}) of the differential DSI receiver can be driven to two different states by the receiver:

- ❖ Low Power (LP) mode when the termination resistor is not connected between differential inputs (CLKP <=> CLKN or D0P <=> D0N or D1P <=> D1N or D2P <=> D2N or D3P <=> D3N)
- ❖ High Speed (HS) mode when the termination resistor is connected between differential inputs (CLKP <=> CLKN or D0P <=> D0N or D1P <=> D1N or D2P <=> D2N or D3P <=> D3N)

The termination switch (HS/LP), when the termination resistor is not connected, is illustrated below.

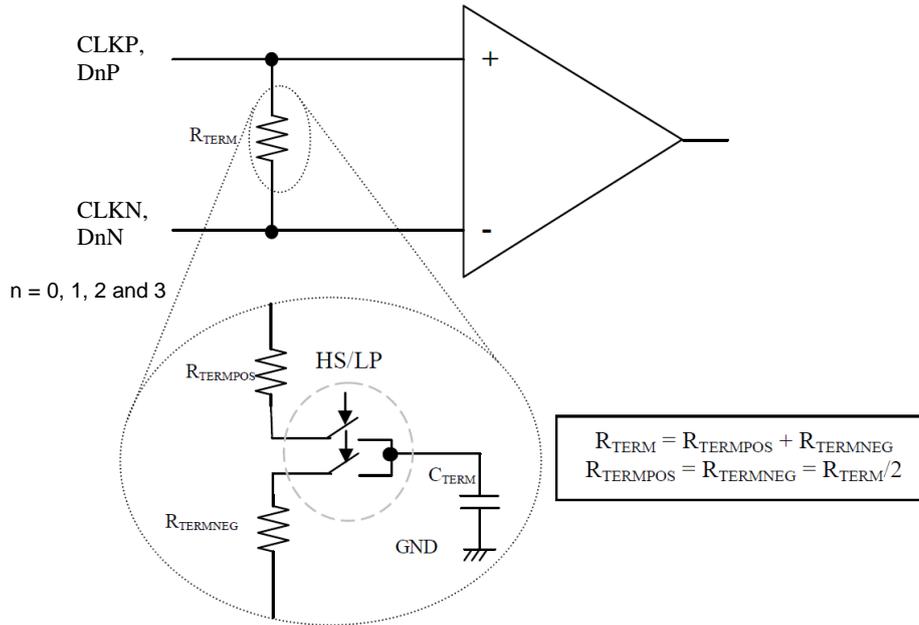


Figure 104: Differential Pair Termination Resistor on the Receiver Side

17.4. AC Characteristics

17.4.1. DSI Timing Characteristics

17.4.2. High Speed Mode – Clock Channel Timing

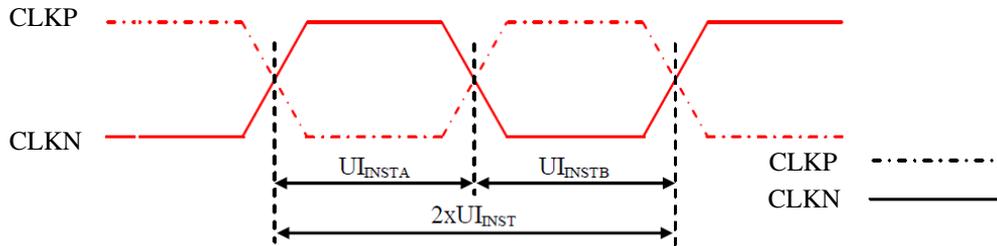


Figure 105: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xU_{INST}$	Double UI instantaneous	Note 2	25	ns
CLKP/N	U_{INSTA}, U_{INSTB} (Note 1)	UI instantaneous Half	Note 2	12.5	ns

Notes:

1. $UI = U_{INSTA} = U_{INSTB}$
2. Define the minimum value, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	750 Mbps	650 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	750 Mbps	650 Mbps

17.4.3. High Speed Mode – Data Clock Channel Timing

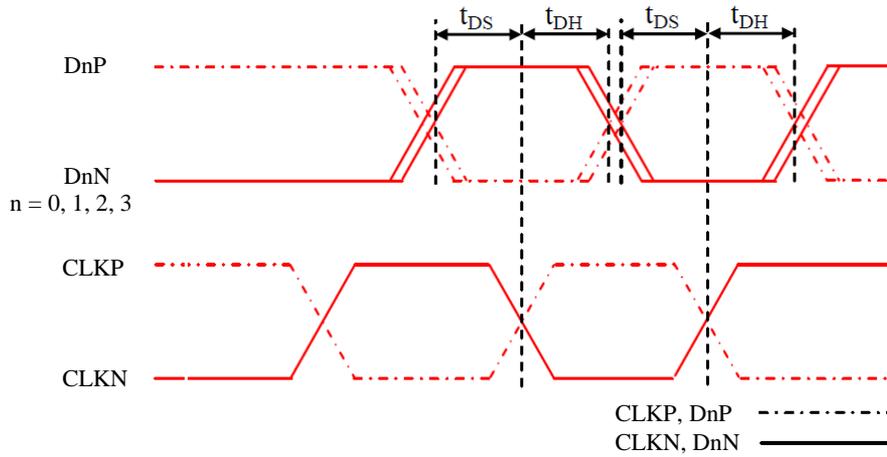


Figure 106: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

17.4.4. High Speed Mode – Rising and Falling Timings

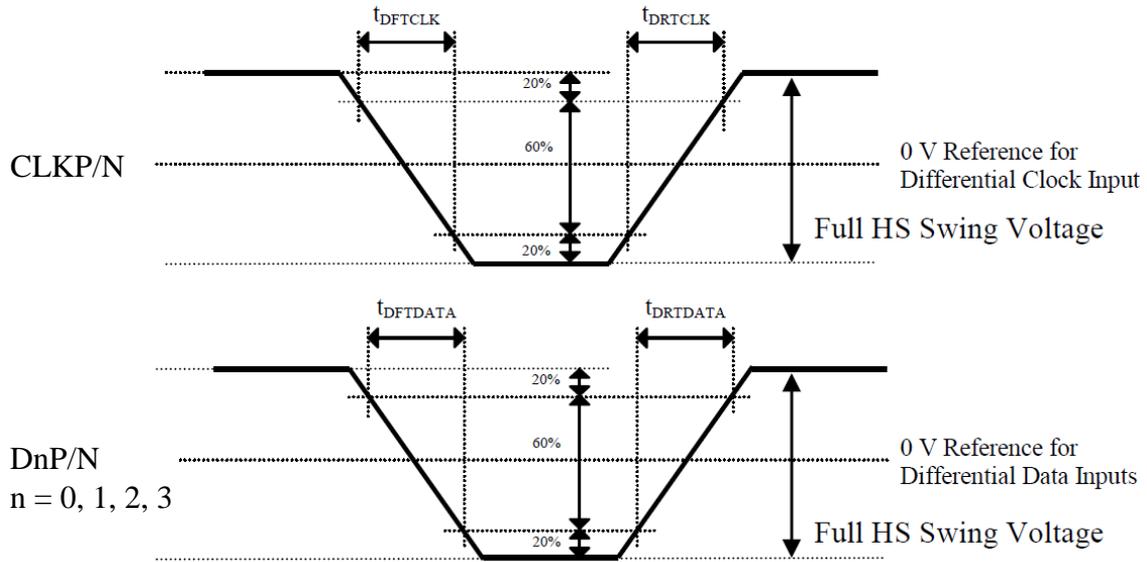


Figure 107: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.

17.4.5. Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C-04) are illustrated for reference purposes below.

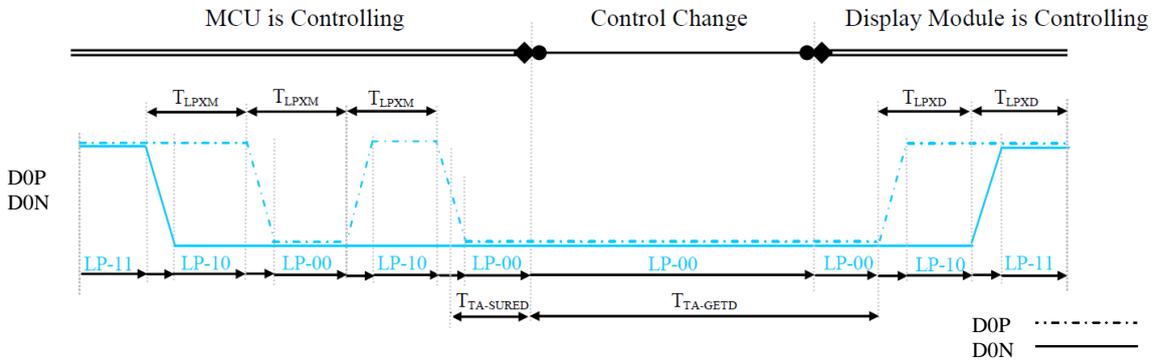


Figure 108: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C-04) to the MCU are illustrated for reference purposes below.

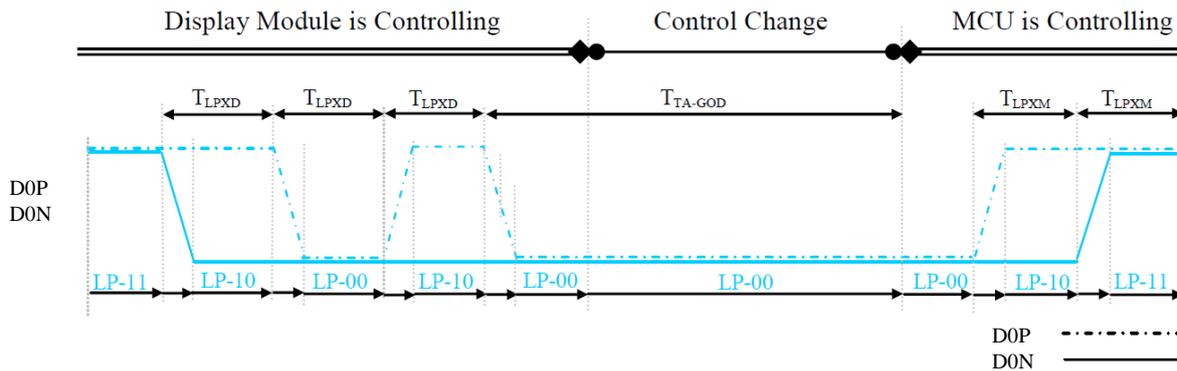


Figure 109: BTA from the Display Module to the MCU

Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (ILI9881C-04)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C-04) → MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C-04) starts driving	T_{LPXD}	$2 \times T_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C-04)	$5 \times T_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4 \times T_{LPXD}$	ns

17.4.6. Data Lanes from Low Power Mode to High Speed Mode

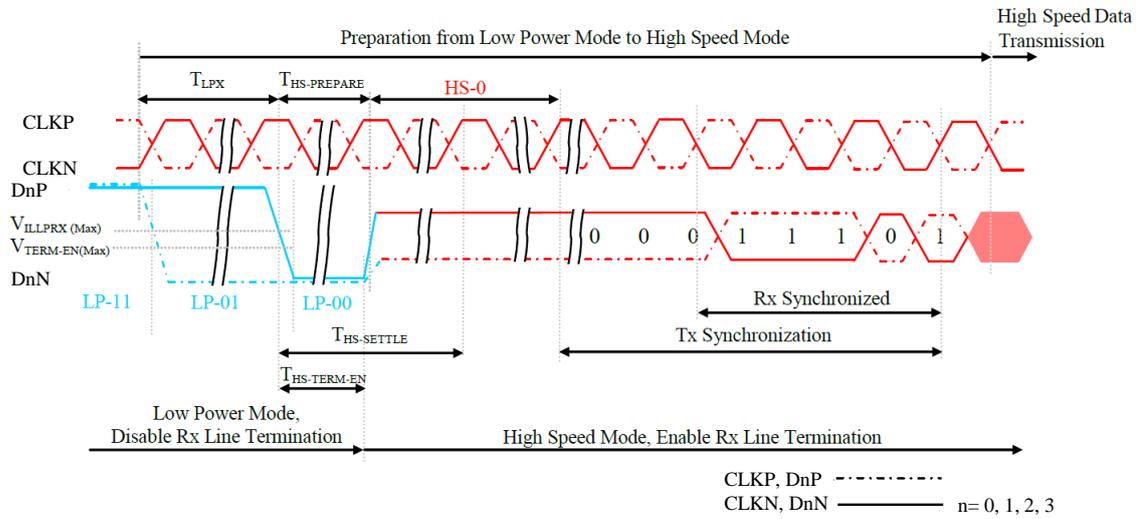


Figure 110: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T _{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	T _{HS-PREPARE}	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	T _{HS-TERM-EN}	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

17.4.7. Data Lanes from High Speed Mode to Low Power Mode

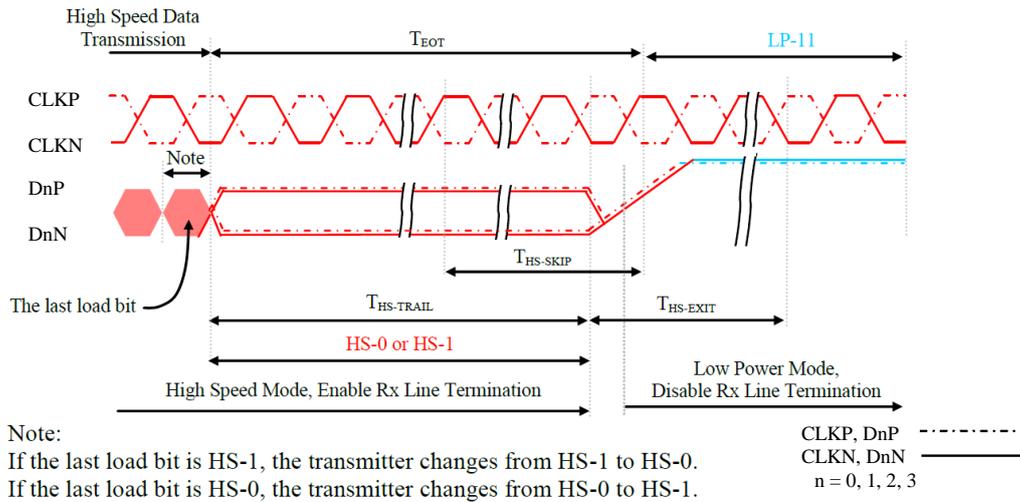


Figure 111: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C-04) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

17.4.8. DSI Clock Burst – High Speed Mode to/from Low Power Mode

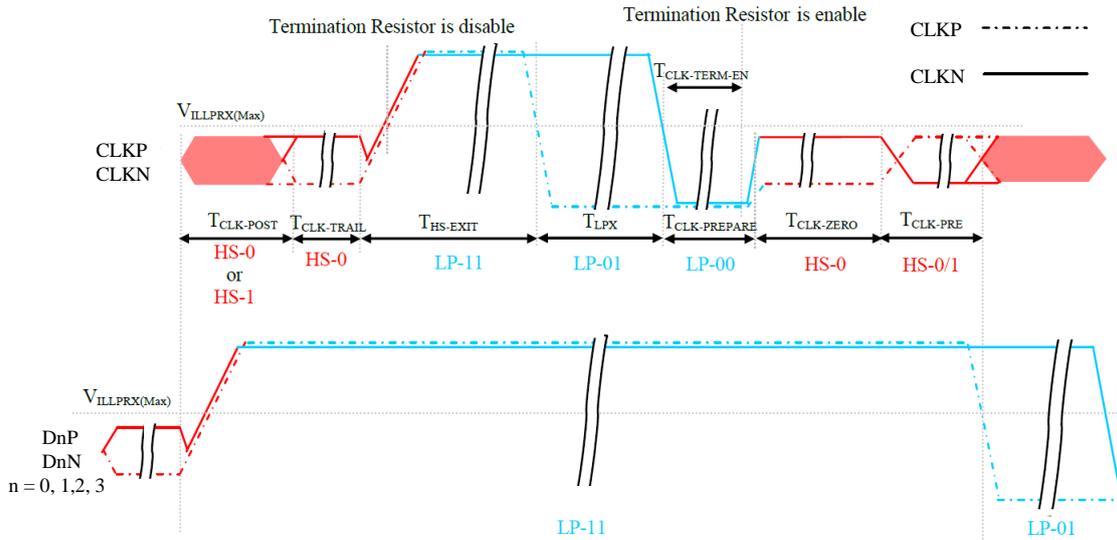
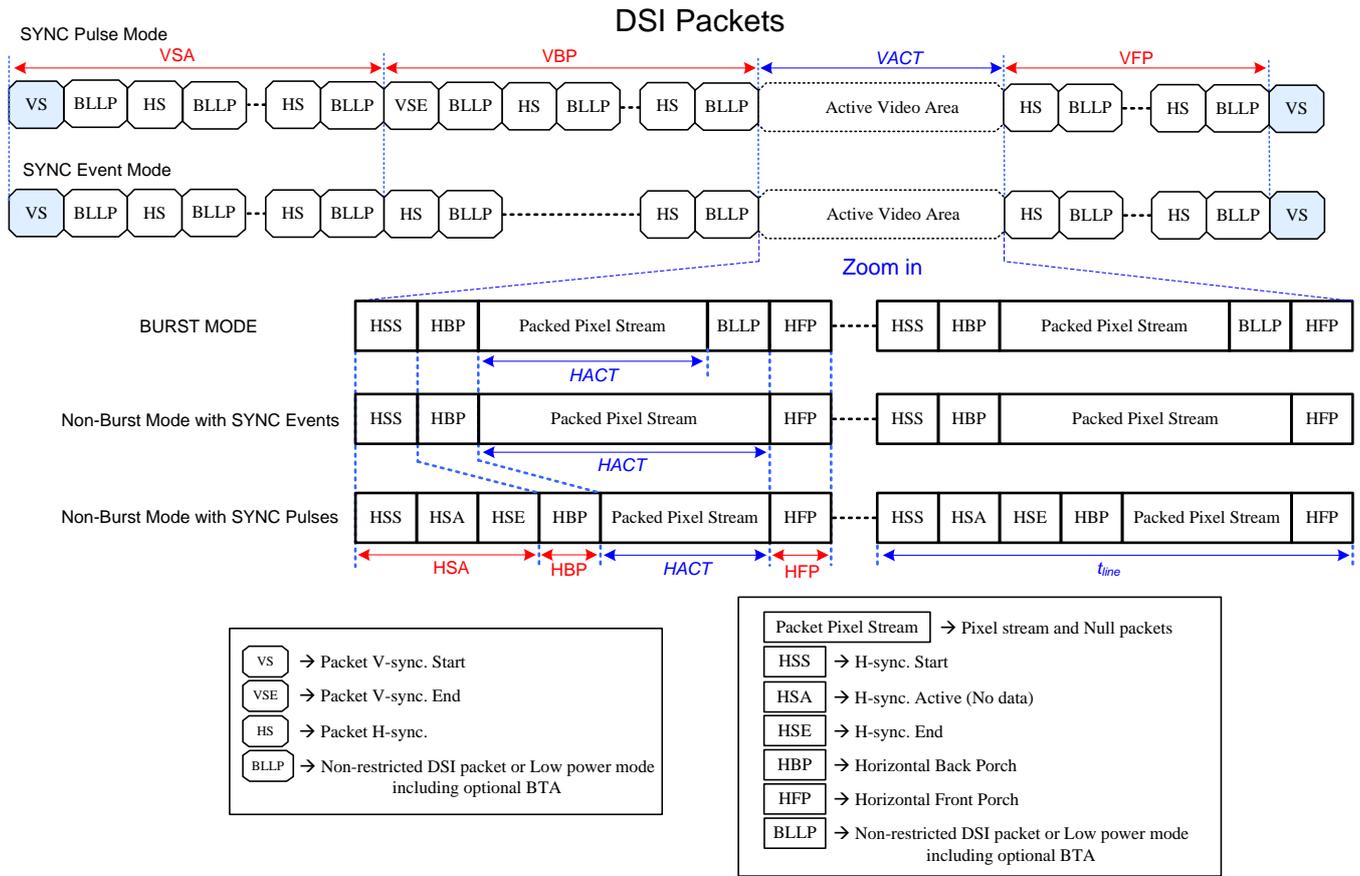


Figure 112: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	T _{CLK-POST}	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	T _{CLK-TRAIL}	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	T _{HS-EXIT}	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	T _{CLK-PREPARE}	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	T _{CLK-TERM-EN}	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	T _{CLK-PREPARE} + T _{CLK-ZERO}	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	T _{CLK-PRE}	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

17.4.9. Timing for DSI video mode



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	2 (Note 6)	-	-	Line
Vertical Back Porch	VBP	14 (Note 6)	-	-	Line
Vertical Front Porch	VFP	8 (Note 6)	-	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	2	-	-	Pixel
Horizontal Porch period	HSA + HBP + HFP	1.6	-	-	us
Active pixels per line	HACT	-	720	-	Pixel
Bit rate	BR _{bps}	385		Note 5	Mbps/lane

1 UI=1/Bit rate

$$HSA(\text{pixel}) = (tHSA \times \text{lane number}) / (UI \times \text{pixel format})$$

$$HBP(\text{pixel}) = (tHBP \times \text{lane number}) / (UI \times \text{pixel format})$$

$$HFP(\text{pixel}) = (tHFP \times \text{lane number}) / (UI \times \text{pixel format})$$

$$\text{Frame Rate} = \frac{BR_{\text{bps}} \times \text{Lane}_{\text{num}}}{(VACT + VSA + VBP + VFP) \times (HACT + HSA + HBP + HFP) \times \text{Pixel Format}}$$

Example : BR_{bps} = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, Lane_{num}=4(lane), Pixel Format=24(bit).

Note:

1. Lane_{num}: Date lane of MIPI-DSI.
2. Pixel Format: Please reference to “4.1DSI System Interface”.
3. The formula exists slightly error because of the host-transmission way.
4. The best frame rate setting : 2 data lanes : 50~60 Hz / 3 data lanes : 50~70 Hz / 4 data lanes : 50~70 Hz.
5. Please reference to “Table 39: Limited Clock Channel Speed”.
6. The minimum values of this table mean the limitation of IC without considering the panel GIP. The actual values of VSA, VBP and VFP will be changed by different panel GIP setting.

17.4.10. Reset Timing

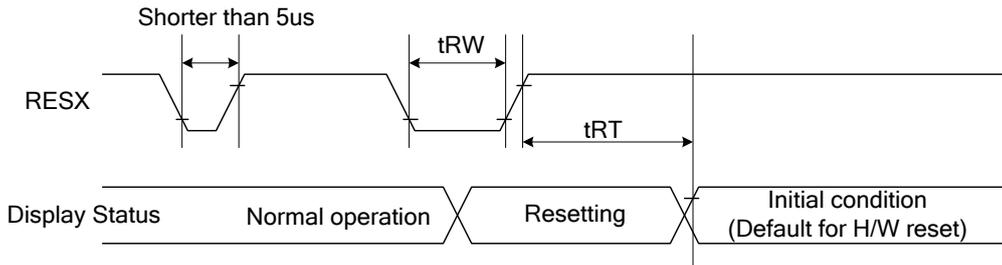


Figure 113: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5) 120 (note 1,6,7)	mS

Notes:

1. The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

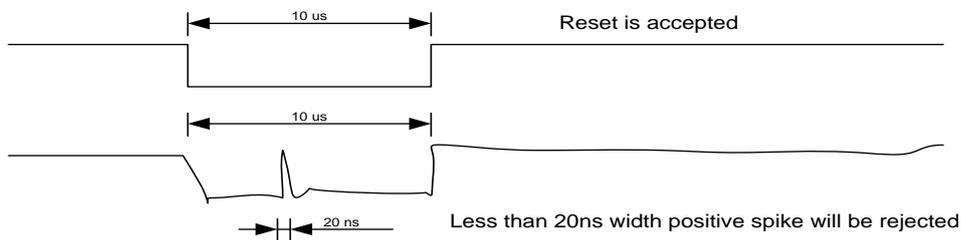


Figure 114: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

18. Panel Application

18.1. Input Power Type

ILI9881C-04 supports 3 kinds of input power type as shown below.

Table 49: Different Input Power Type

Setting	Input Power Type
<p>Power Mode 2A</p> <p>BOOSTM[2:0] = 1h DI_PWR_REG = 0h</p>	
<p>Power Mode 3</p> <p>BOOSTM[2:0] = 2h DI_PWR_REG = don't care</p>	
<p>Power Mode 4</p> <p>BOOSTM[2:0] = 1h DI_PWR_REG = 1h</p>	

18.2. Power Mode 2A (BOOSTM[2:0] = 1h, DI_PWR_REG = 0h)

18.2.1. Power Structure

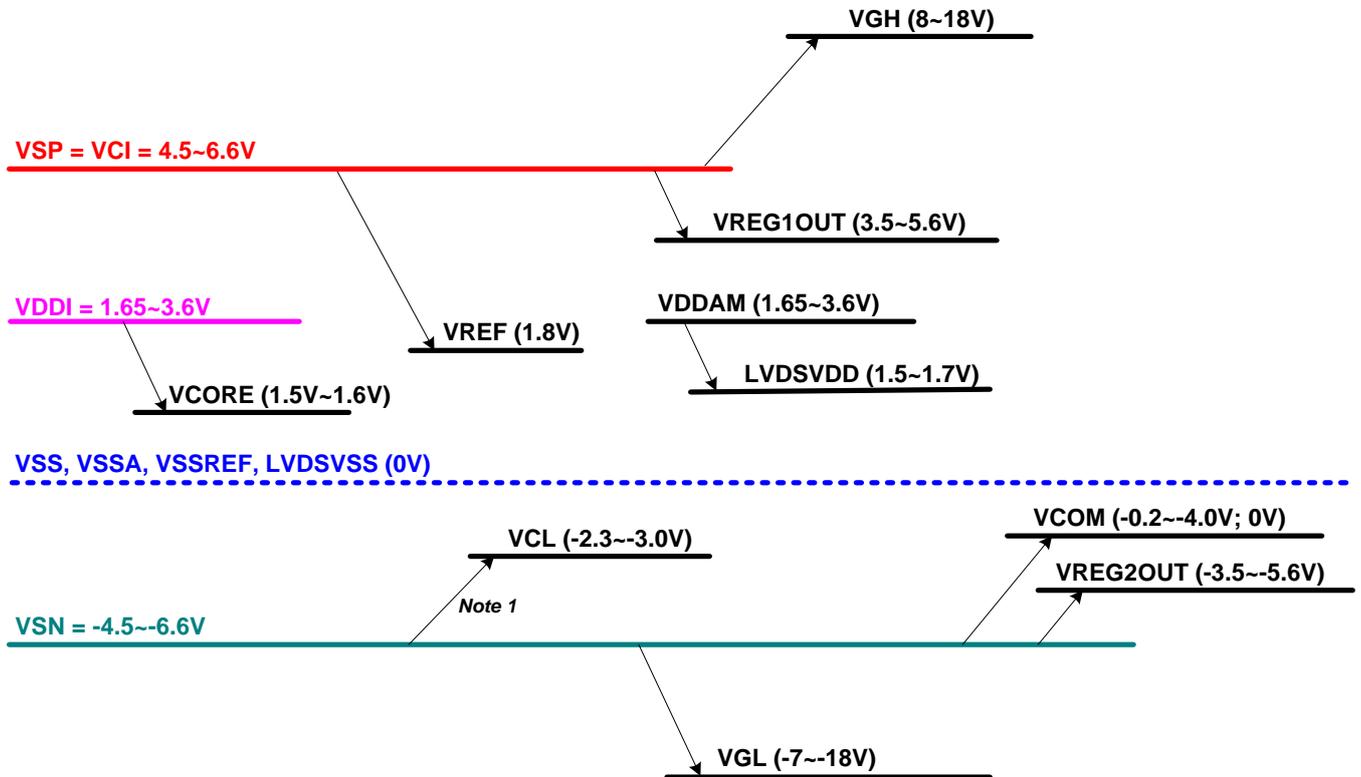
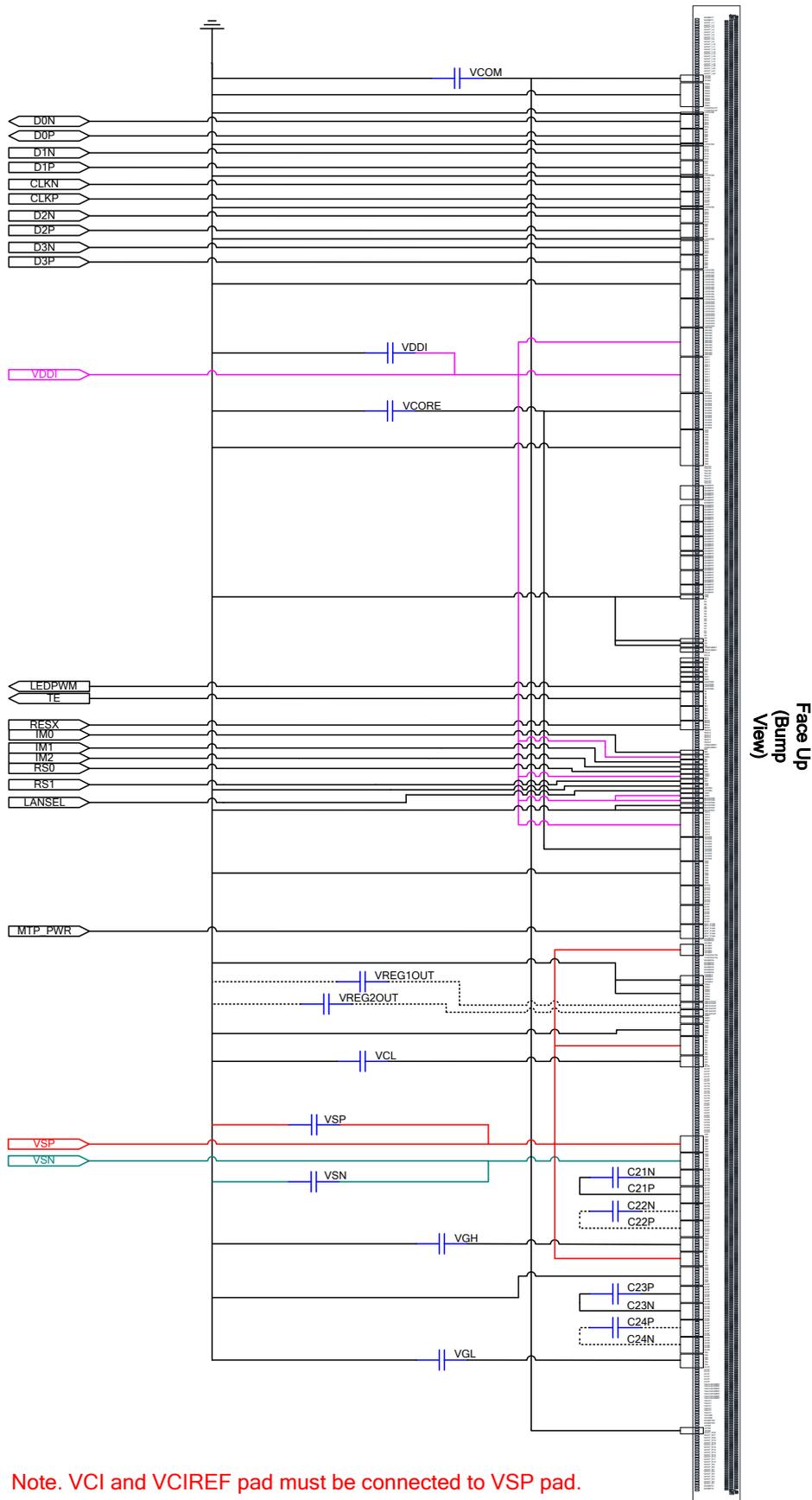


Figure 115: Power Structure of Power Mode 2A

Notes:

1. Please refer to "5.7.11 Power Control 3 (6Fh)".
2. The VREG1OUT, VREG2OUT, VCOM, VGH, VGL and VCL output voltage levels are lower than their theoretical levels (Ideal voltage levels) due to the current consumption at respective outputs.

18.2.2. Reference Circuit



Note. VCI and VCIREF pad must be connected to VSP pad.

Figure 116: Reference Circuit of Power Mode 2A

18.2.3. External Component

Table 50: External Component table of Power Mode 2A

N0.	Pad Name	Typical Value	Note	Reference Command (page)
1	VDDI	1.0uF / 6.3V	I/O and Digital Power	
2	VSP	2.2~4.7uF / 10V	Analog Power	
3	VSN	4.7uF / 10V	Analog Power	
4	VCORE	2.2uF / 6.3V		
5	VCL	1.0uF / 6.3V		
6	VREG1OUT	1.0uF / 10V	Optional	Register Page 4_R7Ah (page.242)
7	VREG2OUT	1.0uF / 10V	Optional	Register Page 4_R7Ah (page.242)
8	VCOM	2.2uF / 6.3V		
9	VGH	1.0uF / 25V		
10	VGL	1.0uF / 25V		
11	C21P/C21N	1.0uF / 16V		
12	C22P/C22N	1.0uF / 25V	Optional	Register Page 4_R6Fh (page.241)
13	C23P/C23N	1.0uF / 16V		
14	C24P/C24N	1.0uF / 25V	Optional	Register Page 4_R6Fh (page.241)

18.3. Power Mode 3 (BOOSTM[2:0] = 2h, DI_PWR_REG = don't care)

18.3.1. Power Structure

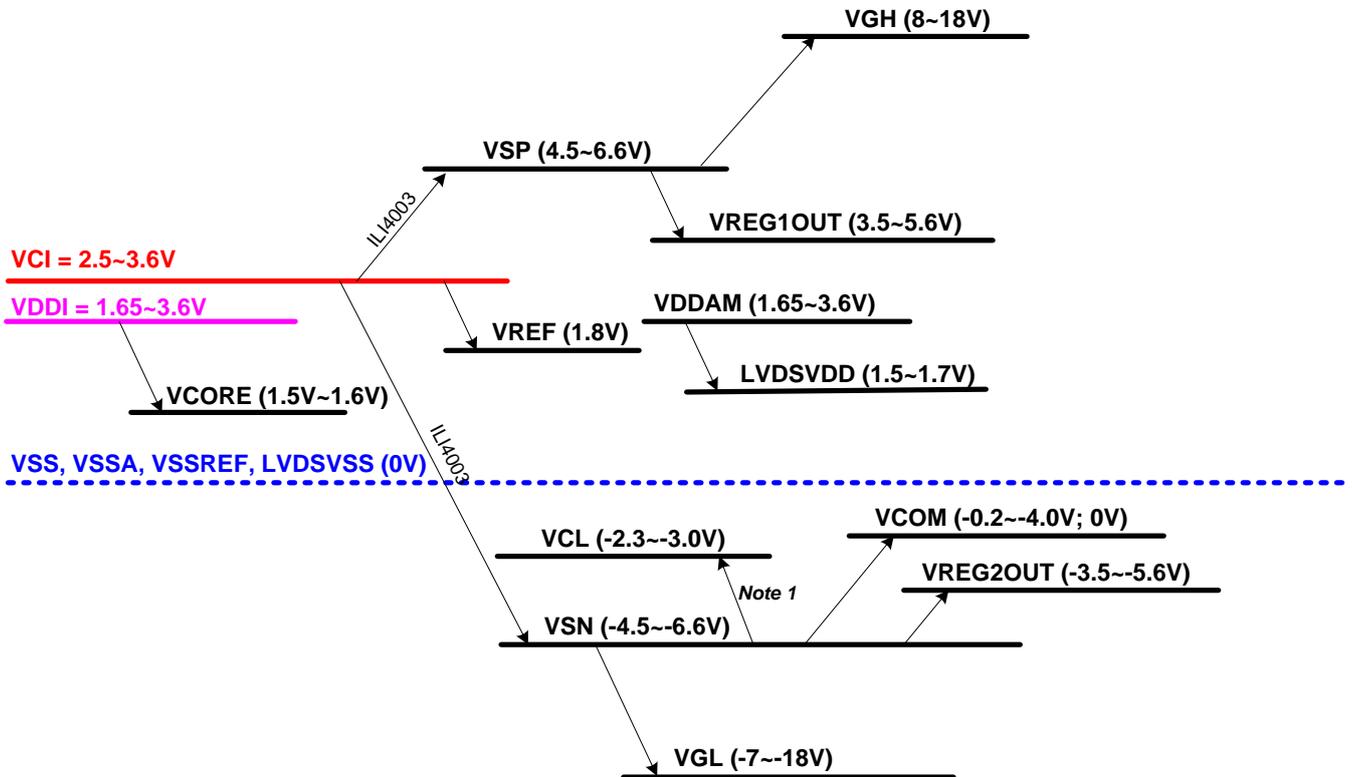


Figure 117: Power Structure of Power Mode 3

Notes:

1. Please refer to "5.7.11 Power Control 3 (6Fh)".
2. The VSP, VSN, VREG1OUT, VREG2OUT, VCOM, VGH, VGL and VCL output voltage levels are lower than their theoretical levels (Ideal voltage levels) due to the current consumption at respective outputs.

18.3.3. External Component

Table 51: External Component table of Power Mode 3

N0.	Pad Name	Typical Value	Note	Reference Command (page)
1	VCI	1.0uF / 6.3V	Analog Power	
2	VDDI	1.0uF / 6.3V	I/O and Digital Power	
3	VSP	2.2~4.7uF / 10V		
4	VSN	2.2~4.7uF / 10V		
5	VCORE	2.2uF / 6.3V		
6	VCL	1.0uF / 6.3V		
7	VREG1OUT	1.0uF / 10V	Optional	Register Page 4_R7Ah (page.242)
8	VREG2OUT	1.0uF / 10V	Optional	Register Page 4_R7Ah (page.242)
9	VCOM	2.2uF / 6.3V		
10	VGH	1.0uF / 25V		
11	VGL	1.0uF / 25V		
12	C21P/C21N	1.0uF / 16V		
13	C22P/C22N	1.0uF / 25V	Optional	Register Page 4_R6Fh (page.241)
14	C23P/C23N	1.0uF / 16V		
15	C24P/C24N	1.0uF / 25V	Optional	Register Page 4_R6Fh (page.241)
16	Q1		ILI4003	
17	C1P/C1N	2.2uF / 6.3V		
18	C2P/C2N	2.2uF / 6.3V		
19	C3P/C3N	2.2uF / 6.3V		

18.4. Power Mode 4 (BOOSTM[2:0] = 1h, DI_PWR_REG = 1h)

18.4.1. Power Structure

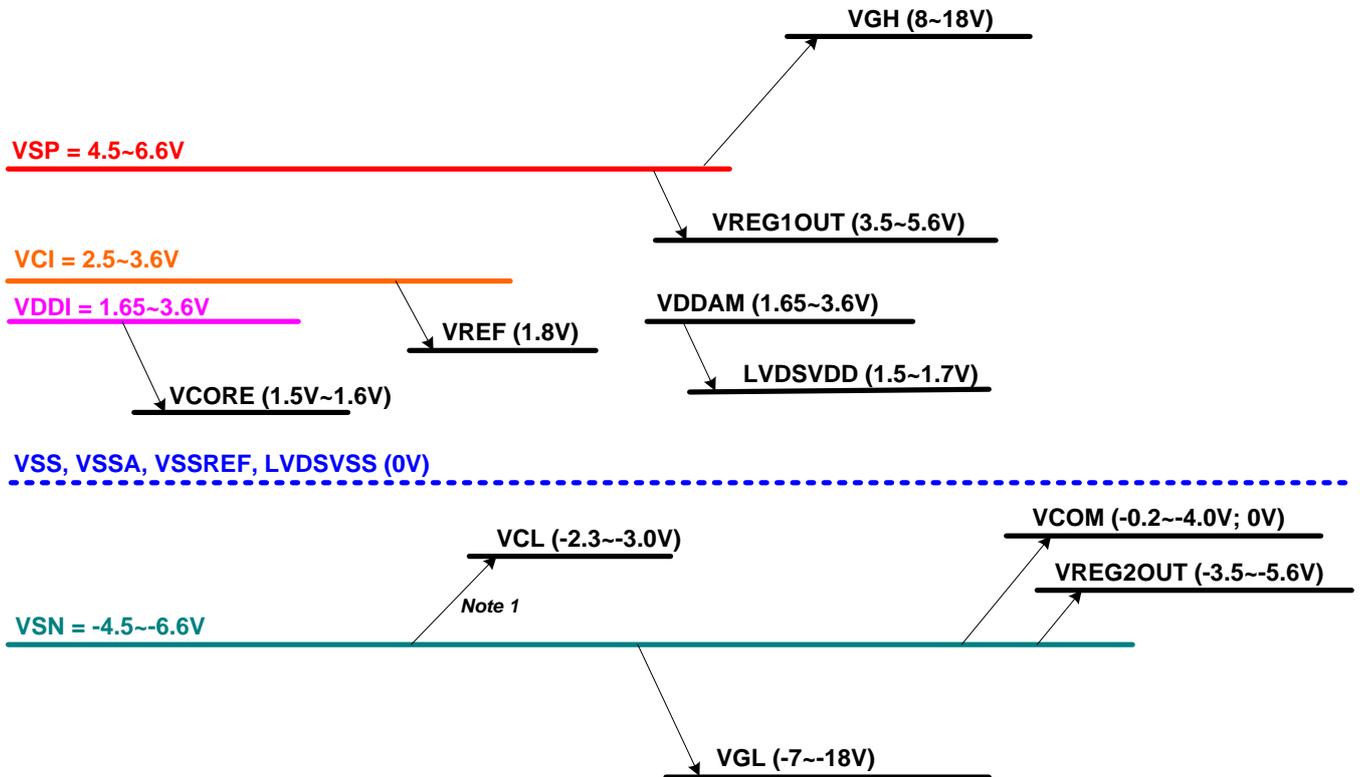


Figure 119: Power Structure of Power Mode 4

Notes:

1. Please refer to "5.7.11 Power Control 3 (6Fh)".
2. The VREG1OUT, VREG2OUT, VCOM, VGH, VGL and VCL output voltage levels are lower than their theoretical levels (Ideal voltage levels) due to the current consumption at respective outputs.

18.4.3. External Component

Table 52: External Component table of Power Mode 4

N0.	Pad Name	Typical Value	Note	Reference Command (page)
1	VDDI	1.0uF / 6.3V	I/O and Digital Power	
2	VCI	1.0uF / 6.3V	Analog Power	
3	VSP	2.2~4.7uF / 10V	Analog Power	
4	VSN	4.7uF / 10V	Analog Power	
5	VCORE	2.2uF / 6.3V		
6	VCL	1.0uF / 6.3V		
7	VREG1OUT	1.0uF / 10V	Optional	Register Page 4_R7Ah (page.242)
8	VREG2OUT	1.0uF / 10V	Optional	Register Page 4_R7Ah (page.242)
9	VCOM	2.2uF / 6.3V		
10	VGH	1.0uF / 25V		
11	VGL	1.0uF / 25V		
12	C21P/C21N	1.0uF / 16V		
13	C22P/C22N	1.0uF / 25V	Optional	Register Page 4_R6Fh (page.241)
14	C23P/C23N	1.0uF / 16V		
15	C24P/C24N	1.0uF / 25V	Optional	Register Page 4_R6Fh (page.241)

18.5. Maximum Layout Resistance

Table 53: Maximum Layout Resistance

Pad Name	Type	Maximum series resistance	Unit
VCI	Power Supply	5	Ω
VCIREF	Power Supply	10	Ω
VDDI	Power Supply	5	Ω
VCC1	Power Supply	5	Ω
VCC2	Power Supply	5	Ω
VDDAM	Power Supply	5	Ω
VSP	Power Supply	5	Ω
VSN	Power Supply	5	Ω
VSSA	Ground	5	Ω
VSSREF	Ground	10	Ω
LVDSVSS	Ground	50	Ω
VSS	Ground	5	Ω
MTP_PWR	Power Supply	5	Ω
VREG1OUT	Analog	20	Ω
VERG2OUT	Analog	20	Ω
VCL	Analog	5	Ω
VGH	Analog	10	Ω
VGL	Analog	10	Ω
EXTP	Output	10	Ω
EXTN	Output	10	Ω
LVDSVDD	Analog	5	Ω
VREF	Analog	20	Ω
VCORE	Analog	5	Ω
C21P, C21N, C22P, C22N C23P, C23N, C24P, C24N	Step-up Capacitor	5	Ω
IM[2:0], RS[1:0] LANSEL, BOOSTM[2:0]	Input	100	Ω
RESX	Input	100	Ω
TE, TE1, LEDPWM	Output	50	Ω
CLKP, CLKN D1P, D1N D2P, D2N D3P, D3N	Input	5	Ω
D0P, D0N	Input + Output	5	Ω
CSX, DCX, SCL, SDI	Input	100	Ω
SDO	Output	100	Ω
GOUT_L[22:1] GOUT_R[22:1]	Output	10	Ω
VCOM	Analog	5	Ω
VTESTOUTP	Analog	100	Ω
VTESTOUTN	Analog	100	Ω
TOUT[3:0]	Input + Output	100	Ω
TEST[5:0]	Input + Output	100	Ω
VS, HS	Input + Output	100	Ω
PCLK	Input	100	Ω
D[7:0]	Input + Output	50	Ω

19. Liquid Crystal Power Supply Specifications

Table 54: Liquid Crystal Power Supply Specifications

Item		Description
TFT Source Driver		2404 pins , 800(RGB)
TFT Gate Driver Control Signal		44 pins
TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
Liquid Crystal Drive Output	S1 ~ 2400, SDUM[3:0]	V0 ~ V255 grayscales
	GOUT_L/R[22:1]	VGH – VGL
	VCOM	-4.0 ~ -0.2V; 0V
Input Power Voltage	VCI	2.50 ~ 6.6V
	VCIREF	2.50 ~ 6.6V
	VDDI	1.65 ~ 3.6V
	VCC1	1.65 ~ 6.6V
	VCC2	1.65 ~ 6.6V
	VDDAM	1.65 ~ 3.6V
	VSP	4.5 ~ 6.6V
	VSN	-6.6 ~ -4.5V
Liquid Crystal Drive Voltages	VGH	8.0V ~ 18.0V
	VGL	-18.0V ~ -7.0V
	VCL	-3.0V ~ -2.3V
	VGH – VGL	Max. 32.0V
Internal Step-up Circuits	VGH	2xVSP or 2.5xVSP or 3*VSP or 3.5*VSP or 4*VSP or 4.5*VSP or 5*VSP
	VGL	-1.5xVSP or -2xVSP or -2.5xVSP or -3xVSP or -3.5xVSP or -4xVSP or -4.5xVSP or -5xVSP

20. Revision History

Version No.	Date	Page	Description
V100	2018/05/01	All	New created