SPECIFICATIONS FOR LCD MODULE

CUSTOMER	
MODEL	**SCT024001-V02**
CUSTOMER APPROVED	

APPROVED BY	CHECKED BY	ORGANIZED BY
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RECORDS OF REVISIONS

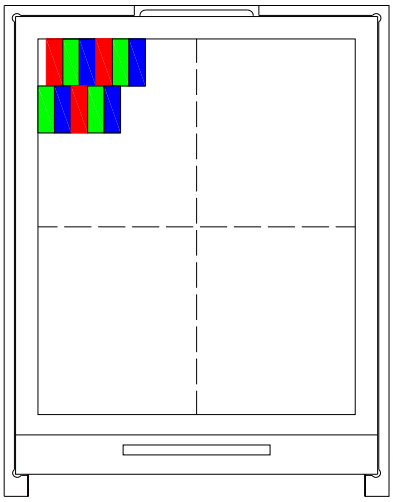
Revision No	Revision Date	Description
Ver: A0	2013-11-1	First release

CONTENTS

1. General Description

This LCM SCT024001-V02 is a TFT LCD module, comprising a 480-channel source driver, a 234-channel gate driver, 480 x 234 dots graphic, and power supply circuit. The 262k color can be display.

This TFT-LCD has 2.36 inch diagonally measured active display area with 480x234 resolution.



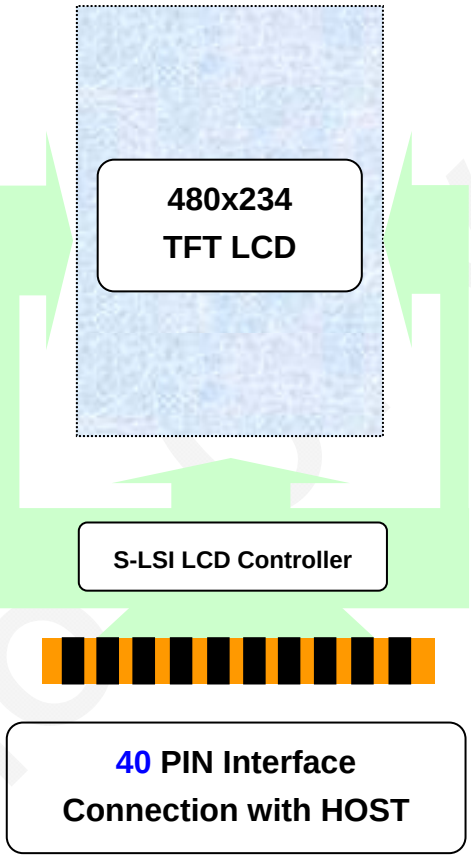
1.1 Mechanical Specifications

Item	Nominal Dimension	Unit
Dot Matrix	480 x 234	Dots
Module Size (W×H×T)	55.2 x 47.55 x 2.8	mm.
Active Area (W×H)	48.0 x 35.685	mm.
Pixel arrangement	RGB Delta Stripe	mm.
Color depth	262K（MAX）	colors
Interface	8 bit RGB	-
Driving IC Package	COG	-

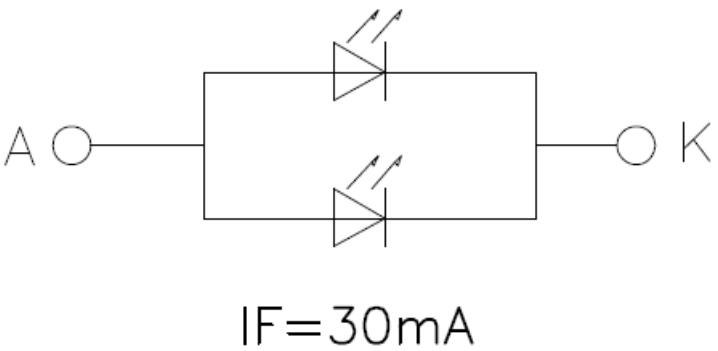
1.2 Display Specifications

Item	Nominal Dimension	Unit
Operating temperature	-20 ~70	℃
Storage temperature	-30~80	℃
LCD Type	a-Si TFT	-
LCD Mode	TN/Normal White	-
Backlight Type	LED x 2	PCS

1.3 Block Diagram



1.4 Back-light Unit

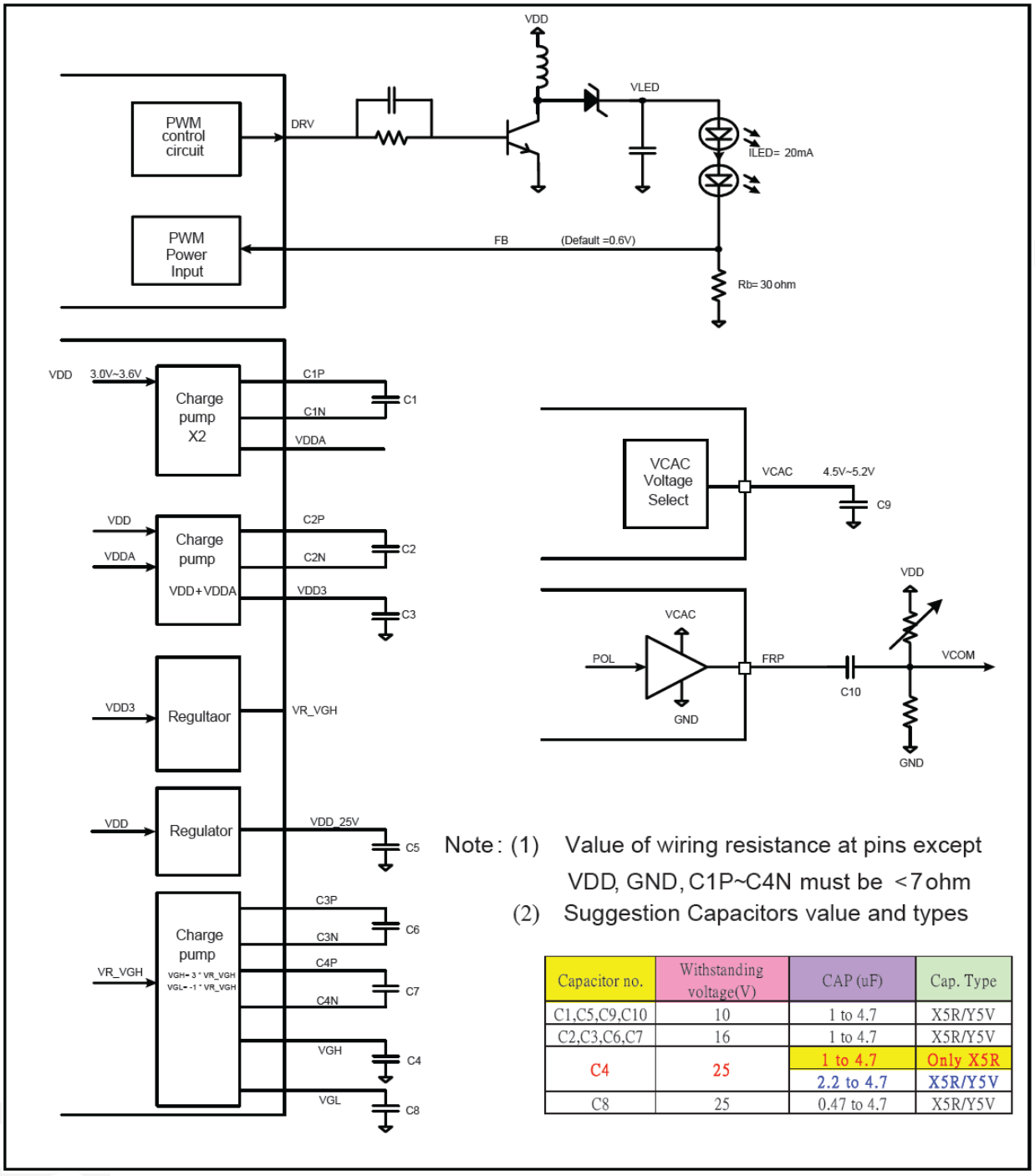


1.5 Interface Pin

Pin No	Pin Symbol	Level	Description
1-2	NC		
3	C1N	-	Pins to connect capacitors for power circuitry
4	C2N	-	Pins to connect capacitors for power circuitry
5	C1P	-	Pins to connect capacitors for power circuitry
6	C2P	-	Pins to connect capacitors for power circuitry
7-9	NC		
10	VDD3	-	Intermediate voltage for charge pump
11	VDD_25V	-	Intermediate voltage for charge pump
12	AGND	-	Power ground
13	NC		
14	VCAC	-	Intermediate voltage for charge pump
15	C3P	-	Pins to connect capacitors for power circuitry
16	C3N	-	Pins to connect capacitors for power circuitry
17	DRV	-	Gate signal for the power transistor of the boost converter
18	FB	-	Main boost regulator feedback input
19	LEDK	-	LED backlight Cathode
20-21	NC		
22	LEDA	-	Supply voltage for LED backlight Anode
23	GND	-	Power ground
24	VDD	-	Power supply for analog(1.8V-3.6V)
25	VSYNC	H/L	Frame synchronizing
26	HSYNC	H/L	Line synchronizing
27	DCLK	H/L	Data clock
28-35	D0-D7	H/L	Data input
36	SDA	H/L	Serial data input
37	SCL	H/L	Serial clock input
38	CSB	H/L	Serial chip select, Low enable
39	NC		
40	GRB	H/L	Global reset pin

Note1:VCOM=+5.0V Vp-p(Typ.)

Note2: The external capacitor is required on the those pin as following



Note: (1) Value of wiring resistance at pins except VDD, GND, C1P~C4N must be <7ohm

(2) Suggestion Capacitors value and types

Capacitor no.	Withstanding voltage(V)	CAP (uF)	Cap. Type
C1,C5,C9,C10	10	1 to 4.7	X5R/Y5V
C2,C3,C6,C7	16	1 to 4.7	X5R/Y5V
C4	25	1 to 4.7	Only X5R
		2.2 to 4.7	X5R/Y5V
C8	25	0.47 to 4.7	X5R/Y5V

Note3:VDD,VDDIO=+3.3V(Typ.)

Note4:Outputs the control signal of switching regulator for LED.Duty cycle varies according to FB input voltage

Note5:Feedback signal of switching signal for LED.It controls DRV output duty cycle with 0.6V input level sense.So Rb should be adjust for ILED.

Note6:HSYNC is a "Low" active signal

Note7:VSYNC is a "Low" active signal

Note8:DCLK timing for data loading defined at rising edge.

2. Interface Timing

2.1 RAW DATA MODE

The below specifications apply for:

SEL2	SEL1	SEL0
0	0	0

Table 7: RAW DATA MODE 480x240 AC characteristics (VDD=3.3V, AGND=GND=0V, T_{OPR} = -30°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DCLK frequency	Fclk		-	9.7	-	MHz
DCLK period	Tcph		-	103	-	ns
Delay from Hsync to Source Output	Thso		-	56	-	DCLK
Delay from Hsync to Gate Output	Thgo		-	45	-	DCLK
Delay from Hsync to Gate Output off	Thgz		-	19	-	DCLK
Delay from Hsync to 1st data input	Ths	Function of DDL[4..0] settings	84	100	115	DCLK
DC converter osc. Frequency	Fosc	Fclk/32	-	303.1	-	kHz

2.2 SERIAL RGB MODE

The below specifications apply for:

SEL2	SEL1	SEL0
0	0	1

Table 8: SERIAL MODE, AC characteristics (VDD=3.3V, AGND=GND=0V, T_{OPR} = -30°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DCLK frequency	Fclk		-	24.54/27	-	MHz
DCLK cycle time	Tcph		-	40/37	-	ns
Delay from Hsync to Source Output	Thso		-	143	-	DCLK
Delay from Hsync to Gate Output	Thgo		-	113	-	DCLK
Delay from Hsync to Gate Output off	Thgz		-	48	-	DCLK
Delay from Hsync to 1st data input	Ths	Function of DDL[4..0] settings	236	252	267	DCLK
DC converter osc. Frequency	Fosc	Fclk/64 = 383.4kHz / 421.9kHz	-	383.4 / 421.9	-	kHz

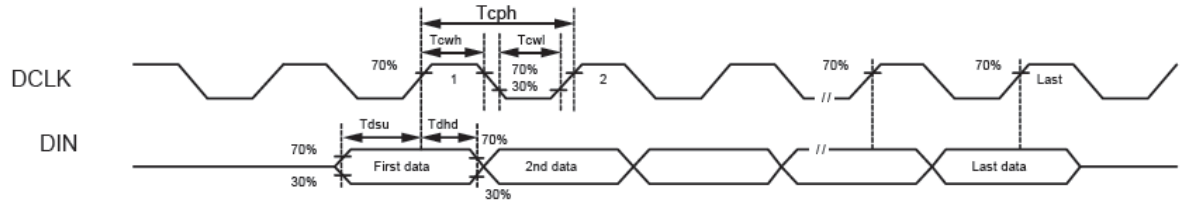
2.3 CCIR

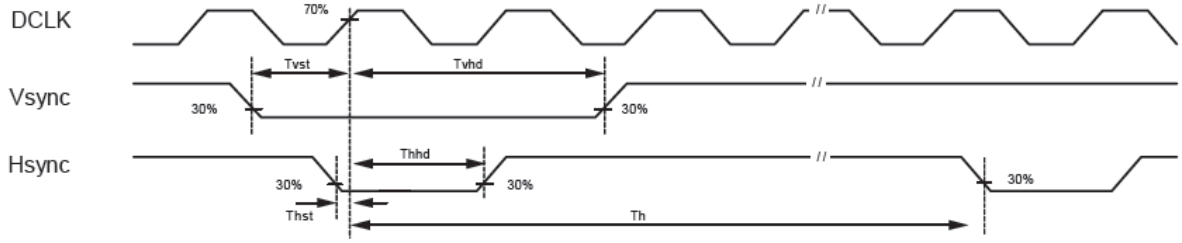
The below specifications apply for:

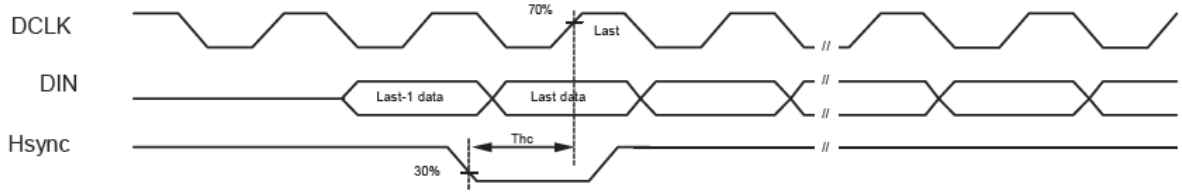
SEL2	SEL1	SEL0
1	1	1

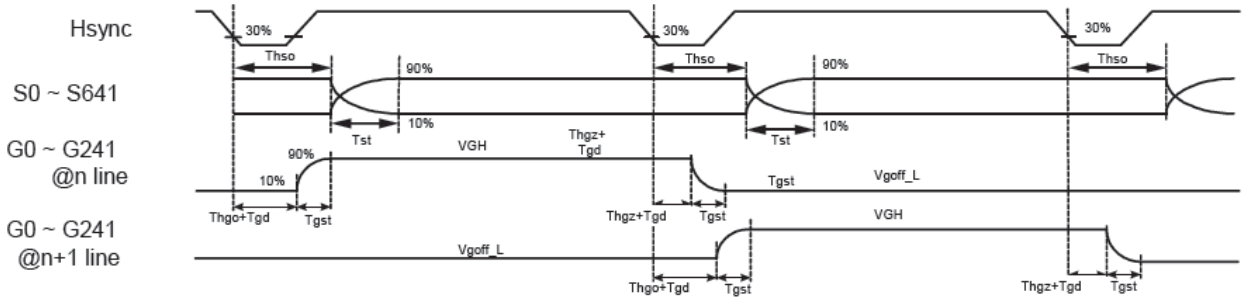
Table 9:CCIR MODE, AC characteristics (VDD=3.3V, AGND=GND=0V, T_{OPR} = -30°C to +85°C)

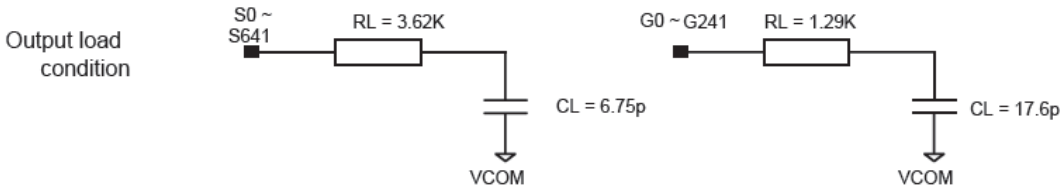
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DCLK frequency	Fclk		-	27	-	MHz
DCLK cycle time	Tcph		-	37	-	ns
CLK pulse duty	Tcw		40	50	60	%
Delay from EAV to Source Output	Thso		-	143	-	DCLK
Delay from EAV to Gate Output	Thgo		-	113	-	DCLK
Delay from EAV to Gate Output off	Thgz		-	48	-	DCLK
Delay from EAV to 1st data input	Ths	Function of DDL[4..0] settings	257	273	288	DCLK
DC converter osc. Frequency	Fosc	Fclk/64	-	421.9	-	kHz

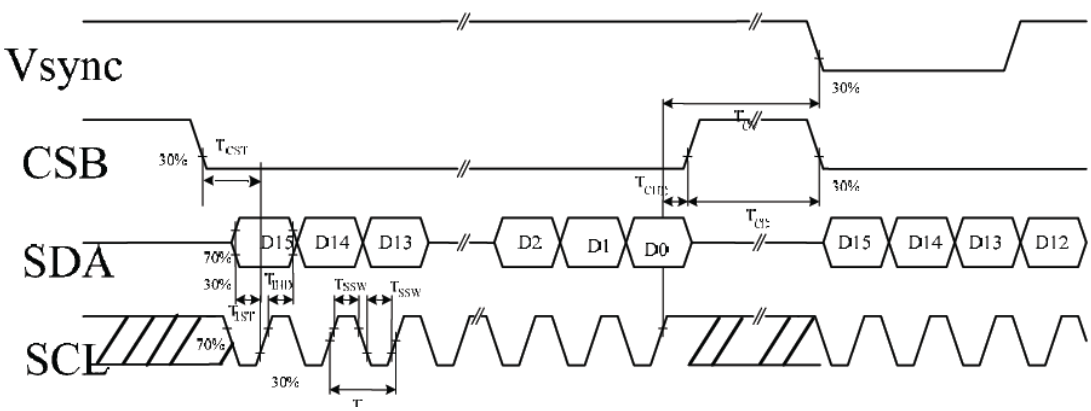

Tcph
Tcwh
Tcwl
DCLK
DIN
70%
30%
Tdsu
Tdhd
First data
2nd data
Last data
Last

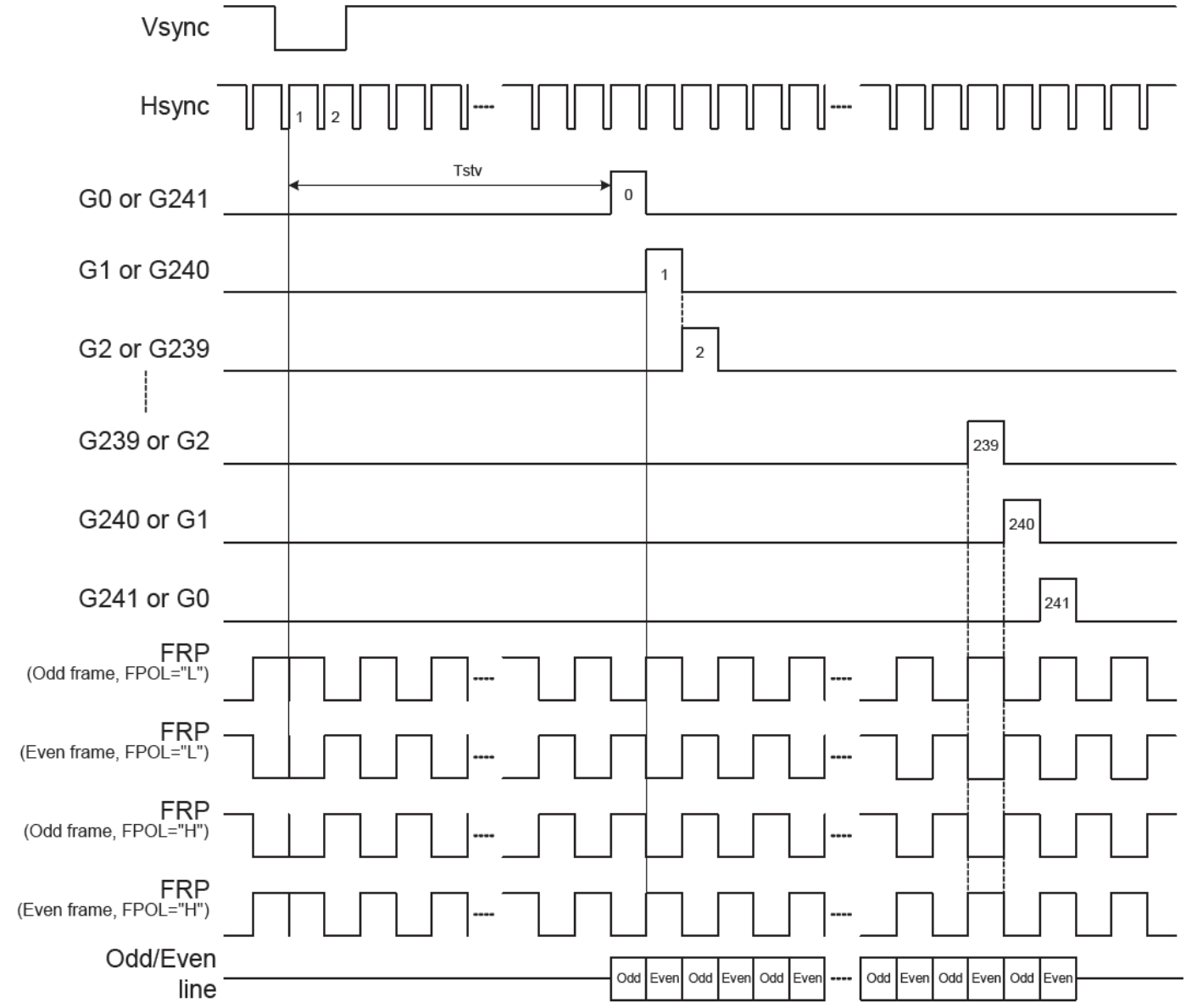

DCLK
Vsync
Hsync
Tvst
Tvhd
Thhd
Thst
Th
30%
70%


DCLK
DIN
Hsync
Last-1 data
Last data
Last
Thc
70%
30%

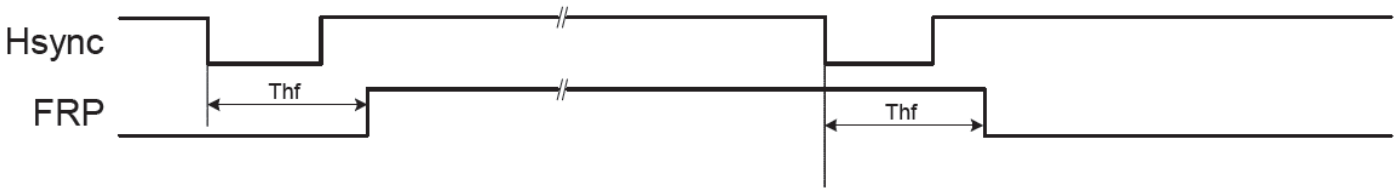

Hsync
S0 ~ S641
G0 ~ G241
@n line
G0 ~ G241
@n+1 line
Thso
Tst
Thgo+Tgd
Tgst
Thgz+Tgd
VGH
Vgoff_L
90%
10%
30%


Output load
condition
S0 ~
S641
RL = 3.62K
CL = 6.75p
VCOM
G0 ~ G241
RL = 1.29K
CL = 17.6p
VCOM


Vsync
CSB
SDA
SCL
30%
70%
D15
D14
D13
D2
D1
D0
D12



Note: SD Line 1,3,5,…, 241 =Odd line, : SD Line 2,5, 6,…, 242 =Even line



2.4 Vertical input timing

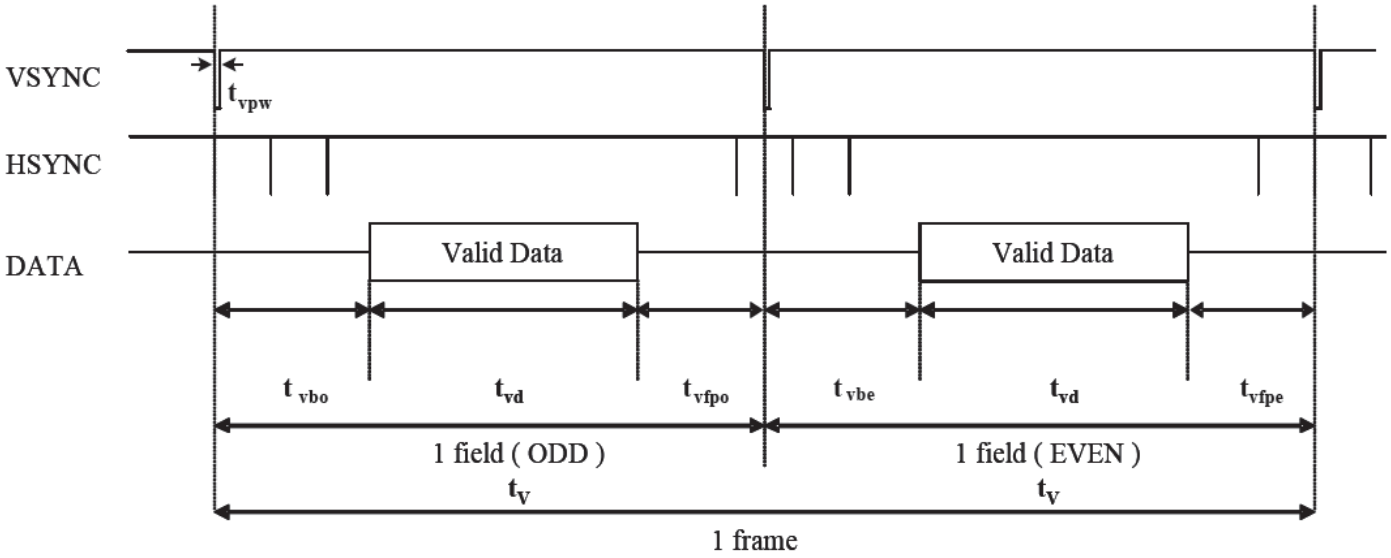


Figure 13: Vertical input timing diagram for interlace application

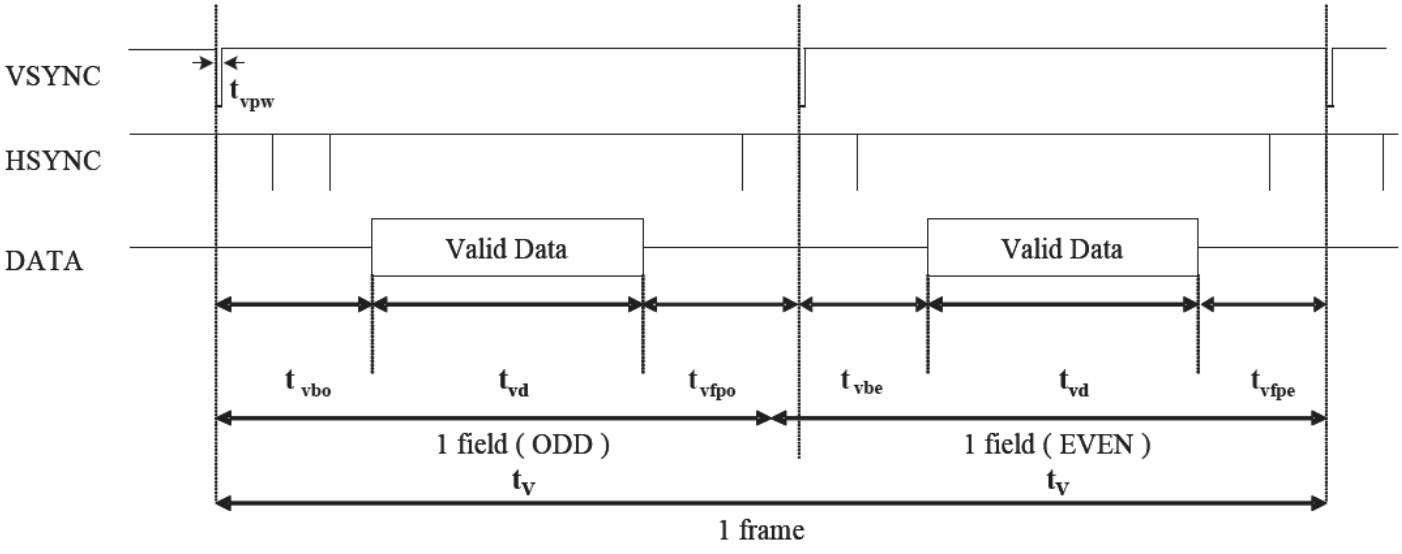


Figure 14: Vertical input timing diagram for non-interlace application

2.4.1 Raw data vertical input timing

Parameter		Symbol	Interlace			(*)Non-Interlace			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Vertical display area		t_{vd}		240			240		H
VSYNC period time		t_v	247.5	262.5	277.5	247	262	277	H
VSYNC pulse width		t_{vpw}	1 DCLK	1H	6H	1 DCLK	1H	6H	
(*)VSYNC Blanking (t_{vb})	Odd field	t_{vbo}	6	13	21	6	13	21	H
	Even field	t_{vbe}	6.5	13.5	21.5				
VSYNC Front porch (t_{vfp})	Odd field	t_{vfpo}	1.5	9.5	16.5	1	9	16	H
	Even field	t_{vfpe}	1	9	16				

2.4.2 SERIAL RGB vertical input timing

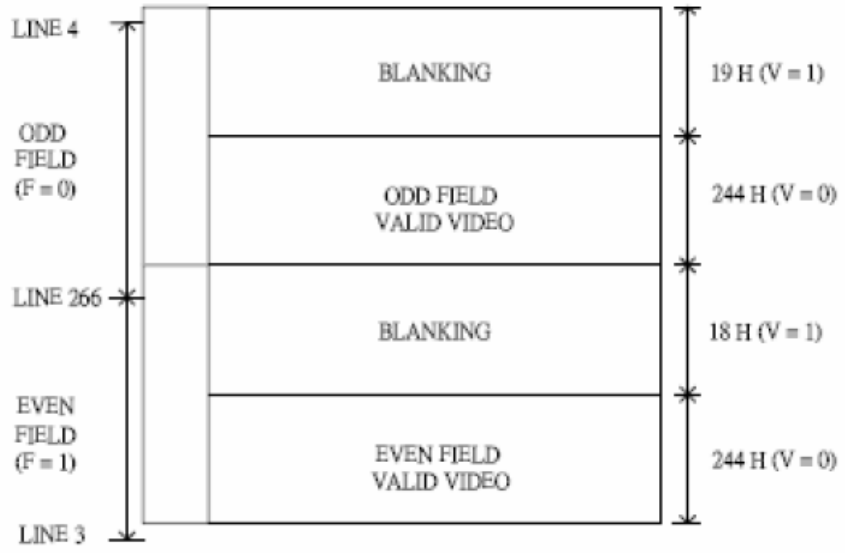
NTSC

Parameter		Symbol	Interlace			(*)Non-Interlace			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Vertical display area		t_{vd}		240			240		H
VSYNC period time		t_v	247.5	262.5	277.5	247	262	277	H
VSYNC pulse width		t_{vpw}	1 DCLK	1H	6H	1 DCLK	1H	6H	
(*)VSYNC Blanking (t_{vb})	Odd field	t_{vbo}	6	13	21	6	13	21	H
	Even field	t_{vbe}	6.5	13.5	21.5				
VSYNC Front porch (t_{vfp})	Odd field	t_{vfpo}	1.5	9.5	16.5	1	9	16	H
	Even field	t_{vfpe}	1	9	16				

PAL

Parameter		Symbol	Interlace			(*)Non-Interlace			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Vertical display area		t_{vd}		288(280)			288(280)		H
VSYNC period time		t_v	295.5 (287.5)	312.5	325.5 (317.5)	295 (287)	312	325 (317)	H
VSYNC pulse width		t_{vpw}	1 DCLK	1H	6H	1 DCLK	1H	6H	
(*)VSYNC Blanking (t_{vb})	Odd field	t_{vbo}	6	13	21	6	13	21	H
	Even field	t_{vbe}	6.5	13.5	21.5				
VSYNC Front porch (t_{vfp})	Odd field	t_{vfpo}	1.5	11.5(19.5)	16.5	1	11(19)	16	H
	Even field	t_{vfpe}	1	11(19)	16				

(*) Non-interlace mode: NTSC is 262 lines (typical), but 263 is tolerant.
PAL is 312 lines (typical), but 313 is tolerant.



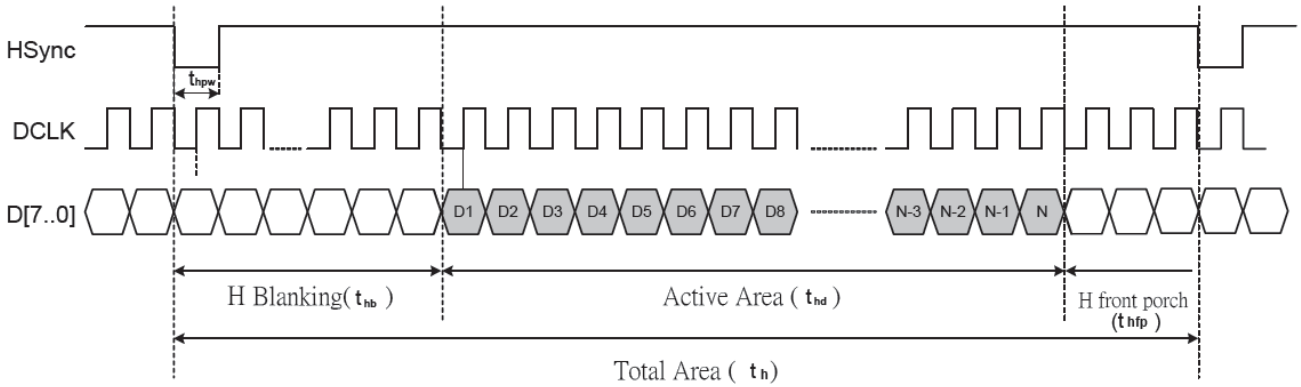
NTSC

PAL

	F	H	V
1	EVEN Field	EAV	BLANKING
0	ODD Field	SAV	VALID VIDEO

Figure 15: Illustration on SERIAL RGB vertical input timing

2.5 Horizontal input timing



2.5.1 Raw Data Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		t_{hd}	480			DCLK
DCLK frequency		f_{clk}	Min.	Typ.	Max	
			8.1	9.7	11.3	Mhz
1 Horizontal Line		t_h	617			DCLK
HSYNC pulse width	Min.	t_{hpw}	1			
	Typ.		1			
	Max.		96			
HSYNC blanking		t_{hb}	84	100	115	
HSYNC front porch		t_{hfp}	53	37	22	

2.5.2 SERIAL RGB MODE Horizontal input timing

NTSC

Parameter		Symbol	Value			Value			Value			Unit
Horizontal display area		t_{hd}	1280			1408			1440			DCLK
DCLK frequency		f_{clk}	Min.	Typ.	Max	Min.	Typ.	Max	Min.	Typ.	Max	
			20.47	24.54	28.66	22.5	27	31.5	22.5	27	31.5	MHz
1 Horizontal Line		t_h	1560			1716			1716			DCLK
HSYNC pulse width	Min.	t_{hpw}	1			1			1			
	Typ.		1			1			1			
	Max.		96			96			96			
HSYNC blanking		t_{hb}	237	252	268	237	252	268	237	252	268	
HSYNC front porch		t_{hfp}	43	28	12	71	56	40	39	24	8	

PAL

Parameter		Symbol	Value			Value			Unit
Horizontal display area		t_{hd}	1408			1440			DCLK
DCLK frequency		f_{clk}	Min.	Typ.	Max	Min.	Typ.	Max	
			22.5	27	31.5	22.5	27	31.5	MHz
1 Horizontal Line		t_h	1728			1728			DCLK
HSYNC pulse width	Min.	t_{hpw}	1			1			
	Typ.		1			1			
	Max.		96			96			
HSYNC blanking		t_{hb}	237	252	268	237	252	268	
HSYNC front porch		t_{hfp}	83	68	52	51	36	20	

2.5.3 CCIR Horizontal input timing

Parameter		Symbol	Mode(NTSC/PAL)	Unit
Horizontal display area		t_{hd}	1440	DCLK
DCLK frequency		f_{clk}	27	MHz
1 Horizontal Line		t_h	1716	DCLK
Internal HSYNC pulse width	Min.	t_{hpw}	1	
	Typ.		1	
	Max.		-	
HSYNC blanking		t_{hb}	268	

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit
Supply voltage for logic	VDDIO	0	+5V	V
Supply voltage	VDD	0	+5V	V
Operate temperature range	TOP	-20	70	℃
Storage temperature range	TST	-30	80	℃

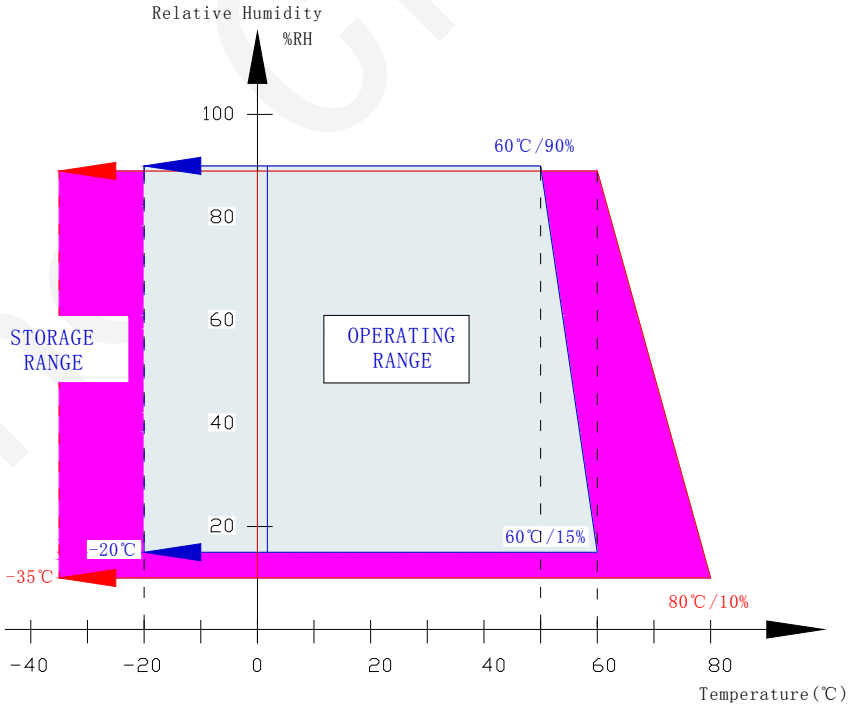
Note:

(1) 90%RH maximum humidity, 60℃ maximum wet-bulb temperature When operated at a temperature lower than 0℃,the LCD worked slowly and the screen appeared low-contrast images due to the characteristics of LC(Liquid Crystal).

(2) If any fixed pattern is displayed on LCD for minutes, image-sticking phenomenon may occur.

(3) Degradation could occur to pixels' TFT when DC BIOS is input into its gate-signal under POWER OFF WAITING STAND-BY & SLEEP MODE. Therefore, LCD should be turn off then.

(4) Please operate a LCD module on the basis of the recommended S/W(Register)



Temperature & Ilumidity Graph at Absolute Environment

DATA). If you want to change any part of the S/W, you must take driver's confirmation.

3.2 DC Characteristics

T_a= 25℃

Item	Symbol	Min	Typ	Max	Unit	Condition
Supply voltage (Logic)	VDDIO	1.8	3.3	3.6	V	
Input high level voltage	V_{IH}	0.8VDDIO	--	VDDIO	V	
Input low level voltage	V_{IL}	0	--	0.2 VDDIO	V	
Power supply current	I_{CC}+ I_{CI}	--	TBD	--	mA	
Backlight forward voltage	V_F	--	3.1	3.2	V	
Backlight forward current	I_F	--	30	40	mA	

4. Optical characteristics

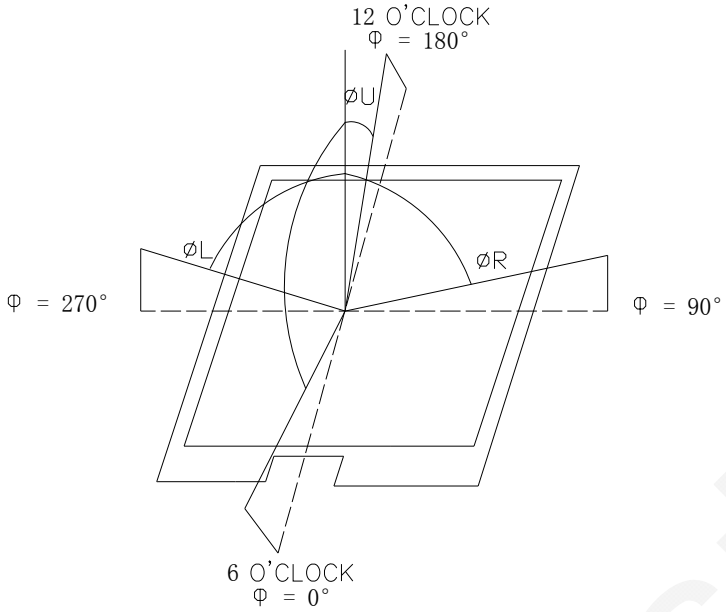
Parameter		Symbol	Condition	Min	Typ	Max	Unit	Note
Viewing angle		Left	CR≥10		30		Degree	(2)
		Right			30		Degree	
		Up			55		Degree	
		Down			40		Degree	
Color Chromaticity	Red	Rx	θ=0 Normal viewing angle	0.55	0.57	0.59	-	Color Chromaticity
		Ry		0.284	0.304	0.324	-	
	Green	Gx		0.277	0.297	0.317	-	
		Gy		0.516	0.536	0.556	-	
	Blue	Bx		0.119	0.139	0.159	-	
		By		0.126	0.146	0.166	-	
	White	Wx		0.277	0.297	0.317	-	
		Wy		0.309	0.329	0.349	-	
Contrast ratio		CR	optimal	-	300		-	(1)
Response time		Tr+Tf			25		ms	(3)

Note (1) Definition of contrast ratio

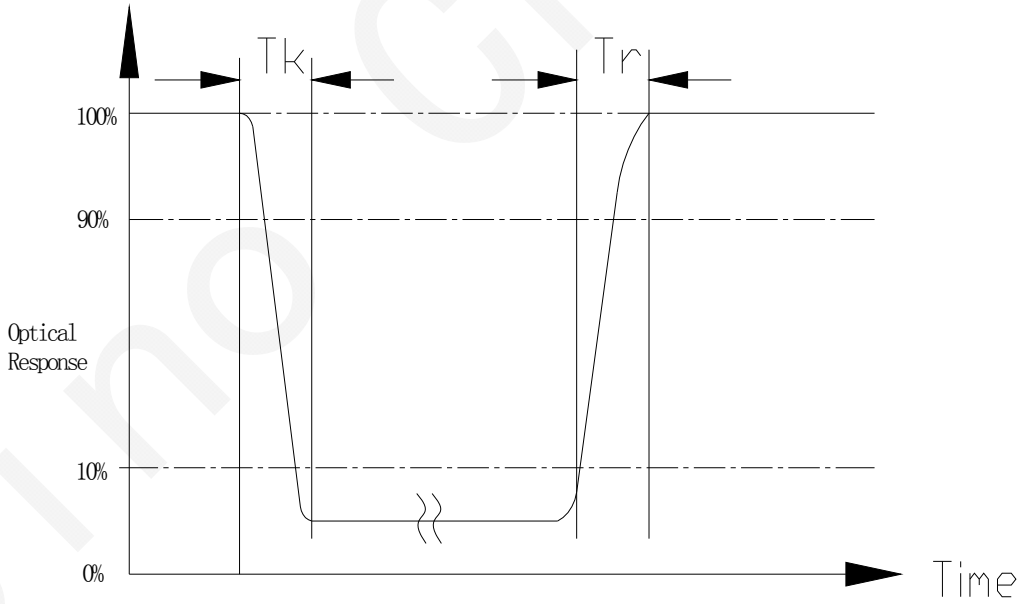
Measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixel white}}{\text{Luminance with all pixel black}}$$

Note (2) Definition of viewing angle



Note (3) Definition of response time: Tr+Tf



5. Reliability

5.1 Reliability Condition

*One single product test for only one item.

Item No	Item	Condition	Remark
1	High temperature Operating	60℃, 120Hours	Finish product (With polarizer)
2	Low temperature Operating	-10℃, 120 Hours	Finish product (With polarizer)
3	High temperature Storage	70℃, 200 Hours	Finish product (With polarizer)
4	Low temperature Storage	-20℃, 200 Hours	Finish product (With polarizer)
5	High temperature & humidity Storage	50℃, 90%RH, 120 Hours	Finish product (With polarizer)
6	Thermal Shock Storage (No operation)	-10℃ , 30min.<=> 60℃ , 30min. 10 Cycles	Finish product (With polarizer)
7	ESD test	Voltage:±8KV R:330 ohm,C:150pF Air discharge,10 times	Finish product (With polarizer)
8	Vibration test	10 => 55 =>10 => 55 => 10 Hz, within 1 minute;Amplitude:1.5mm. 15 minutes for each Direction (X,Y,Z)	Finish product (With polarizer)
9	Drop test	Packed, 100CM free fall 6 sides, 1 corner, 3edges	Finish product (With polarizer)

* Judgment after test: keep in room temperature for more than 2 hours.

- Current consumption < 2 times of initial value
- Contrast > 1/2 initial value
- Function: work normally

5.2 Inspection plan

Class	Item	Judgment	Class
Packing & Indicate	1.Outside and inside package	〝Model no.〞, 〝lot no.〞 and 〝quantity〞 Should indicate on the package.	Minor
	2.Model mixed and quantity	Other model mixed…….rejected. Quantity short or over….rejected.	Critical
	3.Product indication	〝Model no.〞 should indicate on the product	Major
Assembly	4.Dimension,LCD glass scratch And scribe defect	According to specification or drawing	Major
Appearance	5.Viewing area	Polarizer edge or LCD's sealing line is visible in the viewing area …..rejected	Minor
	6.Blemish、black spot、 White spot in the LCD And LCD glass cracks	According to standard of visual inspection（inside viewing area）	Minor
	7. Blemish、black spot White spot and scratch on the polarizer	According to standard of visual inspection（inside viewing area）	Minor
	8.Bubble in polarizer	According to standard of visual inspection（inside viewing area）	Minor
	9.LCD's rainbow color	Strong deviation color（or Newton ring） of LCD ……rejected. Or according to limited sample （if needed, and inside viewing area）	Minor
	10.FPC	Burned area or wrong part number is on FPC. The symbol, character, and mark of FPC are unidentifiable. The stripped solder mask, A>1.0mm 0.3mm < stripped solder mask or visible circuit, A<1.0mm,and the number is ≧4 pieces. Particle between circuits in solder mask.. Circuit is peeled off or cracked. Any circuit risen or exposed. 0.2mm< Area of solder ball, A is ≦0.4mm,the number of solder ball is ≧3 pieces. The magnitude of solder ball, A is>0.4mm.	Minor

5.3 Standard of visual inspection

Class	Item	Judgment	Class
Electrical	11.Electrical and optical characteristics （contrast、VOP、chromaticity…etc）	According to specification or drawing. （inside viewing area）	Critical
	12.Missing pattern	Missing dot、line、character…..rejected	Critical
	13.Short circuit、wrong pattern display	Non display、wrong pattern display、current consumption out of specification……rejected	Critical
	14.Pin hole、pattern deformity	According to standard of visual inspection	Minor
	15.Black spot、white spot、black line、white line、slant line、background uneven、color uneven	Strong deviation color…..rejected Or according to limited sample full off screen（all black）…disregards	Minor
	16.Stick image （retention image）	Fixed test picture within two hours…rejected	Minor

Class	Item	Judgment
Minor	・Blemish、black spot、white spot in the LCD. ・Blemish、black spot、white spot and scratch on th polarizer	（A） Round type: unit: mm Diameter（mm.） / Acceptable Q'ty 0.2<A / 0 Note: A=（Length +Width）/ 2 （B） Liner type: unit: mm Length / Width / Acceptable Q'ty --- / W≦0.03 / Disregard L≦5 / 0.03＜W≦0.05 / 3 L≦5 / 0.05＜W≦0.07 / 1 --- / 0.07＜W / Follow round type
Minor	Bubble in polarizer	unit: mm Diameter / Acceptable Q'ty A≦0.3 / Disregard 0.3＜A≦0.5 / 1 0.5＜A / 0
Minor	Pin hole、Pattern deformity	unit: dot size Diameter / Acc. Q'ty 0.4<Φ / 0

6. Precaution

6.1 Handling

(1) Protect the panel from static, it may cause damage to the CMOS Gate Array IC.

(2) Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

(3) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.

(4) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Don't use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

(5) Pins of I/F connector shall not be touched directly with bare hands.

(6) Refrain from strong mechanical shock and / or any force to the panel. In addition to damage, this may cause improper operation or damage to the panel.

(7) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than a B pencil lead.

(8) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, staining and discoloration may occur.

(9) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.

6.2 Storage

(1) Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the panel with temperature from 0 to 35℃ and relative humidity of less than 70%.

(2) The panel shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.

6.3 Operation

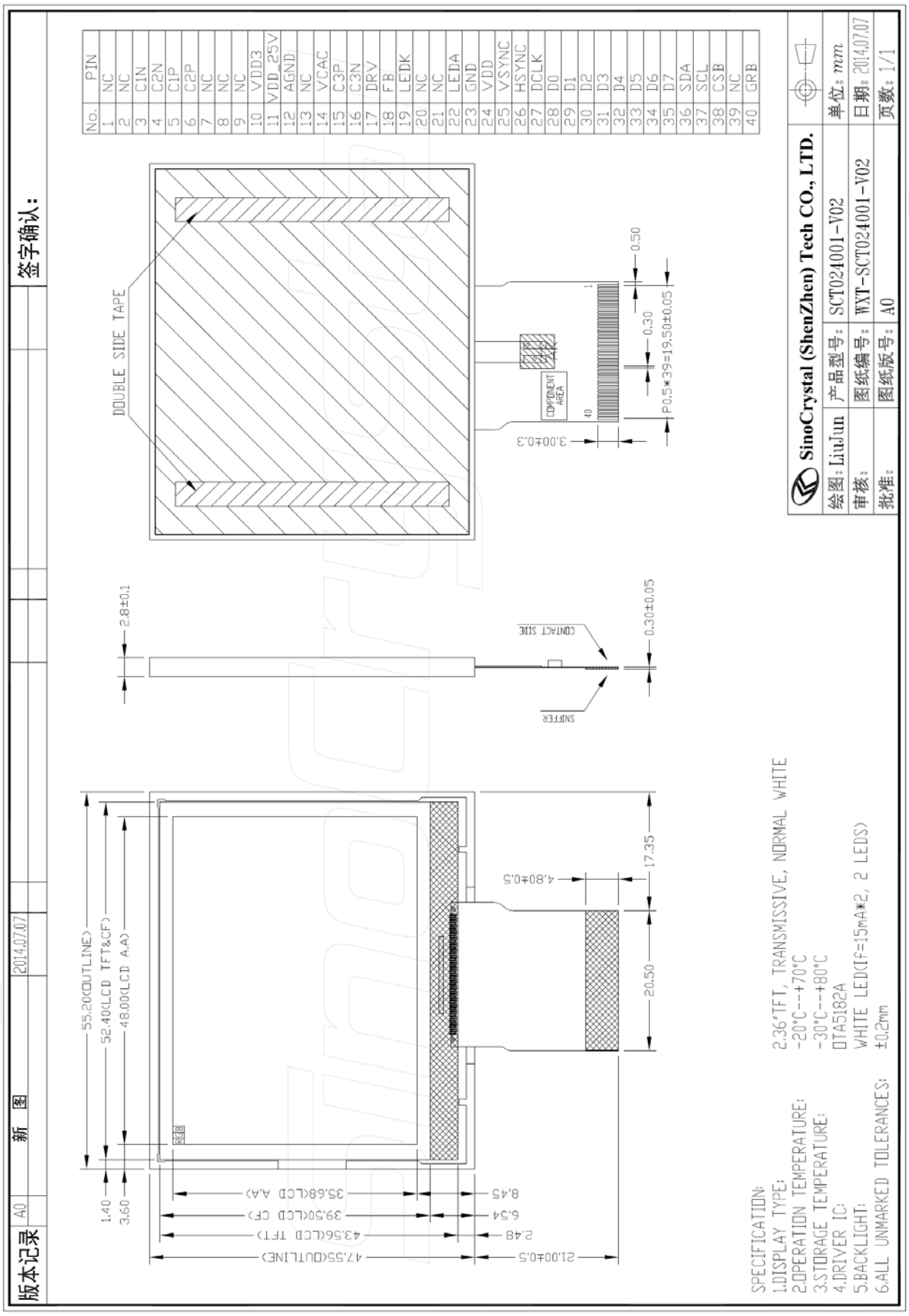
(1) The LCD shall be operated within the limits specified. Operation at values outside of these limits may shorten life, and/or harm display images.

(2) Do not exceed the absolute maximum rating value. (the supply voltage variation, Input voltage variation in part contents and environmental temperature and so on). Otherwise the panel may be damaged.

(3) If the panel displays the same pattern continuously for a long period of time, it can be the situation when the image" Sticks" to the screen.

7. Outline Dimension

Refer to SCT024001-V02 drawing.



8. Packing method

8.1 Packing Quantity (TBD)

8.2 Flowing chart (TBD)